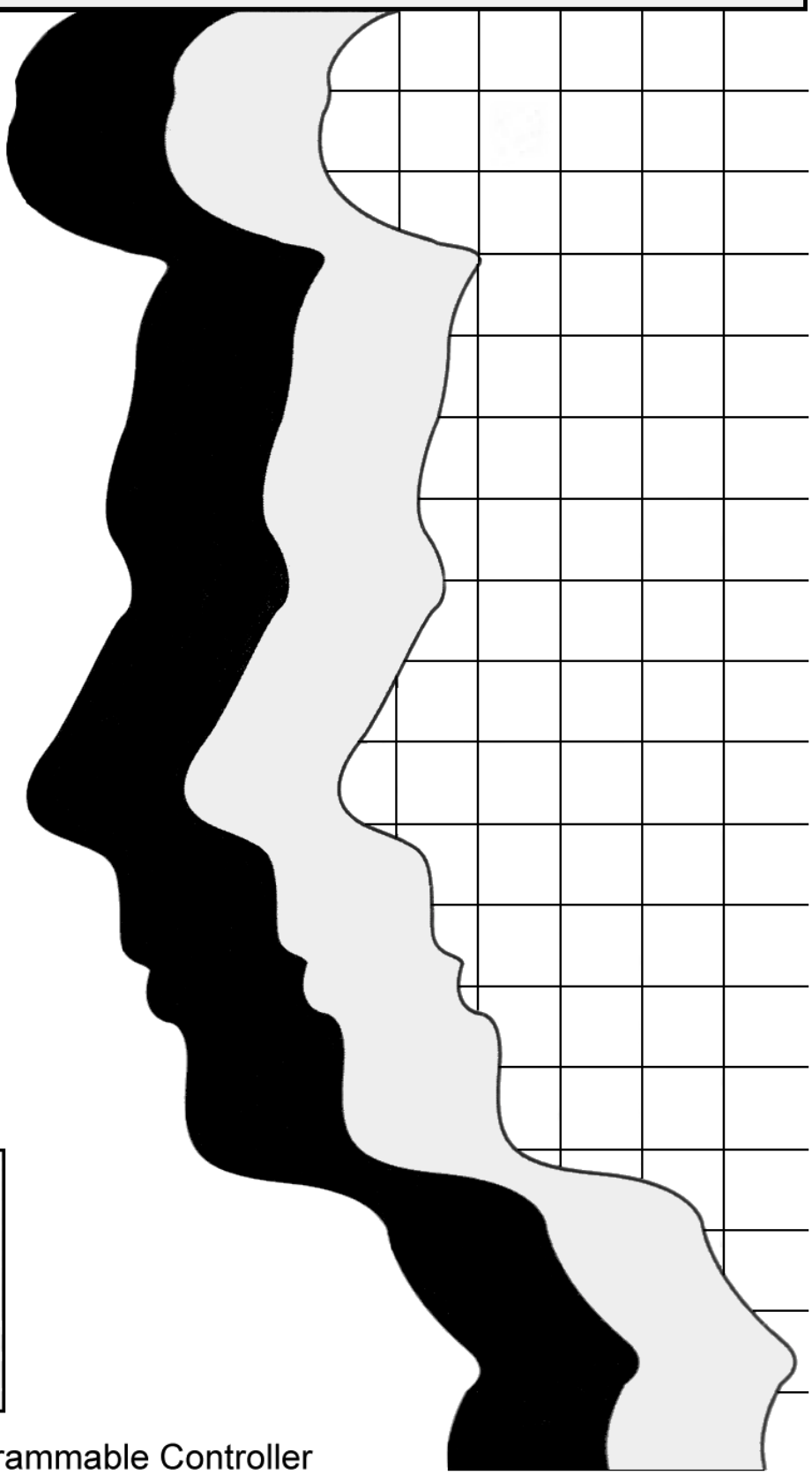
MITSUBISHI

AnS(H) CPU

User's Manual



MELSEC

Mitsubishi Programmable Controller

● SAFETY PRECAUTIONS ●

(Read these precautions before using.)

When using Mitsubishi equipment, thoroughly read this manual and the associated manuals introduced in this manual.

Also pay careful attention to safety and handle the module properly. These precautions apply only to Mitsubishi equipment. Refer to the CPU module user's manual for a description of the PC system safety precautions.

These ● SAFETY PRECAUTIONS ● classify the safety precautions into two categories: "DANGER" and "CAUTION".

⚠ DANGER	**Procedures which may lead to a dangerous condition and cause death or serious injury if not carried out properly.**
⚠ CAUTION	**Procedures which may lead to a dangerous condition and cause superficial to medium injury, or physical damage only, if not carried out properly.**

Depending on circumstances, procedures indicated by ⚠ CAUTION may also be linked to serious results.

In any case, it is important to follow the directions for usage.

Store this manual in a safe place so that you can take it out and read it whenever necessary. Always forward it to the end user.

[DESIGN PRECAUTIONS]

⚠ DANGER

- Install a safety circuit external to the PC that keeps the entire system safe even when there are problems with the external power supply or the PC module. Otherwise, trouble could result from erroneous output or erroneous operation.

  (1) Outside the PC, construct mechanical damage preventing interlock circuits such as emergency stop, protective circuits, positioning upper and lower limits switches and interlocking forward /reverse operations.

  (2) When the PC detects the following problems, it will stop calculation and turn off all output.
  - The power supply module has over current protection equipment and over voltage protection equipment.
  - The PC CPUs self-diagnostic functions, such as the watchdog timer error, detect problems. In addition, all output will be turned on when there are problems that the PC CPU cannot detect, such as in the I/O controller. Build a fail safe circuit exterior to the PC that will make sure the equipment operates safely at such times. See Section 8.1 of this user's manual for example fail safe circuits.

  See this user's manual for example fail safe circuits.

  (3) Output could be left on or off when there is trouble in the outputs module relay or transistor. So build an external monitoring circuit that will monitor any single outputs that could cause serious trouble.
- When overcurrent which exceeds the rating or caused by short-circuited load flows in the output module for a long time, it may cause smoke or fire. To prevent this, configure an external safety circuit, such as fuse.
- Build a circuit that turns on the external power supply when the PC main module power is turned on. If the external power supply is turned on first, it could result in erroneous output or erroneous operation.
- When there are communication problems with the data link, the communication problem station will enter the following condition.
  Build an interlock circuit into the PC program that will make sure the system operates safely by using the communication state information. Not doing so could result in erroneous output or erroneous operation.

  (1) For the data link data, the data prior to the communication error will be held.

  (2) The MELSECNET (II,/B,/10) remote I/O station will turn all output off.

  (3) The MELSECNET/MINI-S3 remote I/O station will hold the output or turn all output off depending on the E.C. remote setting.

  Refer to the data link manuals regarding the method for setting the communication problem station and the operation status when there are communication problem.

⚠ CAUTION

- Do not bunch the control wires or communication cables with the main circuit or power wires, or install them close to each other. They should be installed 100 mm (3.94 inch) or more from each other. Not doing so could result in noise that would cause erroneous operation.

[INSTALLATION PRECAUTIONS]

⚠ DANGER

- Use the PC in an environment that meets the general specifications contained in this manual. Using this PC in an environment outside the range of the general specifications could result in electric shock, fire, erroneous operation, and damage to or deterioration of the product.
- Install so that the pegs on the bottom of the module fit securely into the base unit peg holes, and use the specified torque to tighten the module's fixing screws. Not installing the module correctly could result in erroneous operation, damage, or pieces of the product falling.
- Tightening the screws too far may cause damages to the screws and/or the module, resulting in fallout, short circuits, or malfunction.
- When installing more cables, be sure that the base unit and the module connectors are installed correctly. After installation, check them for looseness. Poor connections could result in erroneous input and erroneous output.
- Correctly connect the memory cassette installation connector to the memory cassette. After installation, be sure that the connection is not loose. A poor connection could result in erroneous operation.
- Do not directly touch the module's conductive parts or electronic components. Doing so could cause erroneous operation or damage of the module.

[WIRING PRECAUTIONS]

⚠ DANGER

- Completely turn off the external power supply when installing or placing wiring. Not completely turning off all power could result in electric shock or damage to the product.
- When turning on the power supply or operating the module after installation or wiring work, be sure that the module's terminal covers are correctly attached. Not attaching the terminal cover could result in electric shock.

⚠ CAUTION

- Be sure to ground the FG terminals and LG terminals to the protective ground conductor. Not doing so could result in electric shock or erroneous operation.
- When wiring in the PC, be sure that it is done correctly by checking the product's rated voltage and the terminal layout. Connecting a power supply that is different from the rating or incorrectly wiring the product could result in fire or damage.
- Do not connect multiple power supply modules in parallel. Doing so could cause overheating, fire or damage to the power supply module. If the terminal screws are too tight, it may cause falling, short circuit or erroneous operation due to damage of the screws or module.
- Tighten the terminal screws with the specified torque. If the terminal screws are loose, it could result in short circuits, fire, or erroneous operation.
- Tightening the terminal screws too far may cause damages to the screws and/or the module, resulting in fallout, short circuits, or malfunction.
- Be sure there are no foreign substances such as sawdust or wiring debris inside the module. Such debris could cause fires, damage, or erroneous operation.

[WIRING PRECAUTIONS]

⚠ CAUTION

- External connections shall be crimped or pressure welded with the specified tools, or correctly soldered. For information regarding the crimping and pressure welding tools, see the I/O module's user's manual. Imperfect connections could result in short circuit, fires, or erroneous operation.

[STARTUP AND MAINTENANCE PRECAUTIONS]

⚠ DANGER

- Do not touch the terminals while power is on. Doing so could cause shock or erroneous operation.
- Correctly connect the battery. Also, do not charge, disassemble, heat, place in fire, short circuit, or solder the battery. Mishandling of battery can cause overheating or cracks which could result in injury and fires.
- Switch all phases of the external power supply off when cleaning the module or tightening the terminal screws. Not doing so could result in electric shock. If the screws are too tight, it may cause falling, short circuit or erroneous operation due to damage of the screws or modules.
- Tightening the screws too far may cause damages to the screws and/or the module, resulting in fallout, short circuits, or malfunction.

⚠ CAUTION

- The online operations conducted for the CPU module being operated, connecting the peripheral device (especially, when changing data or operation status), shall be conducted after the manual has been carefully read and a sufficient check of safety has been conducted. Operation mistakes could cause damage or trouble of the module.
- Do not disassemble or modify the modules. Doing so could cause trouble, erroneous operation, injury, or fire.
- Switch all phases of the external power supply off before mounting or removing the module. If you do not switch off the external power supply, it will cause failure or malfunction of the module.

[DISPOSAL PRECAUTIONS]

⚠ CAUTION

- When disposing of this product, treat it as industrial waste.

REVISIONS

*The manual number is given on the bottom left of the back cover.

Print Date	*Manual Number	Revision
May., 1997	IB (NA) 66779-A	First edition
Nov., 1997	IB (NA) 66779-B	Correction Contents, Related manuals, Section 1.1, Section 2.1.1, 2.1.2, Section 2.2, 2.3, Chapter 3, Section 4.1.6, Section 5.1, 5.2, Section 6.1.2, Section 8.7.1, 8.7.2, Section 9.1.3, Section 11.3.1, Appendix 1, 1.1, Appendix 3.1, 3.2, Appendix 5.

INTRODUCTION

Thank you for choosing the Mitsubishi MELSEC-A Series of General Purpose Programmable Controllers. Please read this manual carefully so that the equipment is used to its optimum. A copy of this manual should be forwarded to the end user.

Contents

1. OVERVIEW

This user's manual describes the functions, specification, and handling of the A1SJHCPU general purpose PC (abbreviated as A1SJHCPU from here on), A1SHCPU general purpose PC (abbreviated as A1SHCPU), A2SHCPU general purpose PC (abbreviated as A2SHCPU), and A2SHCPU-S1 general purpose PC (abbreviated as A2SHCPU-S1).

A1SHCPU and A1SJHCPU are grouped as A1SHCPU, unless there is necessity to identify each model.

Also, A1SHCPU, A2SHCPU and A2SHCPU-S1 are grouped as AnSHCPU, unless there is necessity to identify each model.

The AnSHCPU is a compact-type building block PC. The model is one third the size of the conventional building block type PC, and allows easy operation in spite of its small size.

AnSHCPUs are miniature building block programmable controllers, which have been downsized to occupy one third of the volume of conventional building block type programmable controllers, and are designed to be easy to use in spite of their small size.

Sequence programs that have been created for the existing A0J2CPU, A0J2HCPU and A[ ]NCPU models can be used by changing the CPU type specification for the program. Moreover, since modules for use with A[ ]NCPU can be used by installing them on an extension base unit for A[ ]NCPU use, it is possible to extend the functions of an AnSCPU.

The AnSCPU has functions equivalent to those of the A2NCPU and we urge you to make the best use of these functions in order to use the equipment efficiently.

This user's manual refers to peripheral devices (A6GPP, A6PHP, IBM PC/AT, A7PU, A7PUS, and A8PUE) by using the following abbreviations.

A6GPP, A6PHP, and IBM PC/AT
(started up with SW3IVD-GPPA, MELSEC MEDOC, MELSEC MEDOC plus)
..... Abbreviated as "GPP function".
A7PU, A7PUS, and A8PUE ..... Abbreviated as "PU".

1.1 Features

(1) High-speed operation processing speed

Compared to the conventional A1SCPU, the A1SHCPU is three times and A2SHCPU (-S1) is four times faster in the operation processing speed, respectively.

Item	A1SHCPU	A2SHCPU(-S1)	A1SCPU
Operation processing speed *1	0.33 μs	0.25 μs	1 μs

*1 I/O processing : Refresh and LD instruction

(2) Addition of new dedicated instructions

The CC-Link dedicated instructions (11 instructions) have been added, making the operation even easier.

(3) Increased number of I/O device points

The actual number of I/O points is the same as the AnS series, but each CPU has 2048 points (X/Y0 to 7FF) of I/O devices.
The added I/O device can be used as the MELSECNET (/B), MELSECNET/MINI, or CC-Link.

(4) Increased file register R capacity

The capacity is now max. 8192 points (R0 to 8191), which doubled the AnS series' 4096 points (R0 to 4095).

(5) Increased memory capacity (Increased number of comment points)

The A1SHCPU has 64 k bytes, which doubled the A1SCPU's 32 k bytes. This increased the number of comment points stored in the CPU 3648 in comparison to the 1600 points in A1SCPU.

(6) Increased memory capacity (in the number of comment points)

Only for the A2SHCPU-S1: the program capacity has been increased to 30 k steps in comparison to the 14 k steps for A2SCPU.

(7) Full compatibility with A1S(S1)/A2SCPU(S1)

Because there is full compatibility of the functions and instructions with A1S(S1)/A2SCPU(S1), all software packages can be used.
For the GPP function software package, select "A3" as the CPU type to create the sequence program.
In addition, power supply module, base unit, and I/O modules can be used.

(8) Compact size

The outside dimensions of the AnSHCPU system with one power supply module, one CPU, and eight 16-point I/O modules for use with AnS mounted to the main base unit are:
430 mm (16.9 in.) (W); 130 mm (5.12 in.) (H); and 110 mm (4.33 in.) (D).

(9) Max. 8 k/14 k steps of program

An AnSCPU allows the creation of a program of up to 8 k (A1SCPU(S1)/ A1SCPUC24-R2)/ 14 k (A2SCPU(S1)) steps containing up to 26 sequence instructions, 131 basic instructions, 106 application instructions, and 11 CC-Link dedicated instructions.

In addition, microcomputer programs and utility programs created by the user can be used.

(10) SFC language compatible

An AnSCPU contains a microcomputer program area, so it can use an SFC program by using the software on an IBM personal computer.

(11) Two extension connectors, on the right and left sides.

In order to facilitate wiring wherever the extension base unit is installed, extension connectors are provided at both left and right sides of the AnSHCPU and extension cables that suit the requirements imposed by different mounting locations are available.

(12) Use either screws or DIN rail for panel installations

The AnS base unit is provided both with screw holes and, on its rear face, the fixture for mounting it to a DIN rail.

(13) Easy-to-see terminal block symbol sheet

- A terminal block symbol sheet is attached to the front of AnS I/O modules.

It is possible to write I/O device numbers, connector numbers, etc. on one side of the sheet.

- Terminal symbols for 16 I/O signals can be written on the other side.

(14) A[ ]N, A[ ]A-series I/O module and special function module compatible

By connecting an A[ ]N, A[ ]A-series extension base unit, A[ ]N, A[ ]A I/O modules or special function modules can be used.

(15) Same programming environment as other MELSEC-A CPU modules

A sequence program can be created using the peripheral device currently used for other MELSEC-A CPU modules.

For details on the applicable peripheral devices, see Section 2.2 "Cautions on System Configuration".

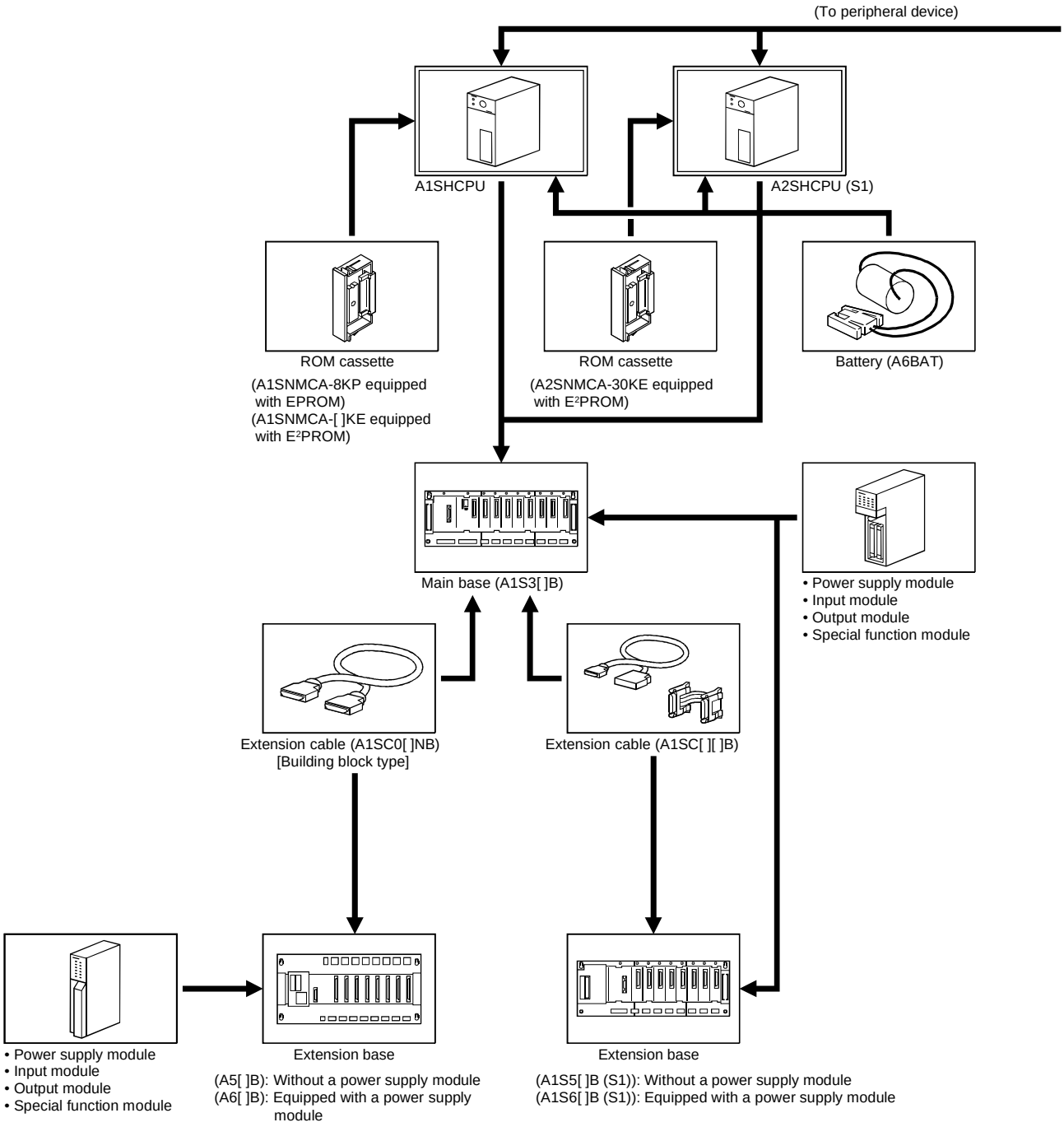
2. SYSTEM CONFIGURATION

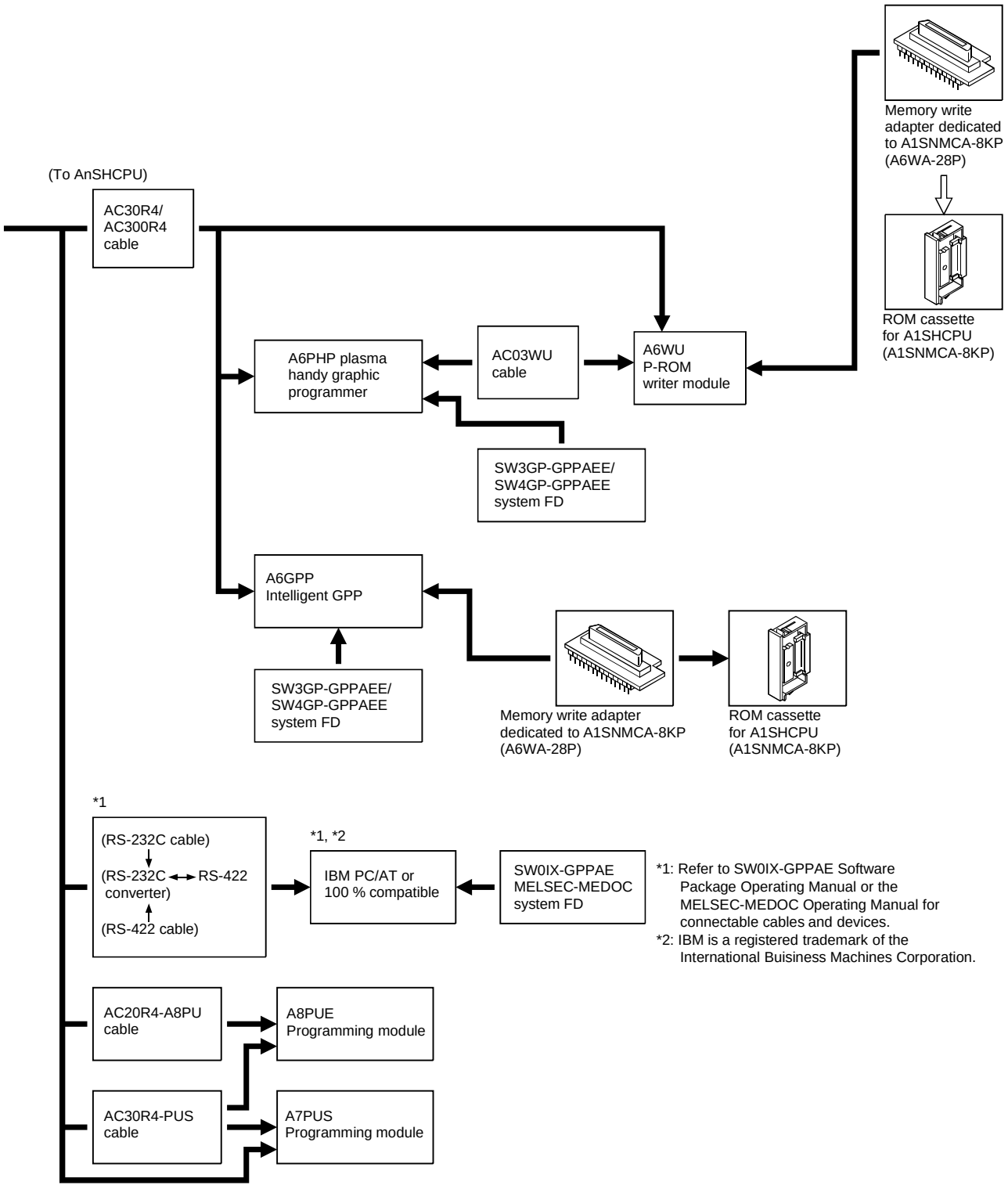
This chapter describes the applicable system configurations, cautions on configuring a system, and component devices of the AnSHCPU.

2.1 Overall Configuration

2.1.1 AnSHCPU

The figure below shows a system configuration when the AnSHCPU is used independently.





*1: Refer to SW0IX-GPPAE Software Package Operating Manual or the MELSEC-MEDOC Operating Manual for connectable cables and devices.

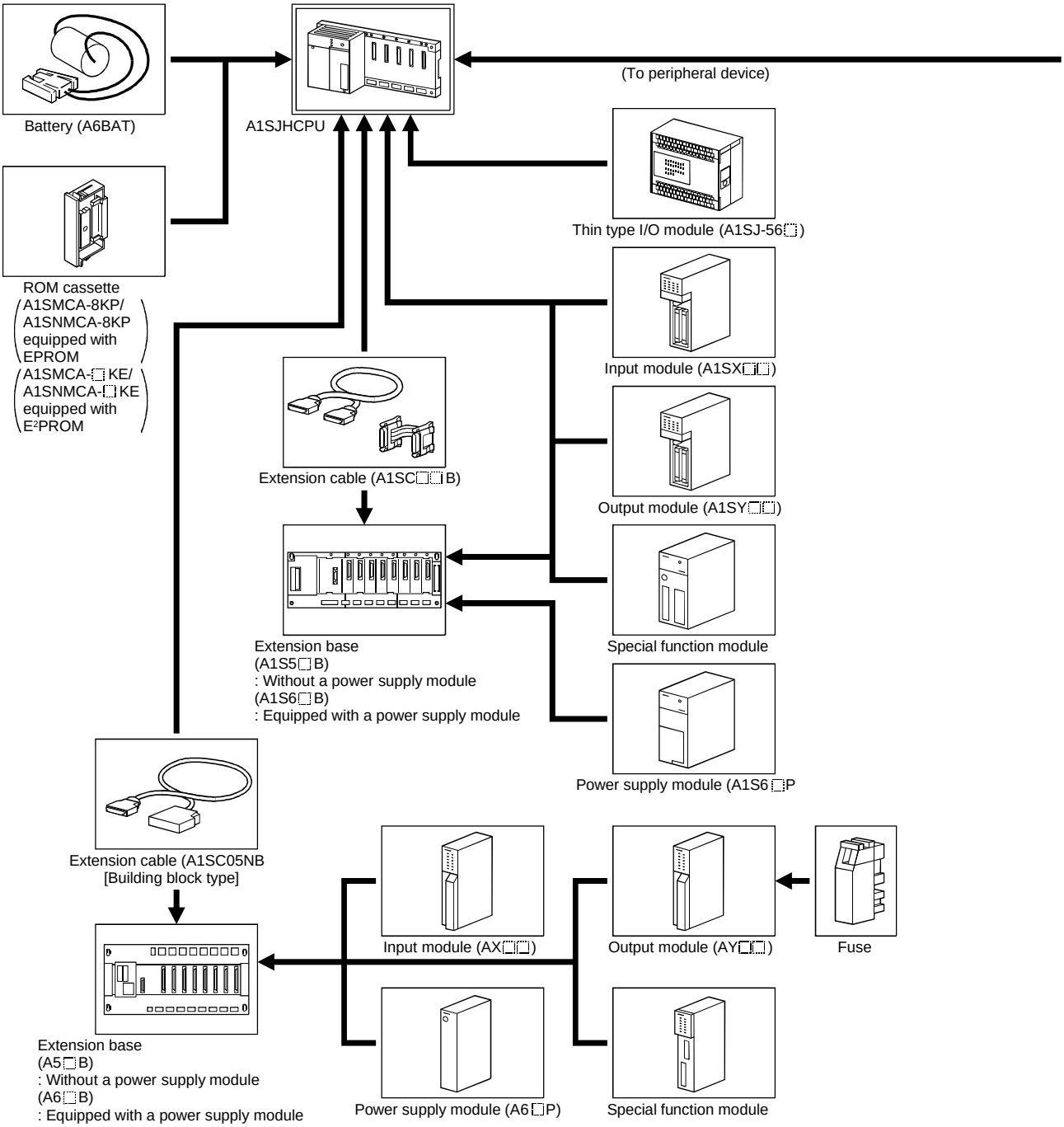
*2: IBM is a registered trademark of the International Buisiness Machines Corporation.

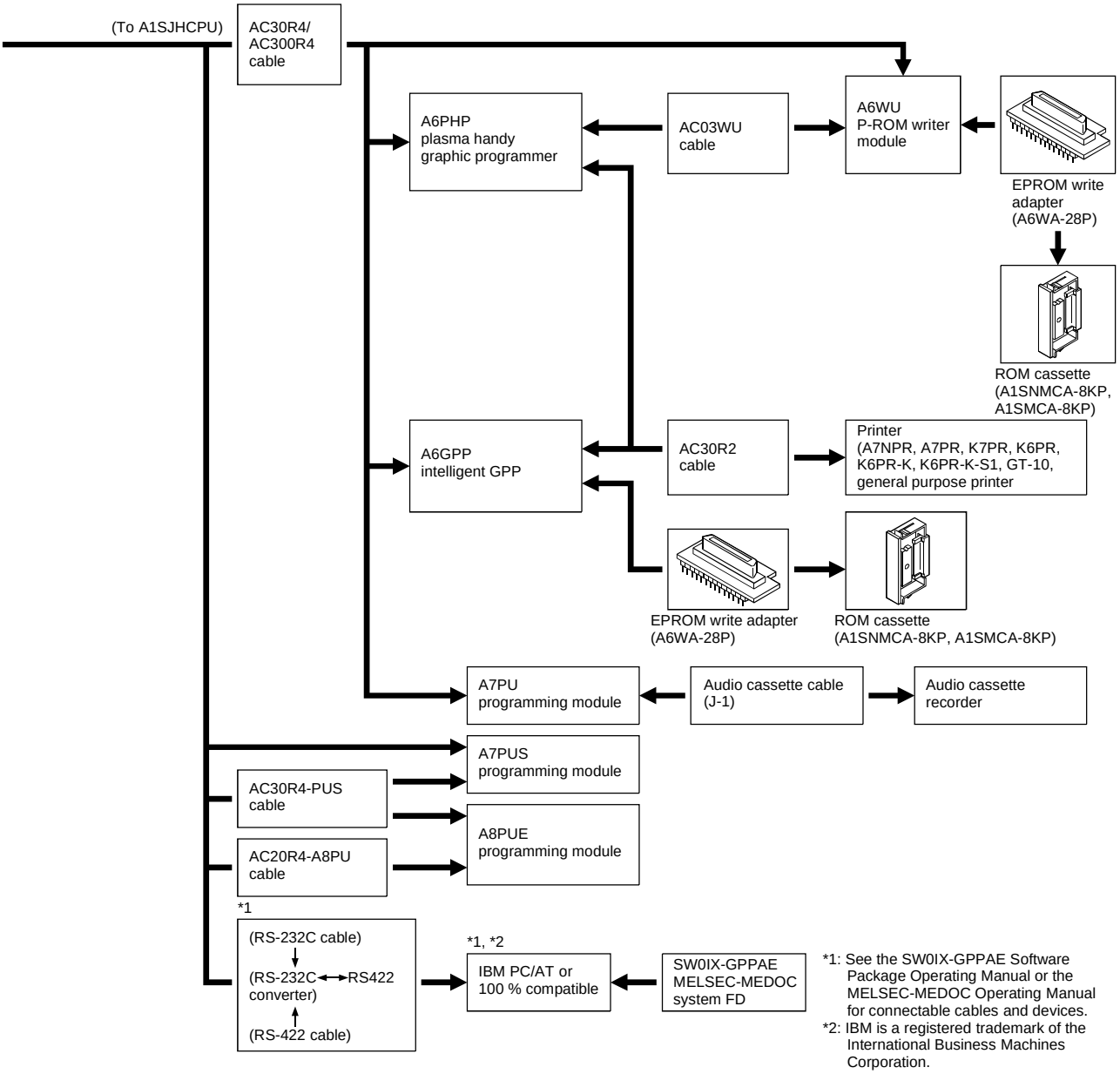
POINT

For applicable printers, cables, and ROM writers, see the operating manual for each peripheral device used.

2.1.2 A1SJHCPU

The figure below shows a system configuration and peripheral device configuration when the A1SJHCPU is used independently.




(To A1SJHCPU)
AC30R4/
AC300R4
cable
A6PHP
plasma handy
graphic programmer
AC03WU
cable
A6WU
P-ROM writer
module
EPROM write
adapter
(A6WA-28P)
ROM cassette
(A1SNMCA-8KP,
A1SMCA-8KP)
A6GPP
intelligent GPP
AC30R2
cable
Printer
(A7NPR, A7PR, K7PR, K6PR,
K6PR-K, K6PR-K-S1, GT-10,
general purpose printer
EPROM write adapter
(A6WA-28P)
ROM cassette
(A1SNMCA-8KP, A1SMCA-8KP)
A7PU
programming module
Audio cassette cable
(J-1)
Audio cassette
recorder
A7PUS
programming module
AC30R4-PUS
cable
A8PUE
programming module
AC20R4-A8PU
cable
*1
(RS-232C cable)
(RS-232C RS422
converter)
(RS-422 cable)
*1, *2
IBM PC/AT or
100 % compatible
SW0IX-GPPAE
MELSEC-MEDOC
system FD
*1: See the SW0IX-GPPAE Software
Package Operating Manual or the
MELSEC-MEDOC Operating Manual
for connectable cables and devices.
*2: IBM is a registered trademark of the
International Business Machines
Corporation.

2.2 Cautions on Configuring a System

This section describes the hardware and software that can be used with the AnSHCPU.

2.2.1 Hardware

(1) I/O module

An A[ ]N or A[ ]A building-block type I/O module can be used by loading it to the A5[ ]B/A6[ ]B extension base.

(2) Special function module

(a) An A[ ]N or A[ ]A special function module can be used by loading it to the A5[ ]B/A6[ ]B extension base.

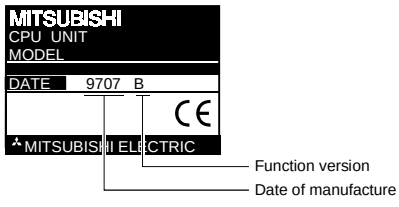
(b) Limits are imposed on the number of the following special function modules that can be loaded.

AD51(S3) AD51FD (S3) AJ71C24(S3/S6/S8) AJ71P41 AJ61BT11 *1	AD51H(S3) AD57G(S3) AJ71C22 AJ71UC24 AJ71E71	Up to 2
A1SD51S A1SJ71C24-R2(PRF/R4) A1SJ71UC24-R2(PRF/R4) A1SJ71E71-B2/B5	A1SJ61BT11 *1	
AI61(S1) A1SI61		Only 1
AJ71AP21(S3) AJ71AT21B AJ71BR11	AJ71AR21 AJ71LP21	Only 1
A1SJ71AT21B A1SJ71AP21(S3) A1SJ71LP21	A1SJ71AR21 A1SJ71BR11	

*1 At intelligent mode

POINT

When the dedicated instruction for the CC-Link is used, use the master module with ("9707 B" or later), shown right, inscribed in the DATE column of the rated plate.

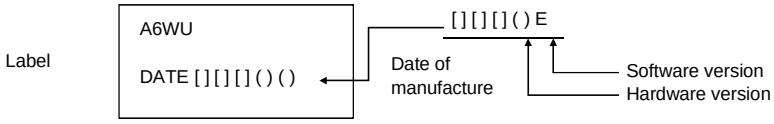


(3) Peripheral device

(a) Points to note when using an A6WU P-ROM writer

1) When using an A1SHCPU

Use an A6WU P-RPM writer module whose software version is "E" or later.



(b) The A6WU P-ROM writer module cannot be installed directly on the AnSHCPU (add-on installation impossible).
Only handheld connection using cables is possible.

(c) When writing to an A1SHCPU/A1SJHCPU using an A6WU series P-ROM writer module, SERIAL must be selected.

(d) Among the programming modules (A7PU, A7PUS and A8PUE), only the A7PUS can be added on.
The other models (A7PU and A8PUE) are available only as the handheld installation type which requires cables.

(4) EPROM memory cassette ROM partition

Partitioning the EPROM memory cassette with an A6GPP (SW4GP-GPPA)/A6WU requires a memory write adapter (optional). The valid combinations of memory cassette and memory write adapter are as follows :

CPU model	Memory cassette model	Memory write adapter model
A1SHCPU	A1SNMCA-8KP	A6WA-28P
A1SJHCPU, A1SHCPU	A1SMCA-8KP, A1SNMCA-8KP	A6WA-28P

(5) Program write during operation with E^2PROM

(a) When an operation is executed using an E^2PROM, writing is not possible in the RUN status. If writing is attempted in this status, the following messages will be sent to the peripheral devices :

- When the SW3GP-GPPA is used : "PC COMMUNICATIONS ERROR : ERROR CODE = 17" is displayed.
- When SW0RX-GPPA is used : "PC COMMUNICATIONS ERROR : ERROR CODE = 17" is displayed.
- When the A7PU is used : "PC NOT RESPOND" is displayed.

(b) Programs cannot be written from peripheral devices which are connected to the computer link module or other stations of the MELSECNET.

Write programs from peripheral devices connected to the AnSHCPU's RS-422.

(c) When writing a program to the A1SNMCA-2KE, set the parameter for main sequence program capacity to 2 k steps or less.

Programs written with a main sequence program capacity setting of 3 k steps or over cannot work properly.

Checking between the AnSHCPU and a peripheral device will result in a mismatch.

2.2.2 Software packages

(1) Specifying the system startup software package and startup model

(a) For AnSHCPU, startup with the PC model "A3."

(b) Perform the PC type setting as shown below when using conventional peripheral devices.

Peripheral device	Software package	CPU type			Remarks
		A1SJH/A1SH	A2SH	A2SH-S1	
A6PHP	SW3GP-GPPAEE	A3 *1	A3	A3	EPROM write not possible.
	SW4GP-GPPAEE				*1
A6GPP	SW3-GPPAEE				EPROM write not possible.
	SW3GP-GPPAEE				
	SW4GP-GPPAEE				*1
IBM PC/AT	SW[ ]IVD-GPPA *2				
	MELSEC MEDOC				
	MELSEC MEDOC plus				
A6WU		A1SH	A2SH	A2SH1	• "A1SH" is displayed when the system is started up with software version "E" or later. Cannot be used if software version "D" or before. • Add-on mounting is not possible.
A7PU					• "A1SH" is displayed when the system is started up with software version "E" or earlier. Cannot be used if the software version is "F" or later. • Add-on mounting is not possible.
A7PUS, A8PUE					"A1SH" is displayed when the system is started up.

*1 When performing the A1SHCPU ROM cutoff with SW4GP-GPP, the startup model must be changed.
Set "AOJ2H" for version Q and earlier, and "A1S" for version R and later.

*2 The software package that can select the CPU model to use, is shown below.
Version 70H or later

POINT

(1) When an A6GPP, or A6PHP is used, use SW3-GPPAEE, SW3-HGPAEE, SW3GP-GPPAEE, or SW4GP-GPPAEE as the system startup software. Other old software packages cannot be used.

i) Utility package

The applicable utility packages are listed below.

- SW0GHP-UTLPC-FN1
- SW0GHP-UTLPC-FN0
- SW0GHP-UTLP-FD1
- SW0-AD57P
- SW1GP-AD57P

(c) Select "A3CPU" when an SW0GHP-UTLPC-FN1 or SW0GHP-UTLP-FD1 is started up.

(d) If both an SW1GP-AD57P and another utility package are used in combination, specify "AD57P-COM" as the file name.

2.3 System Equipment

The following table shows the list of modules and devices which can be used for an AnS system.

(1) AnSCPU dedicated modules

Item	Model	Description		Number of inputs/outputs [I/O allocation module type]	Current consumption		Remarks	* Approved standard
					5 V DC	24 V DC		
CPU module	A1SHCPU	See the "Performance Specifications" in Chapter 4. (Number of I/O points : 256, memory capacity : 64 k bytes)		—	0.30	—	RAM memory embedded	UL/cUL
	A1SJHCPU	See the "Performance Specifications" in Chapter 4. (Number of I/O points : 256, memory capacity : 64 k bytes)						
	A2SHCPU	See the "Performance Specifications" in Chapter 4. (Number of I/O points : 512, memory capacity : 64 k bytes)		—	0.40		RAM memory embedded	
	A2SHCPU-S1	See the "Performance Specifications" in Chapter 4. (Number of I/O points : 1024, memory capacity : 192 k bytes)						
Power supply module	A1S61P	5 V DC, 5 A	Input 100/200 V AC	—	—	—	Loaded to the slot for main base or extension base power supply.	
	A1S62P	5 V DC, 3 A/24 V DC 0.6 A						
	A1S63P	5 V DC, 5 A	Input 24 V DC					
	A1S61PEU	5 V DC, 5 A	Input 200 V AC	—	—	—		UL/cUL
	A1S62PEU	5 V DC, 3 A/24 V DC 0.6A						
	A1S61PN	5 V DC, 5 A	Input 100/200 V AC					
	A1S62PN	5 V DC, 3 A/24 V DC 0.6A						
Input module	A1SX10	16-point 100 V AC input module		16 [16 inputs]	0.05	—		UL/cUL
	ASX10EU	16-point 100 V AC input module		16 [16 inputs]	0.05	—		
	A1SX20	16-point 200 V AC input module		16 [16 inputs]	0.05	—		
	A1SX20EU	16-point 200 V AC input module		16 [16 inputs]	0.05	—		
	A1SX30	16-point 12/24 V DC, 12/24 V AC input module		16 [16 inputs]	0.05	—		UL/cUL
	A1SX40	16-point 12/24 VDC input module		16 [16 inputs]	0.05	—		
	A1SX40-S1	16-point 24 V DC input module		16 [16 inputs]	0.05	—		
	A1SX40-S2	16-point 24 V DC input module		16 [16 inputs]	0.05	—		
	A1SX41	32-point 12/24 V DC input module		32 [32 inputs]	0.08	—		
	A1SX41-S2	32-point 24 V DC input module		32 [32 inputs]	0.08	—		
	A1SX42	64-point 12/24 V DC input module		64 [64 inputs]	0.09	—		
	A1SX42-S2	64-point 24 V DC input module		64 [64 inputs]	0.09	—		
	A1SX71	32-point 5/12 V DC input module		32 [32 inputs]	0.075	—		
	A1SX80	16-point 12/24 V DC sink/source input module		16 [16 inputs]	0.05	—		
	A1SX80-S1	16-point 24 V DC sink/source input module		16 [16 inputs]	0.05	—		
	A1SX80-S2	16-point 24 V DC input module		16 [16 inputs]	0.05	—		
	A1SX81	32-point 12/24 V DC sink/source input module		32 [32 inputs]	0.08	—		
	A1SX81-S2	32-point 24 V DC input module		32 [32 inputs]	0.08	—		

*: Class 2 power supply recognized by the UL/cUL Standard is required for 5/12/24 V DC modules.

Item	Model	Description	Number of inputs/outputs [I/O allocation module type]	Current consumption		Remarks	* Approved standard
				5 V DC	24 V DC		
Output module	A1SY10	16-point relay contact output module (2 A)	16 [16 outputs]	0.12	0.09		UL/cUL
	A1SY10EU	16-point relay contact output module (2 A)	16 [16 outputs]	0.12	0.09		
	A1SY14EU	16-point relay contact output module (2 A)	16 [16 outputs]	0.12	0.09		
	A1SY18A	8-point relay contact output module (2 A) All points independent	16 [16 outputs]	0.24	0.075		
	A1SY18AEU	8-point relay contact output module (2 A)	16 [16 outputs]	0.24	0.075		UL/cUL
	A1SY22	16-point triac output module (0.6 A)	16 [16 outputs]	0.27	(200 V AC) 0.004		
	A1SY28A	8-point triac output module (1 A) All points independent	16 [16 outputs]	0.11	—		
	A1SY28AEU	8-point triac output module (0.6 A)	16 [16 outputs]	0.27	—		UL/cUL
	A1SY40	16-point 12/24 V DC transistor output module (0.1 A) sink type	16 [16 outputs]	0.27	0.016		
	A1SY41	32-point 12/24 V DC transistor output module (0.1 A) sink type	32 [32 outputs]	0.50	0.016		
	A1SY42	64-point 12/24 V DC transistor output module (0.1 A) sink type	64 [64 outputs]	0.93	0.016		
	A1SY50	16-point 12/24 V DC transistor output module (0.5 A) sink type	16 [16 outputs]	0.12	0.12		
	A1SY60	16-point 24 V DC transistor output module (2 A) sink type	16 [16 outputs]	0.12	0.015		
	A1SY60E	16-point 12 V DC transistor output module (1 A) source type	16 [16 outputs]	0.20	0.01		
	A1SY68A	8-point 5/12/24/48 V DC transister output module sink/source type All points independent	16 [16 outputs]	0.13	—		
	A1SY71	32-point 5/12 V DC transistor output module (0.016 A) sink type	32 [32 outputs]	0.40	0.15		
	A1SY80	16-point 12/24 V DC transistor output module (0.8 A) source type	16 [16 outputs]	0.12	0.04		
	A1SY81	32-point 12/24 V DC transistor output module (0.1 A) source type	32 [32 outputs]	0.50	0.016		
	A1SY81EP	32-point 12/24 V DC transistor output module (0.1/0.05 A) source type	32 [32 outputs]	0.50	0.016		
Input/ output combi-nation module	A1SH42	32-point 12/24 V DC input module 32-output 12/24 V DC transistor output module (0.1 A) sink type	32 [32 outputs]	0.50	0.008		
	A1SX 48Y18	8-point 24 V DC input module 8-output relay contact output module	16 [16 outputs]	0.085	0.045		
	A1SX 48Y58	8-point 24 V DC input module 8-output 12/24 V DC transistor output module	16 [16 outputs]	0.06	0.06		UL/cUL
	A1SJ-56DR	32-point 12/24 V DC input module sink type 24-point 24 VDC/240 V AC relay contact output module (2 A)	128 points (slot 0: 64 points slot 1 to 4: Vacant 16 points)	0.22	0.14	Install to A1SJHCPU. (Not installable to the extension base.)	
	A1SJ-56DT	32-point 12/24 V DC input module sink type 24-point 24 V DC transistor output module (0.5 A) sink type		0.22	—		
Dynamic input module	A1S42X	16-, 32-, 48- and 64-point 12/24 V DC dynamic input module	Number of set points (Inputs [ ])	0.08	—		
Dynamic output module	A1S42Y	16-, 32-, 48-, and 64-point 12/24 V DC dynamic output module	Number of set points (Outputs [ ])	0.10	0.008		
Blank cover	A1SG60	Keeps unused slots free from dust	16 [empty]	—	—		

* : Class 2 power supply recognized by the UL/cUL Standard is required for 5/12/24 V DC modules

Item	Model	Description	Number of inputs/outputs [I/O allocation module type]	Current consumption		Remarks	* Approved standard
				5 V DC	24 V DC		
Dummy module	A1SG62	16-, 32-, 48-, and 64-input selectable module	Number of set points ([ ] inputs)	—	—		
40-pin connector	A6CON1	Soldered joint type	—	—	—		UL/cUL
	A6CON2	Solderless attachment type					
	A6CON3	Pressed joint type					
37-pin D-sub connector	A6CON1E	Soldered joint type					
	A6CON2E	Solderless attachment type					
	A6CON3E	Pressed joint type					
Pulse catch module	A1SP60	Pulse input module with short ON time (Pulse : min. 0.5 msec) 16-point inputs	16 [16 outputs]	0.055	—		UL/cUL
Analog timer module	A1ST60	For changing timer set values(0.1 to 1.0 sec, 1 to 10 sec, 10 to 60 sec, 60 to 600 sec) by potensiometer. Analog timer 8 points	16 [16 outputs]	0.055	—		
Interrupt module	A1SI61	For specifying execution of an interrupt program. Interrupt module (Interrupt input points : 16)	32 [Special 32-point]	0.057	—		
High-speed counter module	A1SD61	32-bit signed binary 50 KBPS, 1 channel	32 [Special 32-point]	0.35	—		
Tempera-ture ad-justment module	A1S62TCTT-S2	Transistor output, thermocouple input 2 channels/module PID control : ON/OFF pulse	32 [Special 32-point]	0.28	—		
	A1S62TCTTBW-S2	Transistor output, thermocouple input 2 channels/module PID control : ON/OFF pulse, heater wire breakage detection function			—		
	A1S62TCRT-S2	Transistor output, platinum temperature-measuring resistor input 2 channels/module PID control : ON/OFF pulse			—		
	AS62TCRTBWS-2	Transistor output, platinum temperature-measuring resistor input 2 channels/module PID control : ON/OFF pulse, heater wire breakage detection function		0.28	—		
	A1S64TCTT-S1	Transistor output, thermocouple input 4 channels/module PID control : ON/OFF pulse or 2-position control	32 [Special 32-point]	0.42	—		
	A1S64TCTTBWS-1	Transistor output, thermocouple input 4 channels/module PID control : ON/OFF pulse or 2-position control Heater wire breakage detection function			—		
	A1S64TCRT-S1	Transistor output, thermocouple input 4 channels/module PID control : ON/OFF pulse or 2-position control			—		
	A1S64TCRTBW-S1	Transistor output, thermocouple input 4 channels/module PID control : ON/FOO pulse or 2-position control Heater wire breakage detection function		0.42	—		

* : Class 2 power supply recognized by the UL/cUL Standard is required for 5-12-24 V DC modules.

Item	Model	Description	Number of inputs/outputs [I/O allocation module type]	Current consumption		Remarks	* Approved standard
				5 V DC	24 V DC		
A-D converter module	A1S64AD	4 to 20 mA / 0 to 10 V Analog 4 channels	32 [Special 32-point]	0.4	—		
Tempera-ture-digital converter module	A1S62RD3	For connecting a Pt100 (3-wire type) Temperature input : 2 channels	32 [Special 32-point]	0.54	—		
	A1S62RD4	For connecting a Pt100 (4-wire type) Temperature input : 2 channels	32 [Special 32-point]	0.44	—		
D-A converter module	A1S62DA	4 to 20 mA / 0 to 10 V Analog output : 2 channels	32 [Special 32-point]	0.8	—		UL/cUL
Computer link module	A1SJ71(U)C24-R2	Computer link functions RS-232C : 1 channel	32 [Special 32-point]	0.1	—		
	A1SJ71(U)C24-PRF	Computer link and printer functions RS-232C : 1 channel	32 [Special 32-point]	0.1	—		
	A1SJ71(U)C24-R4	Computer link and multidrop link functions RS-422/485 : 1 channel	32 [Special 32-point]	0.1	—		
Intelligent communi-cation module	A1SD51S	Interpreter BASIC, Compile BASIC RS-232C : 2 channels RS-422/485 : 1 channel	32 [Special 32-point]	0.4	—		
Ethernet interface module	A1SJ71E71-B2	10 base 2 (Cheapernet)	32 [Special 32-point]	0.52	—		
	A1SJ71E71-B5	10 base 5 (Ethernet)	32 [Special 32-point]	0.35	—		
Position-ing module	A1SD70	For 1-axis position control, speed control, speed position control. Analog voltage output (0 to ± 10 V)	32 [Special 32-point]	0.3	—		
	A1SD71-S2	For position control, for speed control, for speed position control. Pulse train output, 2 axes (independent/simultaneous 2-axis control, direct interpolation)	48 [Special 48-point]	0.8	—		UL/cUL
Position-ing module	A1SD71-S7	Allows alteration of the output speed setting of a manual pulse generator for position control. Pulse train output, 2 axes (independent/simultaneous 2-axis control, direct interpolation)	48 [Special 48-point]	0.8	—		
ID interface module	A1SJ71D1-R4	ID interface module Reader/writer connection : 1	32 [Special 32-point]	0.25	0.1		
	A1SJ71D2-R4	ID interface module Reader/writer connection : 2	32 [Special 32-point]	0.25	0.15		UL/cUL
Paging module	A1SD21-S1	Number of entries for calling control trigger device 2000 : maximum word number of 40 (Half-character) 1120 : maximum word number of 80 (Half-character) Number of entries for receiver number : 1000	32 [Special 32-point]	0.14	—		
Analog I/O module	A1S63ADA	Analog input : 2 channel Simple loop Analog output : 1 channel Control possible	32 [Special 32-point]	0.8	—		

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Item	Model	Description	Number of inputs/outputs [I/O allocation module type]	Current consumption		Remarks	* Approved standard
				5 V DC	24 V DC		
High-speed counter module	A1SD62 A1SD62E	24-bit binary 100 k BPS, 2 channels	32 [Special 32-point]	0.14	—		
	A1SD62D	24-bit binary 100 k BPS, 2 channels	32 [Special 32-point]	0.14 0.25	—		
MELSECNET (II) data link module	A1SJ71AP21	For master or local station of MELSECNET (II) optical data link	32 [Special 32-point]	0.33	—		
	A1SJ71AP21-S3	For master or local station of MELSECNET (II) data link module system (GI type optical fiber cable)	32 [Special 32-point]	0.33	—		
	A1SJ71AR21	For master or local station of MELSECNET (II) coaxial data link	32 [Special 32-point]	0.8	—		
MELSECNET/B data link module	A1SJ71AT21B	For master or local station of MELSECNET/B data link system	32 [Special 32-point]	0.66	—		
	A1SJ72T25B	For remote I/O station of MELSECNET/B data link system	—	0.3	—		
MELSECNET/10 data link module	A1SJ71LP21	For control station, master station, and local station of the MELSECNET/10 data link module system (For SI type optical fiber cable, double loop)	32 [Special 32-point]	0.65	—		UL/cUL
	A1SJ71BR11	For control station, master station, and local station of the MELSECNET/10 data link module system (For coaxial cable, single bus)	32 [Special 32-point]	0.80	—		
CC-Link system master-local module	A1SJ61BT11	For the master station of the C.C-Link data link system (Dedicatedly for shielded twisted pair cable)	32 [32 outputs]	0.40	—		
MELSECNET/MINI-S3 master module	A1SJ71PT32-S3	Used to control up to 64 MELSECNET/MINI-S3 master stations, and a total of 512 remote I/O points and remote terminals.	Exclusive I/O mode: 32 [Special 32-point] Expansion mode: 48 [Special 48-point]	0.35	—		
	A1SJ71T32-S3	MELSECNET/MINI-S3 master station Remote I/O and remote terminal controls are performed for a total of 512 I/O points with maximum of 64 stations. (Dedicatedly for twisted pair cable)	I/O dedicated mode 32 [Special 32-point] Expansion mode: 48 [Special 48-point]	0.30	—		
MELSECNET-I/O LINK master module	A1SJ51T64	MELSECNET-I/O LINK master station. Performs I/O LINK remote I/O module control for a total of 128 I/O points with maximum of 16 stations.	64 [64 outputs]	0.115	0.09		
Simulation module	A6SIM-X64Y64	I/O simulation module used by connecting to the basic base. Desktop debugging is possible without installing the I/O module to the base unit. Use the AnS series extension cable between the AnS series basic base and A6SIM-X64Y64.	64 [64 inputs] 64 [64 outputs]	TYP. 0.3 (all points on)	—		
Graphic operation terminal	A64GOT-L A64GOT-LT21B	Compact graphic operation terminal - monitor screen included model (black and white LCD) 250 monitor screens, 255 parts.	—	—	0.4		UL/cUL

* : Class 2 power supply recognized by the UL/cUL Standard is required for 5-12-24 V DC modules.

Item	Model	Description	Number of inputs/outputs [I/O allocation module type]	Current consumption		Remarks	* Approved standard
				5 V DC	24 V DC		
Graphic operation terminal	A77GOT-S5	Large graphic operation terminal - monitor screen included model (black and white LCD, color LCD, EL) 250 monitor screens, 255 parts	—	—	—	When connected via bus, 32 special points are occupied. Consumed power : 100 VA	UL/cUL
	A850GOT	Mid-size graphic operation terminal - monitor included model (black and white LCD, STN color LCD) Base/window screen : 1024 pixels	—	—	0.5 (when connecting MELSECNET: 0.7)	When connected via bus, 32 special points are occupied.	
	A851GOT				0.5		
	A870GOT	Large graphic operation terminal - monitor screen included model (STN/TFT color EL) Base/window screen : 1024 pixels	—	—	—	When connected via bus, 32 special points are occupied. Consumed power: 100 VA	
	A810GOT	Large graphic operation terminal CRT connection model for monitor Base/window screen : 1024 pixels					
Main base unit	A1S32B	Up to two I/O modules can be loaded.	—	—	—	Equipped with two extension connectors: one is on the right; the other on the left side	
	A1S33B	Up to three I/O modules can be loaded.					
	A1S35B	Up to five I/O modules can be loaded.					
	A1S38B	Up to eight I/O modules can be loaded.					
Extension base unit	A1S52B(S1)	Up to two I/O modules can be loaded.	—	—	—	Power supply module cannot be loaded (power is supplied from the main base unit).	
	A1S55B(S1)	Up to five I/O modules can be loaded.					
	A1S58B(S1)	Up to eight I/O modules can be loaded.					
	A1S65B(S1)	Up to five I/O modules can be loaded.	—	—	—	Needs a power supply module.	
	A1S68B(S1)	Up to eight I/O modules can be loaded.					
Extension cable	A1SC01B	0.055 m (2.17 in.) long flat cable	—	—	—	For extension on the right side	
	A1SC03B	0.33 m (11.8 in.) long	—	—	—	Extension base unit connection cable	
	A1SC07B	0.7 m (27.6 in.) long					
	A1SC12B	1.2 m (47.24 in.) long					
	A1SC30B	3 m (118.11 in.) long					
	A1SC60B	6 m (236.22 in.) long					
	A1SC05NB	0.45 m (17.72 in.) long	—	—	—	A[ ]N, A[ ]A extension base cable	
	A1SC07NB	0.7 m (27.6 in.) long					
	A1SC30NB	4.3 m (118.11 in.) long	—	—	—		
	A1SC07NB	5 m (196.85 in.) long	—	—	—		

* : Class 2 power supply recognized by the UL/cUL Standard is required for 5-12-24 V DC modules.

Item		Model	Description	Applicable model	* Approved standard
Memory cassette	EPROM	A1SMCA-8KP	8 k steps, equipped with EPROM (directly)	For A1SJHCPU : A6WA-28P required	UL/cUL
		A1SNMCA-8KP	8 k steps, equipped with EPROM (directly)	For A1SJH/A1SHCPU : A6WA-28P required	
	E^2PROM	A1SMCA-2KE	2 k steps, equipped with E^2PROM (directly)	For A1SJHCPU Writing/reading directly from the peripheral device is possible	
		A1SMCA-8KE	8 k steps, equipped with E^2PROM (directly)		
		A1SNMCA-2KE	2 k steps, equipped with E^2PROM (directly)	For A1SJH/A1SHCPU Writing/reading directly from the peripheral device is possible	
		A1SNMCA-8KE	8 k steps, equipped with E^2PROM (directly)		
		A2SNMCA-30KE	14 k steps, equipped with E^2PROM (directly)	For A2SHCPU Writing/reading directly from the peripheral device is possible	
Memory write adapter		A6WA-28P	Used for memory cassette connector/EPROM 28-pin	For A1SMCA-8KP Used to partition ROM in A1SMCA-8KP	
Battery		A6BAT	IC-RAM battery backup	Mounted in A1SCPU/A2SCPU body	
Connector/terminal block conversion module		A6TBXY36	For sink type input module and sink type output module (standard type)	A1SX41(S2), A1SX42(S2), A1SY41, A1SY42, A1SH42, AX42(S1), AY42(S1/S3/S4), AH42	
		A6TBXY54	For sink type input module and sink type output module (2-wire type)		
		A6TBX70	For sink type input module (3-wire type)	A1SX41(S2), A1SX42(S2), A1SH42, AX42(S1), AH42	
		A6TBX36-E	For source type input module (standard type)	A1SX81(S2), AX82	
		A6TBY36-E	For source type output module (standard type)	A1SY81, AY82EP	
		A6TBX54-E	For source type input module (2-wire type)	A1SX81(S2), AX82	
		A6TBY54-E	For source type output module (2-wire type)	A1SY81, AY82EP	
		A6TBX70-E	For source type input module (3-wire type)	A1SX81(S2), AX82	
Cable for connector/terminal block conversion module		AC05TB	0.5 m (1.64 ft) for source module	A6TBXY36, A6TBXY54, A6TBX70	
		AC10TB	1 m (3.28 ft) for source module		
		AC20TB	2 m (6.56 ft) for source module		
		AC30TB	3 m (9.84 ft) for source module		
		AC50TB	5 m (16.4 ft) for source module		
		AC05TB-E	0.5 m (1.64 ft) for source module	A6TBX36-E, A6TBY36-E, A6TBX54-E, A6TBY54-E, A6TBX70-E	
		AC10TB-E	1 m (3.28 ft) for source module		
		AC20TB-E	2 m (6.56 ft) for source module		
		AC30TB-E	3 m (9.84 ft) for source module		
		AC50TB-E	5 m (16.4 ft) for source module		
Relay terminal module		A6TE2-16SR	For sink type output module	A1SY41, A1SY42, A1SH42, AY42, AY42-S1, AY42-S3, AY42-S4, AH42	
Cable for connecting relay terminal module		AC06TE	0.6 m (1.97 ft) long	A6TE2-16SR	
		AC10TE	1 m (3.28 ft) long		
		AC30TE	3 m (9.84 ft) long		
		AC50TE	5 m (16.4 ft) long		
		AC100TE	10 m (32.8 ft) long		
AnS I/O module and special module terminal block cover		A1STEC-S	Slim-type terminal block cover for the AnS I/O module and special module (terminal block connector type)	A1SX10, A1SX10EU, A1SX20, A1SX20EU, A1SX30, A1SX40 (S1/S2), A1SX80 (S1/S2), A1SY10, A1SY10EU, A1SY14EU, A1SY18A, A1SY18AEU, A1SY22, A1SY28A, A1SY28EU, A1SY40, A1SY50, A1SY60 (E), A1SY68A, A1SY80, A1SX48Y18, A1SX48Y58, A1SI61, A1S64AD, A1S62DA,A1S63ADA, A1S62RD3/4, A1SD61, A1SP60	

* : Class 2 power supply recognized by the UL/cUL Standard is required for 5-12-24 V DC modules.

REMARK

I/O cables with connectors for I/O modules with 40-pin connector specifications (A1SX41, A1SX42, A1SY41, A1SY42, etc.) or 37-pin D-sub connector specifications (A1SX81, A1SY81, A1SY81EP) are available.
Consult your nearest Mitsubishi representative for I/O cables with connectors.

(2) A[ ]NA[ ]A extension base unit

The following table shows the modules that can be loaded to the A[ ]NA [ ]A extension base units : A65B; A68B; A55B; or A58B.

For details on the specifications of each module see the appropriate module manual.

POINT

(1) All A[ ]NA[ ]A "building block type I/O modules" are compatible with the AnSHCPU.

Item	Model
Single-axis positioning module	AD70, AD70D
Positioning module	AD71, AD71S1, AD72
Position detection module	A61LS, A62LS
High speed counter module	AD61, AD61S1
A-D converter module	A68AD, A68ADS2, A616AD, A60MX, A60MXR, A68ADN
Temperature input module	A616TD, A60MXT
D-A converter module	A62DA, A62DAS1, A616DAI, A616DAV, A68DAV, A68DAI
A-D/D-A converter module	A84AD
CRT control/LCD control module	AD57, AD57S1, AD58
Graphic controller module	AD57G, AD57GS3
Memory card, parrallel interface module	AD59, AD59S1
Voice output module	A11VC
Computer link module	AJ71C24(S3/S6/S8), AJ71UC24
Intelligent communication module	AD51E, AD51ES3, AD51H(S3)
Terminal interface module	AJ71C21, AJ71C21S1
MELSECNET/MINI (S3) data link module	AJ71PT32, AJ71PT32-S3
Data link module	AJ71AP21, AJ71AR21, AJ71AT21B
SUMINET interface module	AJ71P41
Ethernet interface module	AJ71E71

Item	Model
Multidrop data link module	AJ71C22
Interrupt module	AI61
Power supply module	A61P, A62P, A63P, A65P, A66P, A67P, A68P, A61PEU, A62PEU
Extension base unite	A62B, A65B, A68B, A52B, A55B, A58B

(3) Peripheral devices

Item	Module	Remarks	
Plasma handy graphic programmer	A6PHP-SET	• A6PHP • SW[ ]GP-GPPAEE : A-series GPP function system disk • SW[ ]GP-GPPKEE : K-series GPP function system disk • SW0-GPPU : User disk (2DD) • AC30R4 : RS-422 cable (3 m (9.84 ft) long)	
Intelligent GPP	A6GPP-SET	• A6GPP • SW[ ]GP-HGPAEE : A-series GPP function system disk • SW[ ]GP-HGPKEE : K-series GPP function system disk • SW0-GPPU : User disk (2DD) • AC30R4 : RS-422 cable (3 m (9.84 ft) long)	
Composite video cable	AC10MD	• Connects A6GPP and monitor display. (1 m (3.28 ft) long)	
RS-422 cable	AC30R4	3 m (9.84 ft) long	Connects CPU and A6GPP/A6PHP.
	AC300R4	30 m (98.4 ft) long	
User disk	SW0-GPPU	2DD	Used for storing user program (3.5 in., formatted)
	SW0S-USER	2HD	
Cleaning disk	SW0-FDC	Applicable to A6GPP/A6PHP	Used for cleaning disk drive.
Programming module	A7PU	• Connected directly to the CPU with an RS-422 cable (AC30R4, AC300R4) to read and write programs. Provided with an MT function. • The product package includes a cable used for connection to an audio cassette recorder.	
	A7PUS	Connected directly to the CPU with an RS-422 cable (AC30R4-PUS) to read and write programs.	
	A8PUE	Connected directly to the CPU with an RS-422 cable (AC30R4-PUS, AC20R4-A8PU) to read and write programs.	
RS-422 cable	AC30R4, AC300R4,	Used to connect an A7PU to the CPU. Long : 3 m/30 m (9.84 ft./98.4 ft.)	
	AC30R4-PUS	Used to connect an A7PUS or A8PUE to the CPU. Long : 3 m (9.84 ft.)	
	AC20R4-A8PU	Used to connect an A8PUE to the CPU. Long : 2 m (6.56 ft.)	
P-ROM writer module	A6WU	• Used for writing a program in the CPU/A6PHP to ROM, or for reading a CPU program from ROM. • Connected to CPU/A6PHP using an AC30R4/AC03WU cable.	
RS-422 cable	AC30R4, AC300R4	Connects CPU and A6WU. 3 m/30 m (9.84 ft/98.4 ft) long	
	AC03WU	Connects A6PHP and A6WU. 0.3 m (0.98 ft) long	

POINTS

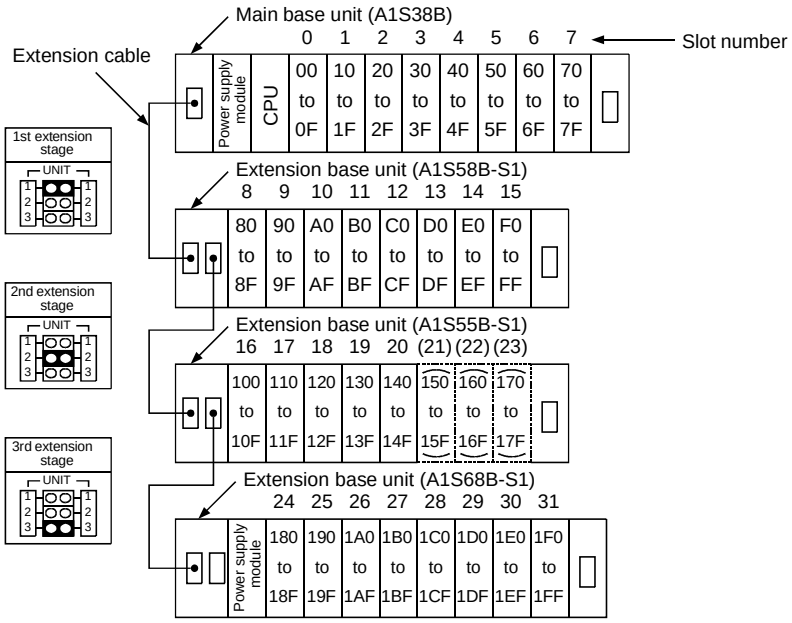
(1) Programming devices compatible with A1SHCPU
A6WU P-ROM writer module cannot be used.
All programming devices compatible with A1SHCPU can be used, excluding A6WU.
(When A7PU, A7PUS, A8PU or A8PUE is used, the CPU type "A3" is displayed when started up.)

(2) Software packages compatible with A1SHCPU
All utility packages compatible with A1SHCPU can be used.

2.4 General Description of System Configuration

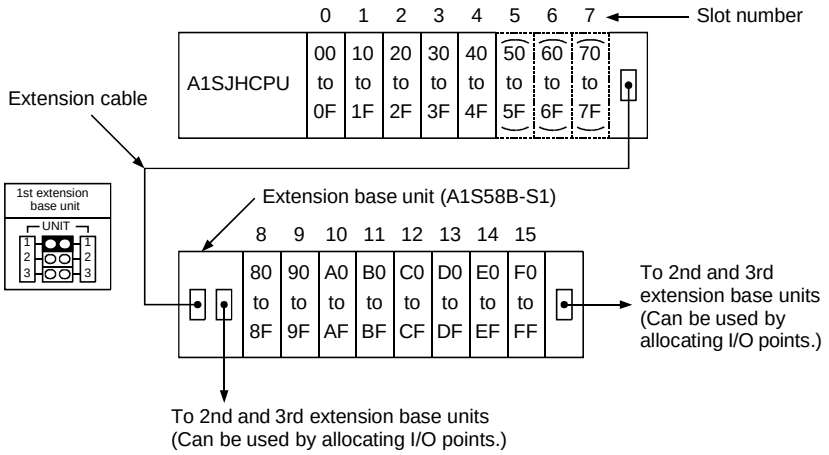
2.4.1 AnSHCPU

The following gives the system configuration, number of inputs/outputs, I/O number allocation, etc. when the AnSHCPU is used as an independent system.

System configuration	
Maximum number of extension stages	Three
Maximum number of input/output points	A1SHCPU : 256 points, A2SHCPU : 512 points, A2SHCPU-S1 : 1024 points
Main base units	A1S32B, A1S33B, A1S35B, A1S38B
Extension base units	A1S52B(S1), A1S55B(S1), A1S58B(S1), A1S65B(S1), A1S68B(S1), A52B, A55B, A58B, A62B, A65B, A68B
Extension cables	A1SC01B, A1SC03B, A1SC07B, A1SC12B, A1SC30B, A1SC60B, AC06B, AC12B, AC30B, A1SC05NB, A1SC07NB
Notes	(1) Only the 1st extension base unit can be used when extension base units of types other than the AnS S1 are equipped. (The S1 type and other types must not be used together.) (2) To use the AnS S1 type extension base unit with an A[ ]N or A[ ]A type, the latter must be equipped with the last extension base unit. (The A[ ]N or A[ ]A extension base unit cannot be connected to the AnS S1 type.) (3) When an A1S52B (S1), A1S55B (S1), A1S58B (S1), A52B, A55B, or A58B is used, a voltage of 5 V DC is supplied from the power supply module. See Section 7.1.3, and consider the application. (4) The extension cable should be used for distances of up to 6 m (19.68 ft.). (5) The extension cable must not be bundled with or laid near the main circuit (high voltage, high current) lines.
I/O number allocation	(1) Allocate I/O numbers to the extension base units in order of extension base unit number, not in extension cable connection order. (2) I/O numbers are allocated on the assumption that both the main base unit and the extension base units have eight slots. Sixteen input/output points will be allocated to each slot indicated by dotted lines in the above system configuration figure. (3) Allocate 16 input/output points to empty slots. (4) If the setting of an extension base unit has been omitted, make the allocation on the assumption that each of the eight slots of the relevant base unit occupies 16 input/output points. (5) Items (2) to (4) can be changed by performing "I/O allocation". For details, see the ACPU Programming Manual (Fundamentals).

2.4.2 A1SJHCPU

This section describes the system configuration, numbers of I/O points, I/O allocations, etc., for a stand-alone A1SJHCPU system.

System configuration	 *In this example, a 16-point module is installed at each slot.
Maximum number of extension stages	Three
Maximum number of input/output points	256
Extension base units	A1S52B(S1), A1S55B(S1), A1S58B(S1), A1S65B(S1), A1S68B(S1), A52B, A55B, A58B, A62B, A65B, A68B
Extension cables	A1SC03B, A1SC07B, A1SC12B, A1SC30B, A1SC60B, A1SC01B, AC06B, AC12B, AC30B, A1SC05NB, A1SC07NB
Notes	(1) If using a type of extension base unit for A1S use other than the S1 type,, only one extension base unit can be installed. (Combined use of S1 type extension base units and extension base units other than the S1 type is not possible.) (2) When using one or more S1 type extension base units for A1S use in combination with one or more extension base units for A[ ]N or A[ ]A use, the final extension base unit must be one for A[ ]N or A[ ]A use. (An S1 type extension base for A1S use can not be connected from an extension base for A[ ]N or A[ ]A use.) (3) Extension base units A1S52B(S1), A1S55B(S1), A1S58B(S1), A52B, A55B, A58B are supplied with a 5 V DC power supply from the power supply module on the main base unit; see Section 7.1.3 to determine whether or not these extension base units can be used. (4) The total length of extension cable used must not exceed 6 m (19.68 ft.).
I/O number allocation	(1) I/O numbers are allocated in the order of the numbers set in extension base number setting, regardless of the order of connection of extension cables. (2) When allocating I/O points, all main bases and extension bases are regarded as having 8 slots of I/O points. Accordingly, 16 points per slot are allocated to the part of the system configuration drawing indicated using dotted lines. (3) 16 points are allocated to vacant slots. (4) If extension base number setting has not been performed at one or more modules, I/O points are allocated by regarding each slot in the total number of slots involved-obtained by multiplying the number of extension bases for which setting was skipped by 8 slots-as occupying 16 points per slot. (5) The allocations in (2) to (4) above can be changed by performing "I/O allocation". When using two or three extension base units, perform "I/O allocation" to allocate 0 points to vacant slots of the A1SJCPU and some slots of the first extension base unit, and allocate I/O points to the second and third extension base units. (The total number of I/O points for the A1SJCPU and 1st, 2nd, and 3rd extension base units is 256.) For details on "I/O allocation", see the ACPU Programming Manual(Fundamentals).

3. SPECIFICATIONS

Table 3.1 General specification

Item	Specifications					
Ambient operating temperature	0 to 50 °C					
Ambient storage temperature	-20 to 75 °C					
Ambient operating humidity	10 to 90 % RH, No-condensing					
Ambient storage humidity	10 to 90 % RH, No-condensing					
Vibration resistance	Conforming to JIS B 6501, IEC 1131-2		Frequency	Acceleration	Amplitude	No. of sweeps
		Under intermittent vibration	10 to 57 Hz	—	0.075 mm (0.003 in.)	10 times each in X, Y, Z directions (for 80 min.)
			57 to 150 Hz	9.8 m/s^2{1 G}	—	
		Under continuous vibration	10 to 57 Hz	—	00.35 mm (0.001 in.)	
			57 to 150 Hz	4.9 m/s^2{1 G}	—	
Shock resistance	Conforming to JIS B 3501, IEC 1131-2 (147 m/s^2 {15G}, 3 times in each of 3 directions X Y Z)					
Operating ambience	No corrosive gases					
Operating elevation	2000 m (6562 ft.) max.					
Installation location	Control panel					
Over voltage category *1	II max.					
Pollution level *2	2 max.					

*1 : This indicates the section of the power supply to which the equipment is assumed to be connected between the public electrical power distribution network and the machinery within premises. Category II applies to equipment for which electrical power is supplied from fixed facilities. The surge voltage withstand level for up to the rated voltage of 300 V is 2500 V.

*2 : This index indicates the degree to which conductive material is generated in terms of the environment in which the equipment is used. Pollution level 2 is when only non-conductive pollution occurs. A temporary conductivity caused by condensing must be expected occasionally.

IMPORTANT

Restrictions for UL standard approved products

In order to be recognized as UL listed products, products must be used in compliance with the following restrictions :

(1) Operating ambient temperature is limited to 0 to 50 °C.

(2) A class 2 power supply recognized by the UL standard must be used.

4. AnSHCPU

4.1 Performance Specifications

The memory capacities of AnSHCPU modules, performances of devices, etc., are presented below.

Table 4.1 Performance specifications

Item \ Type		A1SJHCPU	A1SHCPU	A2SHCPU(S1)
Control system		Repeated operation (using stored program)		
I/O control method		Refresh mode/Direct mode selectable		
Programming language		Language dedicated to sequence control. Relay symbol type and logic symbolic language, MELSAP-II(SFC)		
Number of instructions (types)		Sequence instructions : 26		
		Basic instructions : 131		
		Application instructions : 106		
		CC-Link dedicated instructions : 11		
Processing speed (sequence instruction) (μ sec/step)		Direct : 1.0 to 2.3 Refresh : 1.0		
I/O points		2048 *1		
Actual I/O number of point		512	512	A2SH : 512, A2SH-S1 : 1024
Watchdog timer (WDT) (msec)		10 to 2000		
Memory capacity *2 (built-in RAM)		64 k bytes		A2SH : 64 k bytes, A2SH-S1 : 192 k bytes
Program capacity	Main sequence	Max. 8 k steps		A2SH : Max. 14 k steps, A2SH-S1 : Max. 30 k steps
	Sub sequence	Unavailable		
Internal relay (M) (points)		100 (M0 to 999)	The number of M + L + S = 2048 (set in parameters)	
Latch relay (L) (points)		1048 (L1000 to 2047)		
Number of step relays (S) (points)		0 (Defaults to no value)		
Link relay (B) (points)		1024 (B0 to 3FF)		
Timer (T)		256 points 100 msec timer : Setting time 0.1 to 3276.7 sec (T0 to 199) 10 msec timer : Setting timer 0.01 to 327.67 sec (T200 to 255) 100 msec : Depending on setting Retentive timer : (Setting time 0.1 to 3276.7 sec)		Set in parameters
Counter (C)		256 points Normal counter : Setting range 1 to 32767 (C0 to 255) Interrupt program counter : Setting range 1 to 32767 Counter to be used in interrupt program		Set in parameters
Data register (D) (points)		1024 (D0 to D1023)		
Link register (W) (points)		1024 (W0 to W3FF)		
Annunciator (F) (points)		256 (F0 to F255)		
File register (R) (points)		Max. 8191 (R0 to R8191)		
Accumulator (A) (points)		2 (A0, A1)		

Table 4.1 Performance specifications (Continued)

Item \ Type	A1SJHCPU	A1SHCPU	A2SHCPU(S1)
Index register (V, Z) (points)	2 (V, Z)		
Pointer (P) (points)	256 (P0 to P255)		
Interrupt pointer (I) (points)	32 (I0 to I31)		
Special relay (M) (points)	256 (M9000 to M9255)		
Special register (D) (points)	256 (D9000 to D9255)		
Comment (points) (Specify in batches of 64 points)	Max. 3648		
Self-diagnostic functions	Watchdog error monitor, Memory error detection, CPU error detection, I/O error detection, Battery error detection, etc.		
Operation mode at the time of error	STOP/CONTINUE		
STOP → RUN output mode	Output data at time of STOP restored/data output after operation execution		
Clock function	Year, month, day, hour, minute, second (Automatically recognizes leap years.) Accuracy -3.1 to +5.3 s (TYP. +1.7 s)/d at 0 °C -1.6 to +5.3 s (TYP. +2.4 s)/d at 25 °C -9.6 to +3.6 s (TYP. -2.1 s)/d at 55 °C		
Allowable momentary power interruption time	20 msec		
Current consumption (5 V DC)	0.3 A	0.3 A	0.4 A
Weight [kg (lb.)]	1.00 (2.20)	0.33 (0.73)	0.33 (0.73)
Standard	UL/cUL	—	UL/cUL

*1 The I/O device after the actual input points can be used as MELSECNET(/B), MELSECNET/MINI, or C.C-Link.

*2 The maximum total memory that can be used for parameters, T/C set values, program capacity, file registers, number of comments, sampling trace, and status latch is 32 k/64 k bytes. The memory capacity is fixed. No expansion memory is available. Section 4.1.7 shows how to calculate the memory capacity.

4.1.1 AnSHCPU operation processing

This section explains the operation processing which takes place from the time the AnSHCPU power is switched ON until the sequence program is executed. AnSHCPU processing is generally divided into the following four types:

(1) Initial processing

This is the pre-processing for executing sequence operations. Initial processing is executed once at power up or after key reset.

(a) Resetting the I/O module.

(b) Initialization of the data memory's unset latch area (bit devices turned OFF, word devices set to 0).

(c) I/O module addresses are automatically assigned in accordance with the I/O module type and where the module is installed on a base unit.

(d) Automatic diagnostic check of parameter settings and operation circuits is executed (see Section 4.1.6).

(e) If the AnSHCPU is used in the master station of an MELSECNET(II) MELSECNET/B, data link operation begins after setting the link parameter data in the data link module.

(2) I/O module refresh processing

If the refresh mode for both input and output is set with the I/O control switch, the I/O module is refreshed (see Section 4.1.5).

(3) Sequence program operation processing

The sequence program written in the AnSHCPU is executed from step 0 to the END instruction.

(4) END processing

When sequence program processing reaches the END instruction, the sequence program is returned to step 0.

(a) Self-diagnosis checks for blown fuses, I/O module verification, low battery voltage, etc., are executed (see Section 4.1.6).

(b) T/C present values are updated and contacts are turned ON/OFF. (The ACPU Programming Manual (Fundmentals) gives details.)

(c) Data read or write from/to computer link modules (A1SJ71(U)C24, AJ71C24(S8), AD51(S3), etc.)

(d) Link refresh processing is executed when the link refresh request is given from the MELSECNET data link.

Note that the AnSHCPU can enable and disable execution of link refresh by turning M9053 ON/OFF and by issuing DI/EI instructions.

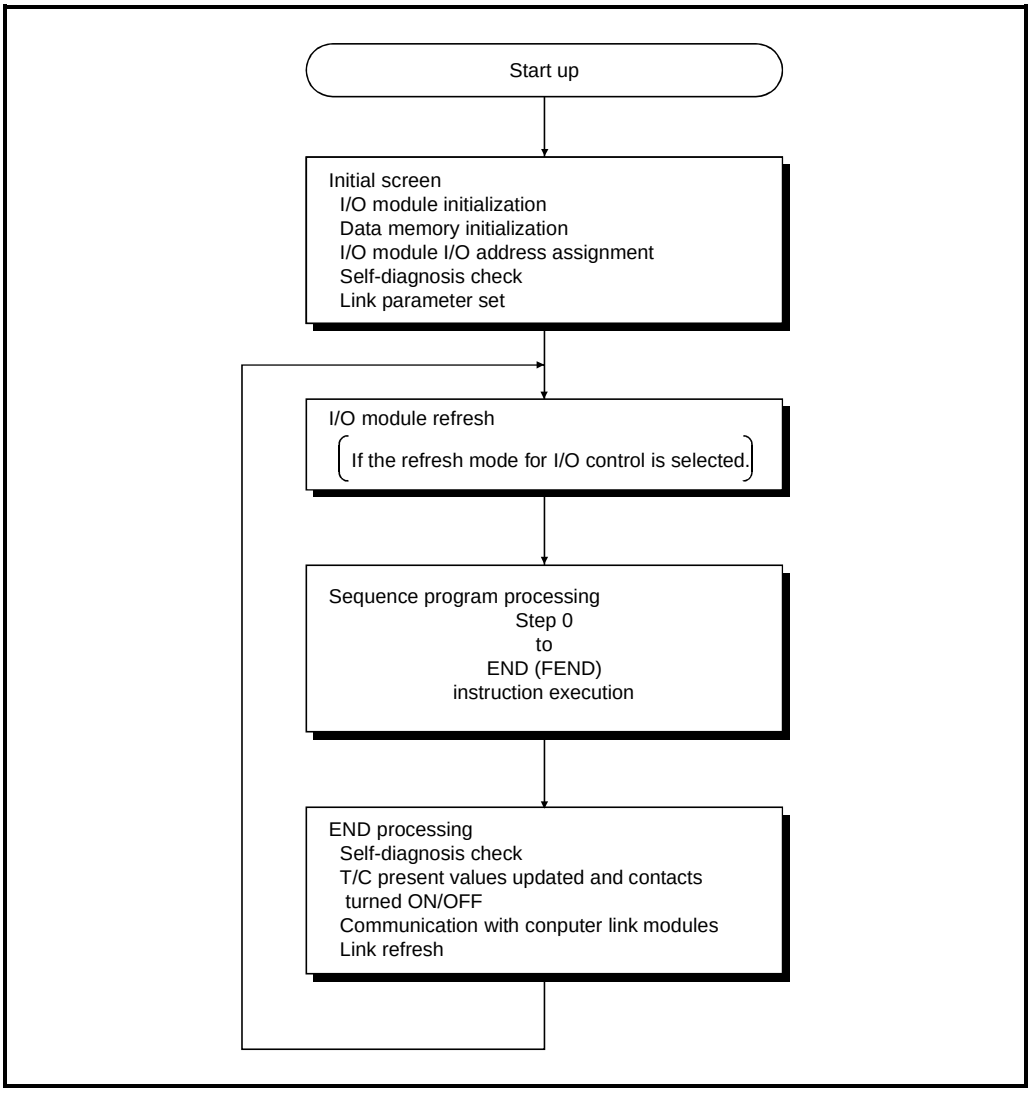


Fig.4.1 AnSHCPU operation processing

4.1.2 Operation processing in the RUN, STOP, PAUSE status

The PC CPU can be operated in the RUN, STOP and PAUSE status as described below.

(1) RUN operation

RUN indicates repeated operations of the sequence program from step 0 to the END (FEND) instruction.

When a CPU changes its status to the RUN mode, the CPU restores all output data which was saved when the CPU was stopped, in accordance with the STOP → RUN mode set in the parameters.

The PC CPU needs initialization time before starting a sequence program operation. It requires two to three seconds after a power ON or reset, and one to three seconds after the mode is changed from STOP to RUN.

(2) STOP operation

STOP indicates stopping of sequence program operation by executing a STOP instruction or by using the remote STOP function (see Section 4.2.3).

When the CPU is set to STOP, the output status is saved and all outputs are switched OFF. Data other than the outputs (Y) is retained.

(3) PAUSE operation

PAUSE indicates stopping of sequence program operation with the output and data memory status retained.

POINT

An AnSHCPU executes the following operations at any time in the RUN, STOP or PAUSE mode :

- Refresh processing of the I/O module when the refresh mode is set.
- Data communications with computer link modules.
- Link refresh processing.

Therefore, the following operations are possible even when the AnSHCPU is in the STOP or PAUSE status :

- Monitoring I/O status and testing using a peripheral device.
- Read/write with computer link modules.
- Communications with other stations in the MELSECNET data link system.

4.1.3 Watchdog timer (WDT)

The watchdog timer is an internal system timer which monitors the scan time of sequence program execution to detect program errors. The WDT also detects PC hardware faults.

The default value for the watchdog timer is 200 msec. This value can be changed from 10 to 2000 msec in the parameters.

(1) Normal operation (scan time is within the set value)

The watchdog timer is reset after the execution of an END instruction.

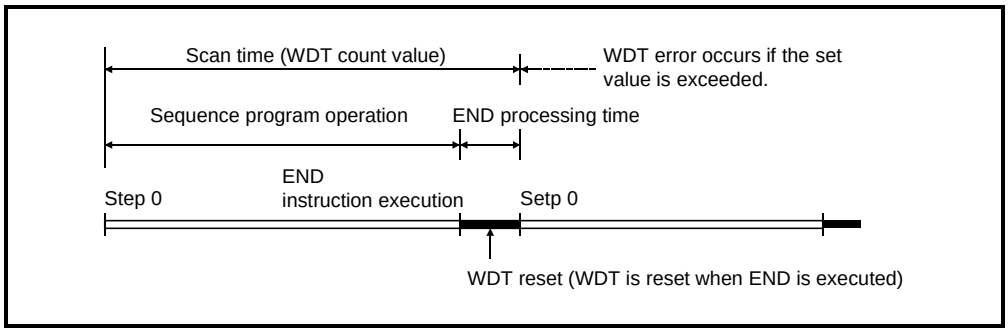
(2) Faulty operation (scan time is not within the set value)

(a) A watchdog timer is detected, then, the CPU stops program processing and flashes the RUN LED on its front face.

(b) There are two types of error code for the watchdog timer, error codes "22" and "25".

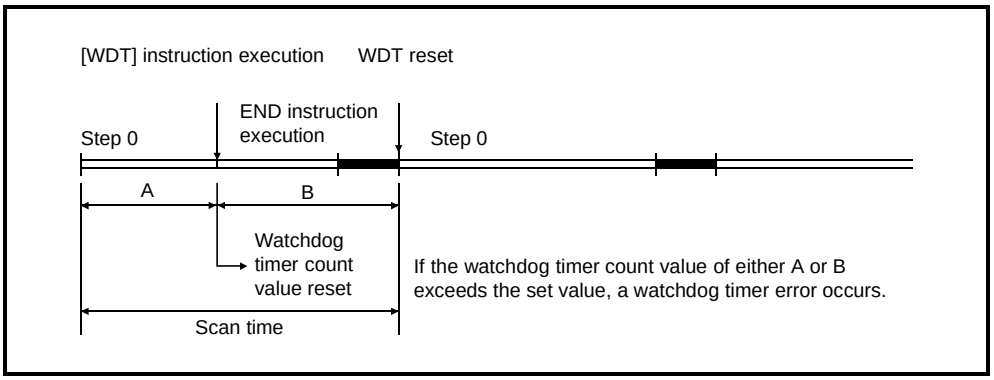
Error code 22 signifies that an END instruction is executed after the WDT has exceeded its set value.

Error code 25 signifies that the CPU is executing a dead-loop program and never reaches an END instruction. This error could occur if the PC hardware is faulty or branch instructions are used incorrectly in the program.



(3) Watchdog timer reset using the sequence program

The watchdog timer is reset with a [WDT] instruction in the sequence program.
The watchdog timer begins counting again from 0.
However, the scan time values registered in D9017 to D9019 are not reset when the WDT instruction is executed.



(4) When a watchdog timer error occurs, check the error by seeing Chapter 11 (Troubleshooting), then turn the RESET switch to clear the error.

4.1.4 Operation processing when a momentary power interruption occurs

When voltage supplied to the power supply module is below the specified range, the AnSHCPU detects a momentary power interruption.

When the AnSHCPU detects a momentary power interruption, the following operations are executed :

(1) Momentary power interruption within 20 msec

(a) Program processing is stopped and the output is retained.

(b) Program processing is resumed when the power is restored.

(c) The watchdog timer (WDT) continues counting even while the operation is stopped.
For example, if a momentary power interrutption of 20 msec occurs when the scan time is 190 msec, a watchdog timer error (200 msec) occurs.

(2) Momentary power interruption over 20 msec

The AnSHCPU is reset and returns to the initial start status. The necessary operations are the same as when the CPU power is turned ON or when the CPU is reset.

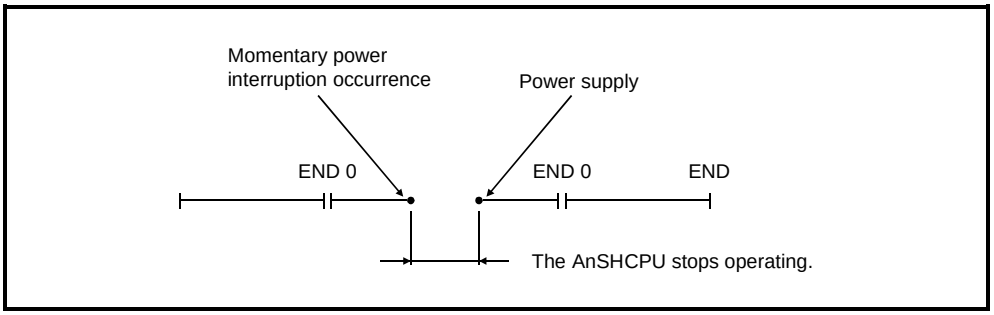


Fig. 4.2 Operation processing when a momentary power interruption occurs

4.1.5 I/O control method

The I/O control method for the AnSHCPU can be selected as either of the following two modes using the I/O control switch :

(1) Direct mode for both input and output

(2) Refresh mode for both input and output

The direct and refresh modes are explained below. Processing in the direct and refresh modes differs only for inputs (X) and outputs (Y). Processing for other devices and for special function modules (FROM/TO instruction) is the same in both modes.

(1) Direct mode

I/O modules are accessed whenever a CPU executes an instruction with an input (X) or output (Y).
One scan time at most is necessary from the input status change to the change in the output status which corresponds to the input.

(2) Refresh mode

I/O modules are batch accessed before executing step 0 of the sequence program.
This is called I/O module refresh processing. Input module status are read to the data memory input (X). Data memory output (Y) status are output to output modules.
When a CPU executes an instruction with an input (X) or output (Y), it only accesses the data memory of the input (X) or output (Y).Two scan times at most is necessary from the input status change to the output status change which corresponds to the input.

POINT

When the refresh mode has been selected, use the SEG instruction when accessing one segment of an I/O module in the same way as with the direct mode. The ACPU Programming Manual (Common Instructions) gives details.

4.1.6 Self-diagnosis

The self-diagnosis function allows the AnSHCPU to detect its own errors.

Self-diagnosis is carried out when the PC power supply is turned ON and if an error occurs while the PC is in the RUN status. If the AnSHCPU detects an error, it displays an error message and stops to prevent faulty PC operation.

The operation of the AnSHCPU when an error is detected by the self-diagnosis function can be selected as either stop mode or continuous mode by making a parameter setting. In the stop mode, PC operation is stopped when the error is detected; in the continuous mode, PC operation is continued.

When an error occurs, the error occurrence and the error content are stored in a special relay (M) and special register (D). In the continuous mode, in particular, the program should read the details of the error and take appropriate action to prevent faulty PC and machine operations.

Operation stops and all outputs (Y) are immediately turned OFF after the self-diagnosis function detects an error which stops PC operation.

If the self-diagnosis function detects an error during which PC operation continues, the part of the program where the error was detected is skipped and the rest of the program is executed.

If an I/O module verify error is detected, the operation is continued with the I/O addresses at the time the error occurred.

Explanations of the errors detected by the self-diagnosis function are given in Table 4.2.

REMARKS

(1) In Table 4.2, in the I/O error, I/O module verify, fuse blown, special function module error, and operation check error diagnoses, the CPU status can be selected as either stop or run; and the RUN LED status as either flashing or ON by using peripheral devices.

(2) The LED Display Message column in Table 4.2 lists messages displayed by the peripheral devices' PC diagnosis.

Table 4.2 Self-diagnosis

Diagnosis	Diagnosis timing	CPU status	"RUN" LED status	LED display message
Memory error Instruction code check	When the corresponding instruction is executed	Stop	Flashing	INSTRUCT. CODE ERR.
Parameter setting check	When power is switched ON or a reset is executed When switched from STOP/PAUSE to RUN			PARAMETER ERROR
No END instruction	When M9056 or M9057 is switched ON When switched from STOP/PAUSE to RUN			MISSING END INS.
Instruction execution disable	When CJ, SCJ, JMP, CALL(P), FOR and NEXT instruction is executed When switched from STOP/PAUSE to RUN			CAN'T EXECUTE (P)
Format (CHK instruction) check	When switched from STOP/PAUSE to RUN			CHK FORMAT ERR.
Instruction execution disable	When an interrupt occurs When switched from STOP/PAUSE to RUN			CAN'T EXECUTE (I)
CPU error RAM check	When power is switched ON or a reset is executed When M9084 is switched ON during STOP	Stop	Flashing	RAM ERROR
Operation circuit check	When power is switched ON or a reset is executed			OPE. CIRCUIT ERR.
Watchdog error check	When an END instruction is executed			WDT ERROR
END instruction not executed	When program processing reaches the end of the program			END NOT EXECUTE
Endless loop execution	At any time			WDT ERROR
I/O error I/O module verify	When an END instruction is executed (Not checked when M9084 is ON)	Stop / Run	Flash-ing / ON	UNIT VERIFY ERR.
Fuse blown	When an END instruction is executed (Not checked when M9084 is ON)			FUSE BREAK OFF.
Special function module error Control bus check	When a FROM, TO instruction is executed	Stop	Flashing	CONTROL-BUS ERR.
Special function module error	When a FROM, TO instruction is executed			SP. UNIT DOWN
Link module error	When power is switched ON or a reset is executed When switched from STOP/PAUSE to RUN			LINK UNIT ERROR
I/O interruption error	When an interruption occurs			I/O INT. ERROR
Special function module assignment	When power is switched ON or a reset is executed When switched from STOP/PAUSE to RUN			SP. UNIT LAY. ERR.
Special function module error	When a FROM, TO instruction is executed	Stop / Run	Flash-ing / ON	SP. UNIT ERROR
Link parameter error	When power is switched ON or a reset is executed When switched from STOP/PAUSE to RUN	Run	ON	LINK PARA. ERROR
Battery error Battery low	At any time (not checked When M9084 is ON)	Run	ON	BATTERY ERROR
Operation check error	When the corresponding instruction is executed	Stop / Run	Flash-ing / ON	OPERATION ERROR

4.1.7 Devices

A device is any contact, coil, or timer used in PC program operations.

AnSHCPU devices and their range of use are shown below. The items marked "*" can be used and set for range change by setting the parameters.

Set parameters which are appropriate for the system configuration and its program. Section 4.1.6 gives details about parameter settings.

Table 4.3 Devices

Device		Application range (Number of points)		Explanation
X	Input	A1SHCPU : X/Y00 to X/YFF (X, Y total 256 points) A2SHCPU : X/Y000 to X/Y1FF (X, Y total 512 points) A2SHCPU-S1 : X/Y0 to X/Y3FF (X, Y total 1024 points)		Provides a command or data from an external device, (e.g. pushbutton, select switch, limit switch, digital switch) to the PC.
Y	Output			Provides the program control result to an external device, e.g. solenoid, magnetic switch, signal light, digital display.
M	Special relay	M9000 to M9255 (256 points)		Predefined internal relay for special purposes.
M	Internal relay *	M0 to M999 (1000 points)	Number of M + L + S = 2048	Internal relay in the PC which cannot be directly output.
L	Latch relay*	L1000 to L2047 (1048 points)		Internal relay in the PC which cannot be directly output. Backed up during power failure.
S	Step relay*	Can be used by setting a parameter (0)		Used in the same manner as an internal relay (M) e.g., as a relay indicating the stage number of a step-by step process operation program.
B	Link relay	B0 to B3FF (1024 points)		Internal relay for MELSECNET which cannot be output. May be used as an internal relay if not assigned for data link use.
F	Annunciator	F0 to F255 (256 points)		Used to detect a fault. When switched ON during RUN by a fault detection program, it stores a corresponding number in a special register D.
T	100 msec timer*	T0 to T199 (200 points)		Forward timers are available in 100 msec, 10 msec and 100 msec retentive types.
T	10 msec timer*	T200 to T255 (56 points)		
T	100 msec retentive timer*	Can be used by setting a parameter (0 points)		
C	Counter*	C0 to C255 (256 points)		Forward counters are available in normal and interrupt types.
C	Interrupt counter*	Can be used by setting a parameter (0 points)		
D	Data register	D0 to D1023 (1024 points)		Memory for storing values.
D	Special register	D9000 to D9255 (256 points)		Predefined data memory for special purposes.
W	Link register	W0 to W3FF (1024 points)		Data register for MELSECNET. May be used as a data register if not assigned for MELSECNET use.
R	File register*	Can be used by setting a parameter (0 points)		Extends the data register utilizing the user memory area.
A	Accumulator	A0, A1 (2 points)		Data register for storing the operation results of basic and application instructions.
Z	Index register	Z (1 point)		Used to index device numbers (X, Y, M, L, B, F, T, C, D, W, R, K, H, P).
V	Index register	V (1 point)		
N	Nesting	N0 to N7 (8 levels)		Indicates the nesting of master controls.

Table 4.3 Devices (Continued)

Device		Application range (Number of points)	Explanation
P	Pointer	P0 to P255 (256 points)	Indicates the destination of branch instructions (CJ, SCJ, CALL, JMP).
I	Pointer for interruption	I0 to I31 (32 points)	Indicates an interrupt program corresponding to the interrupt source.
K	Decimal constant	K-32768 to 32767 (16-bit instruction) K-2147483648 to 2147483647 (32-bit instruction)	Used to specify the timer/counter set value, pointer number, interrupt pointer number, the number of bit device digits, and basic and application instruction values.
H	Hexadecimal constant	H0 to FFFF (16-bit instruction) H0 to FFFFFFFF (32-bit instruction)	Used to specify the basic and application instruction values.

REMARK

The step relay (S) may be used in the same manner as the internal relay (M). The step relay is useful when writing a program which has two functions or applications, i.e., the step relay can be used specifically in accordance with the function or application, independently of the internal relay.

4.1.8 Parameter setting ranges

The parameters specify various PC functions, device ranges and user memory assignments of the AnSHCPU.

As shown in Table 4.4, the parameters have default settings so the user does not have to set all the parameter items. If any parameter item needs to be modified, please refer to the table for the allowed setting range.

The operating manuals for each peripheral device give details on parameter settings.

Table 4.4 Parameter setting ranges

Item \ Setting		Default value	Setting range	Valid peripheral devices	
				PU	GPP
Main sequence program area	A1SHCPU	6 k steps	1 to 8 k steps (in units of 1 k steps)	ϒ	ϒ
	A2SHCPU(S1)		1 to 14 k steps (in units of 1 k steps)	ϒ	ϒ
File register capacity		None	1 to 4 k points (in units of 1 k points)	ϒ	ϒ
Comment capacity	A1SHCPU	None	0 to 3648 points (in units of 64 points)	—	ϒ
	A2SHCPU(S1)		0 to 3648 points (in units of 64 points)		
Status latch	Memory capacity	None	0/8 to 16 k bytes	—	ϒ
	Data memory		Absent/present		
	File register		Absent/present (2 to 8 k bytes)		
Sampling trace	Memory capacity	None	0/8 k bytes	—	ϒ
	Device setting		Device number		
	Execution condition		Per scan		
			Per time		
	Sampling count		0 to 1024 times (in units of 129 times)		
Microcomputer program	A1SHCPU	None	0 to 14 k bytes (in units of 2 k bytes)	—	ϒ
	A2SHCPU (S1)		0 to 26 k bytes (in units of 2 k bytes)		
Setting of latch (power interruption compensation) range	Link relay (B)	Only for L1000 to L2047. None for others	B0 to B3FF (in units of 1 point)	ϒ	ϒ
	Timer (T)		T0 to T255 (in units of 1 point)		
	Counter (C)		C0 to C255 (in units of 1 point)		
	Data register (D)		D0 to D1023 (in units of 1 point)		
	Link register (W)		W0 to W3FF (in units of 1 point)		
Setting of link range	Number of link stations	None	1 to 64	—	ϒ
	Input (X) A1SHCPU		X0 to FF (in units of 16 points)		

Table 4.4 Parameter setting ranges (Continued)

Item \ Setting			Default value	Setting range	Valid peripheral devices	
					PU	GPP
Setting of link range	Input (X)	A2SHCPU	None	X0 to 1FF (in units of 16 points)	—	ϒ
		A2SHCPU-S1		X0 to 3FF (in units of 16 points)		
	Output (Y)	A1SHCPU		Y0 to FF (in units of 16 points)		
		A2SHCPU		Y0 to 1FF (in units of 16 points)		
		A2SHCPU-S1		Y0 to 3FF (in units of 16 points)		
	Link relay (B)			B0 to B3FF (in units of 16 points)		
	Link register (W)			W0 to W3FF (in units of 1 point)		
I/O assignment			None	X/Y0 to X/Y1FF (in units of 16 points)	—	ϒ
Setting of internal relay (M), latch relay (L), and step relay (S) setting			M0 to M999 L1000 to L2047 None for S	M/L/S 0 to 2047 (M, L, S are serial numbers)	ϒ	ϒ
Watchdog timer setting			200 msec	10 msec to 2000 msec (in units of 10 msec)	ϒ	ϒ
Setting of timer			100 msec : T0 to T199 10 msec : T200 to T255	256 points of 100 msec, 10 msec, and integrating timers (in units of 8 points). Timers have serial numbers.	ϒ	ϒ
Setting of counter			No interrupt counter	256 points (in units of 8 points) for counters and interrupt counters. Must be consecutive numbers.	—	ϒ
Setting of remote RUN/PAUSE contact *		A1SHCPU	None	X0 to XFF	—	ϒ
		A2SHCPU		X0 to X1FF		
		A2SHCPU-S1		X0 to X3FF		
Operation mode at the time of error	Fuse blown		Continuation	Stop/continuation	—	ϒ
	I/O verify error		Stop			
	Operation error		Continuation			
	Special function module check error		Stop			
STOP → RUN display mode			Operation status prior to re-output of STOP	Output before STOP or after operation execution	—	ϒ
Print title entry			None	Up to 128 characters	—	ϒ
Keyword entry			None	Max. 6 digits in hexadecimal (0 to 9, A to F)	ϒ	ϒ

* It is not possible to set a PAUSE contact alone.

4.1.9 Memory capacity settings (main programs, file registers, comments, etc.)

The A1SHCPU, A2SHCPU(S1) provides 64 k (192 k) bytes of user memory area (RAM).
Data for parameters, T/C set values, main programs, sampling trace, status latch, file registers, and comments can be stored in the user memory area.

(1) Calculating memory capacity

The user memory can be divided into several memory blocks in accordance with the parameter settings.

Table 4.5 Parameter settings and memory capacity

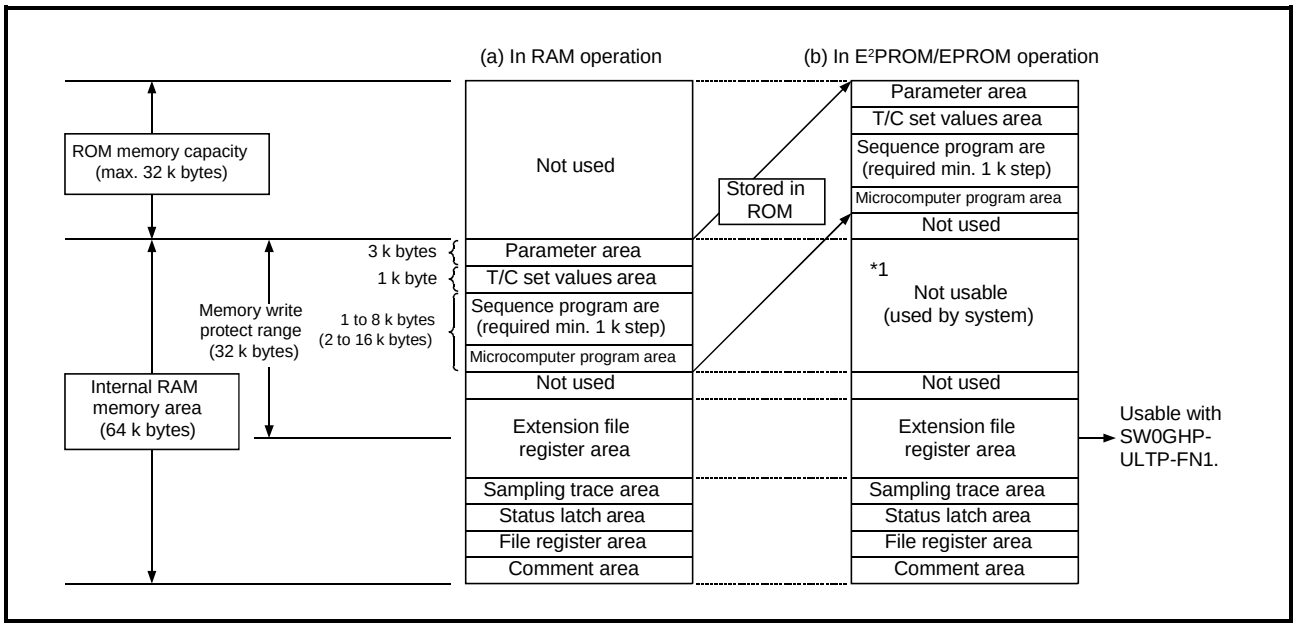
Item		Setting module	Memory capacity	Storage onto ROM	Remark
Main program	Parameter, T/C set values	—	4 k bytes (fixed)	Possible	Occupies 4 k bytes for parameters and T/C set values
	Sequence program	1 k steps	(Main sequence program capacity) × 2 k bytes		
	Microcomputer program	2 k bytes	(Main micro computer program capacity) ×1 k byte		
Sampling trace		Not available/ available	0/8 k bytes	Impossible	
Status latch	Data memory	Not available/ available	0/8 k bytes		The memory capacity for the file register status latch is determined by the number of file register points set using parameters.
	File registers	Not available/ available	(File registers' memory capacity) 1 k byte		
File registers		1 k points	(File registers' number of points) × 2 k bytes		
Comments		64 points	$\frac{\text{(Number of comments)}}{64}$ + 1 k byte		1 k byte is occupied by the system when setting comment capacity.

(2) Storage priority in user memory

The data set in the parameters is stored in the following sequence.
Make sure that the memory protect range does not cover the areas, such as sampling trace and file register, to which data will be written during sequence program execution.

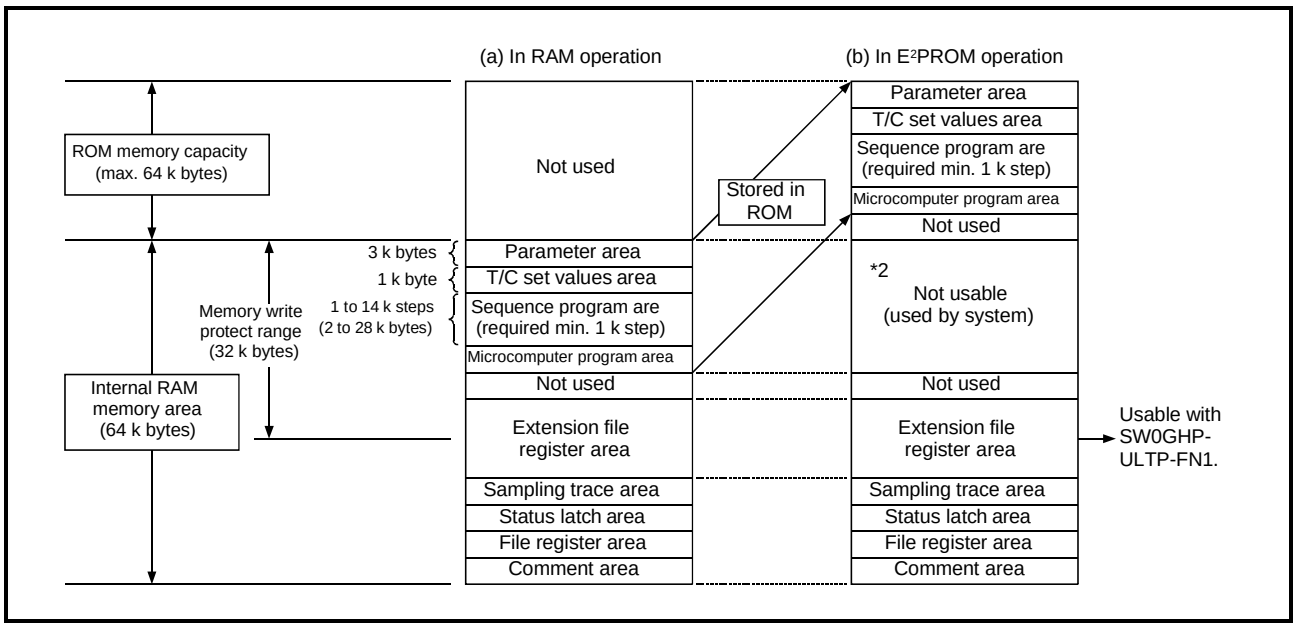
(a) When the A1SHCPU is used

Even if the main program is stored in an E^2PROM/EPROM, the capacities of the sampling trace, status latch, file register, and comment areas cannot be increased, because the system uses the internal RAM area (area indicated by *1 in the following figure) as in RAM operation.



(b) When the A2SHCPU(S1) is used

Even if the main program is stored in an E^{2}PROM, the area cannot be used for the extension file register, because the system uses the internal RAM area (area indicated by *2 in the following figure) as in RAM operation.



4.2 Functions

The following table describes the functions of the AnSHCPU.

Table 4.6 List of functions

Function	Description	Section reference
Constant scan	• Executes the sequence program at the predetermined intervals independently of the scan time. • Setting allowed from 10 to 2000 msec.	4.2.1
Latch (power interruption compensation)	• Retains device data while the PC is switched OFF or reset or a momentary power interruption of 20 msec or longer occurs. • L, B, T, C, D and W can be latched.	4.2.2
Remote RUN/STOP	• Allows remote RUN/STOP control from an external device (e.g. peripheral, external input, computer) with the RUN/STOP switch in the RUN position.	4.2.3
PAUSE	• Stops operation with the output (Y) status retained. • Pause function may be switched ON by using either of the following : Remote PAUSE contact Peripheral device	4.2.4
Status latch	• Stores all device data in the status latch area in the AnS when the status latch condition is switched ON. • The stored data can be monitored by a peripheral device.	4.2.5
Sampling trace	• Samples the specified device operating status at predetermined intervals and stores the sampling result in the sampling trace area in the AnS. • The stored data can be monitored by a peripheral device.	4.2.6
Offline switch	• Allows the device (Y, M, L, S, F, B) used with the OUT instruction to be disconnected from the sequence program processing.	4.2.7
Priority setting ERROR LED	• Sets the ON/OFF status of the ERROR LED in the event of an error.	4.2.8
Clock *1	• Executes clock operation in the CPU module. • Clock data includes the year, month, day, hour, minute, second, and day of the week. • Clock data can be read from special registers D9025 to D9028.	4.2.9

REMARK

The AnSHCPU cannot do "step operation", "PAUSE using RUN/STOP key switch", or "I/O module replacement at online".

*1 Handling the year 2000

Year 2000 is a leap year, so February 29 comes after February 28.
The AnSHCPU automatically fixes date by the clock element in the CPU module, so the user does not have to manually set the date to the clock element.
The year only contains the last two digits of the year. Therefore, when the clock data is read from the PC CPU and used in the sequence control, the year data may have to be fixed using a sequence program depending on the usage.

Year 1999 → "99"

Year 2000 → "00"

When comparison is made only with the last two digits of the year read, the year 2000 and consecutive years are considered older than the year 1999.

4.2.1 Constant scan

Because the processing time of each individual instruction in a sequence program differs depending on whether or not the instruction is executed, the scan time differs accordingly for each scan.

The constant scan function sets varying scan times to a fixed value regardless of the sequence program processing time.

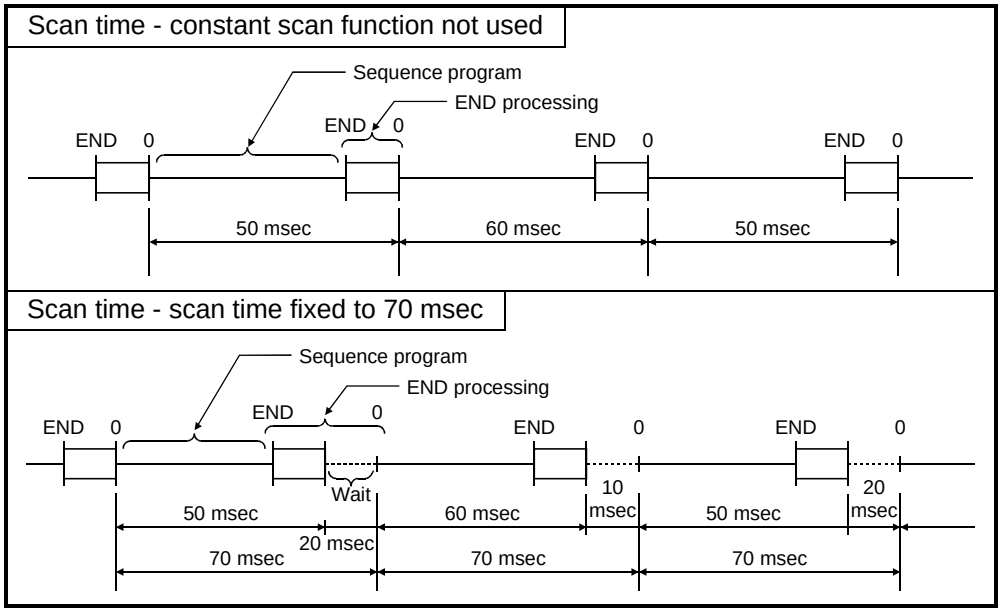


Fig. 4.4 Constant scan function

(1) Constant scan application

When executing simple positioning by turning output (Y) ON/OFF, the positioning time may vary since the ON/OFF timing of output (Y) differs for each scan. When using the constant scan function, variation in the positioning timing can be decreased by the ON/OFF timing of output (Y).

(2) Setting range

(a) Constant scan time can be set in the range of 10 to 2000 msec.

Enter the required constant scan time in special register D9020 in units of 10 msec (setting value between 10 and 2000 msec).

If the D9020 setting is outside the range of 1 to 200, the constant scan time will be as indicated below.

Setting for D9020	Constant scan time
-32768 to 0	Not set
1 to 200	10 to 2000 msec
201 to 32767	2000 msec

(b) The watchdog timer setting must be greater than the constant scan time setting.

If the watchdog timer setting is smaller than the constant scan time setting, a WDT error might occur.

The relationship between the constant scan time setting and the watchdog timer setting is indicated below.

(Constant scan time setting) ≤ (WDT setting) - 1

(c) The set constant scan time must be greater than the maximum scan time of the sequence program.

If the sequence program scan time is longer than the constant scan time, the constant scan function will not be executed correctly.

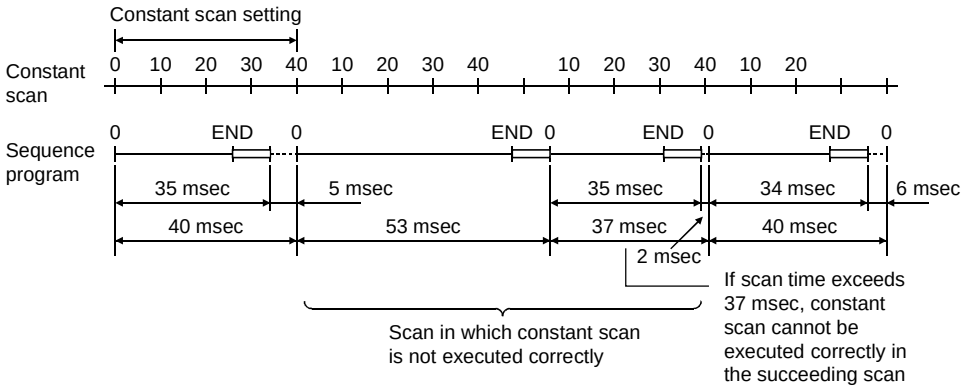


Fig. 4.5 Scan timer larger than constant scan setting

(3) Setting for constant scan execution

(a) Constant scan execution

A constant scan time setting is written to D9020 using the sequence program or a peripheral device (1 - 200).

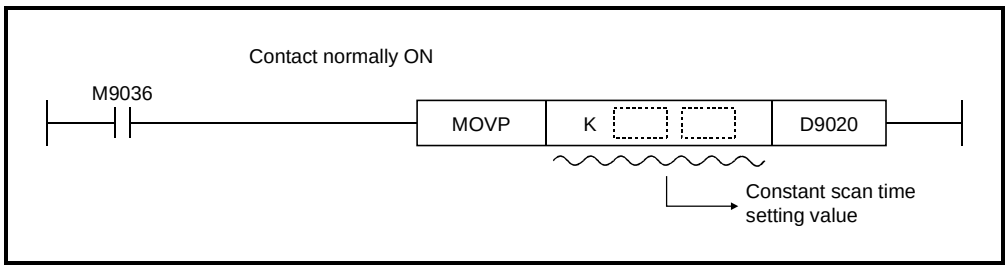
(b) Constant scan not executed

The value "0" is written to D9020 using the sequence program or a peripheral device.

(4) Precautions

(a) The constant scan time setting value stored in D9020 is cleared to zero (0) when the AnSHCPU power is turned ON or reset using the RUN switch.

Therefore, it is necessary to write the following program if a constant scan is required from the first scan immediately after the AnSHCPU is turned ON or reset.



(b) If a momentary power interruption within the allowable time occurs, the constant scan time is lengthened by the time taken up by the momentary power interruption. Accordingly, the constant scan function does not operate correctly.

(c) During constant scan time processing, the following interrupt processing is allowed.

Interrupt	Processing time
I/O interrupt	AD51(S3) general data processing : 0.2 to 0.5 msec Interrupts from AI61 or AD51(S3) : 0.2 msec + (interrupt program execution time of I0 to I17)
10 msec interrupt	1.0 msec + interrupt program execution time of I29 to I31
Interrupt from peripheral devices	0.2 msec

When the above interrupts overlap, the interrupt processing time becomes the total of the overlapping interrupts.

4.2.2 Power interruption compensation for device data in the AnSHCPU (LATCH function)

Data of all the AnS devices except devices specified as latch area are returned to default values (OFF for bit devices and 0 for word devices) when the power for AnSHCPU is interrupted or the reset switch is turned ON.

The latch function retains the device data if (a) the AnSHCPU is reset by turning ON the power, (b) the AnSHCPU is reset using the RUN/STOP switch, or (c) a momentary power interruption lasting 20 msec or more occurs.

The sequence program operation is the same whether or not the data is latched.

(1) Latch application

Even if a momentary power interruption occurs, the processing currently being carried out can continue because the latch function retains the data for production volume, number of defective products, and addresses.

(2) Latch devices and latch range setting

(a) The devices whose data can be latched are listed below :

1) Latch relays (L0 to L2047)
2) Link relays (B0 to B3FF)
3) Timers (T0 to T255)
4) Counters (C0 to C255)
5) Data registers (D0 to D1023)
6) Link registers (W0 to W3FF)

POINT

Device data within the latch range is backed up by the battery (A6BAT) installed in the AnSHCPU.

(1) The battery is required even when sequence program is stored in a ROM.
(2) Device data within the latch range is destroyed if the battery connector is disconnected from the AnSHCPU while the AnSHCPU power is turned OFF.

(3) Clearing the latched data

(a) To clear the latched data, perform the latch clear operation. The latch clear operation also clears unlatched device data as described below.

After the latch clear operation, the data in the each device is set as follows :

1)	Y, M/L/S, F, B	: Turned OFF.
2)	Special relays (M9000 to M9255)	: Data is retained.
3)	T, C	: Contacts and coils are turned OFF, the present value is set to 0.
4)	D, Z, V, W, A	: Data is set to 0.
5)	R	: Data is retained.
6)	Special registers (D9000 to D9127)	: Data is retained.

(b) Latched data can be cleared using either of the following two methods.

1) Using the RUN/STOP switch

i) Turn the RUN/STOP switch from the STOP position to the L.CLR position until the "RUN" LED flashes at high speed (goes ON and OFF at 0.2 sec intervals).

Flashing of the RUN LED at high speed indicates that the latched data is ready to be cleared.

ii) Turn the RUN/STOP switch from the STOP position to the L.CLR position while the RUN LED is flashing.
The latched data is cleared.

POINT

To cancel the latch clear operation, turn the RUN/STOP switch to the RUN or RESET position while the "RUN" LED is flashing.

(1) RUN position :
The AnSHCPU starts program processing.

(2) RESET position :
The AnSHCPU is reset.

2) Using the GPP function

The A6GPP "DEVICE MEMORY ALL CLEAR" of the test functions in the PC mode can be used to execute a latch clear.
(The GPP Operating Manual gives details.)

4.2.3 Running and stopping the AnSHCPU using external devices (remote RUN/STOP function)

The RUN switch is used for AnSHCPU RUN/STOP control.

"Remote RUN/STOP" operation means controlling the AnSHCPU RUN/STOP status with external signals (commands from peripheral devices, remote RUN contacts) with the RUN switch at the RUN position.

(1) Application of remote RUN/STOP

Remote RUN/STOP control is useful in the following cases :

(a) When the AnSHCPU is at a remote location.

(b) When the AnSHCPU is located in a control box.

(2) Executing a remote RUN/STOP

Remote RUN/STOP operation is possible using the following methods :

(a) Remote RUN contacts

Remote RUN/STOP control is possible by turning a remote RUN contact set in the parameters ON and OFF.

1) When the remote RUN contact is turned OFF, the AnSHCPU is set to the RUN status.

2) When the remote RUN contact is turned ON, the AnSHCPU is set to the STOP status.

Switching between RUN and STOP is executed after execution of the END(FEND).

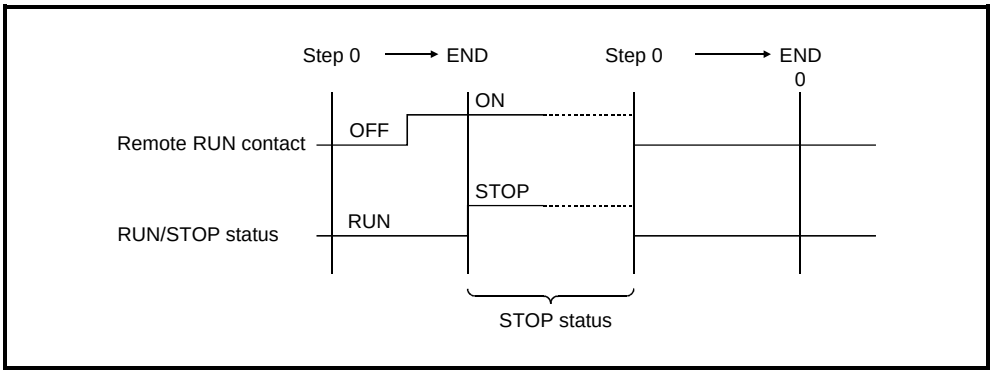


Fig. 4.6 Remote RUN/STOP timing chart when using a remote RUN contact

(b) The AnSHCPU RUN/STOP operation is executed by specifying remote RUN/STOP from a peripheral device, computer link module, or the AD51(S3).

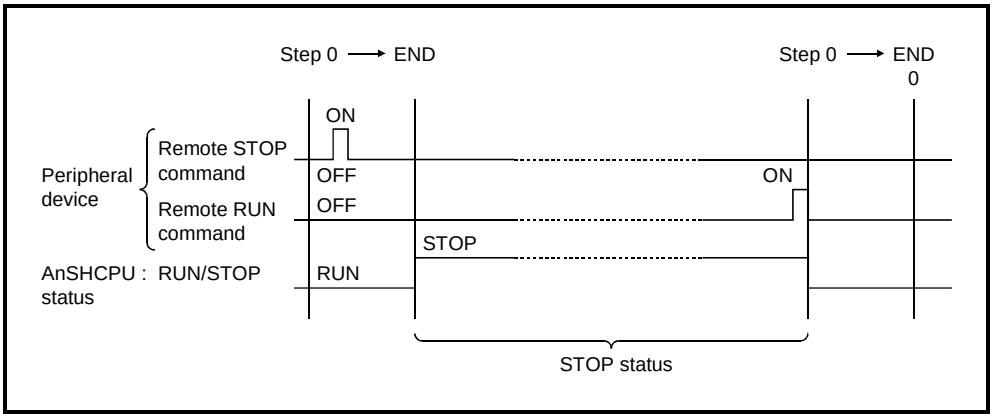


Fig. 4.7 Remote RUN/STOP timing chart when using the remote RUN/STOP command from a peripheral device

(3) Precautions

(a) Because the AnSHCPU gives priority to the STOP command, the following points must be kept in mind :

1) An AnSHCPU is turned to the STOP status when a STOP command is received from any of the following : a remote RUN contact, a computer link module or a programming device.

2) In order to turn the AnSHCPU to the RUN status when the AnSHCPU is in the STOP status due to a remote STOP command, all the STOP factors have to be changed to RUN.

4.2.4 Stopping the sequence program operation while retaining output status (PAUSE function)

The PAUSE function stops AnSHCPU operations while retaining the status of all outputs (Y).

(1) Application

The PAUSE function is useful for systems that do not allow output to be turned off even while the CPU is in the STOP status.

(2) Method

Either remote PAUSE contacts or peripheral devices can be used.

(a) Using a remote PAUSE contact

1) The PAUSE status contact (M9041) closes after execution of the END(FEND) instruction of the scan during which the remote PAUSE contact closes and the PAUSE enable flag (M9040) is set.

When the END(FEND) instruction of the scan after M9041 setting is executed, the AnS is set to PAUSE and its operation stops.

2) When the remote PAUSE contact is opened or M9040 is switched OFF via an external device (peripheral device, computer etc.), the PAUSE status is canceled and sequence program operations resume from step 0.

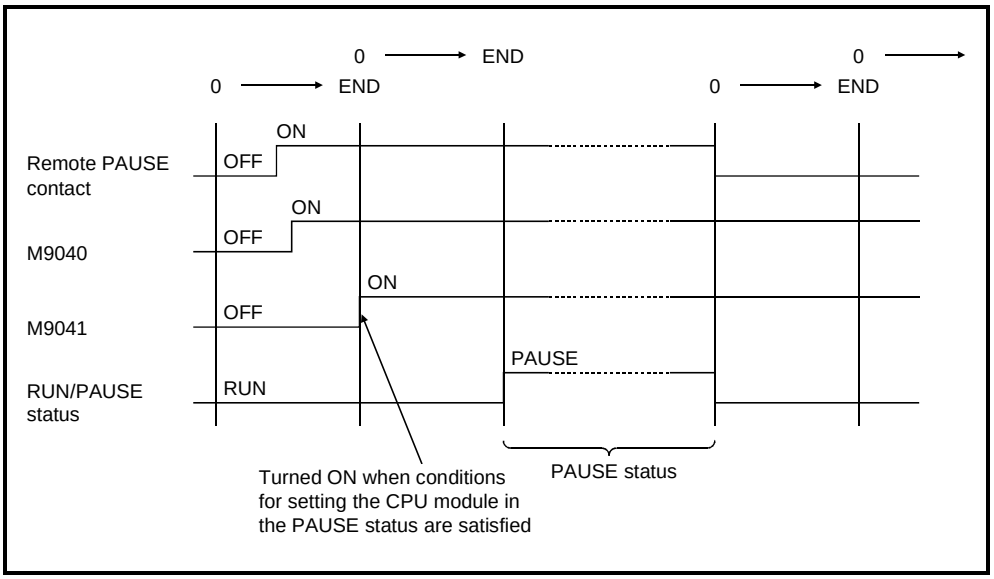


Fig. 4.8 PAUSE timing using a remote PAUSE contact

(b) Peripheral devices

1) The PAUSE status contact (M9041) closes after execution of the END (FEND) instruction of the scan during which the remote PAUSE command from a peripheral device is received.

When the END (FEND) instruction of the scan after M9041 has set is executed, the AnS is set to PAUSE and its operation stops.

2) When a remote RUN command from a peripheral device is received, the PAUSE status is canceled, and sequence program operations resume from step 0.

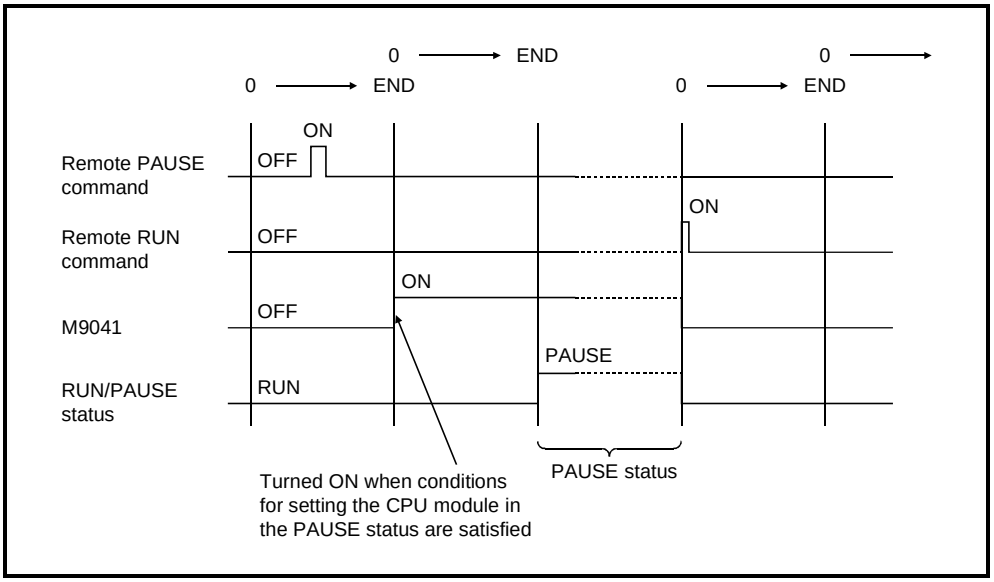
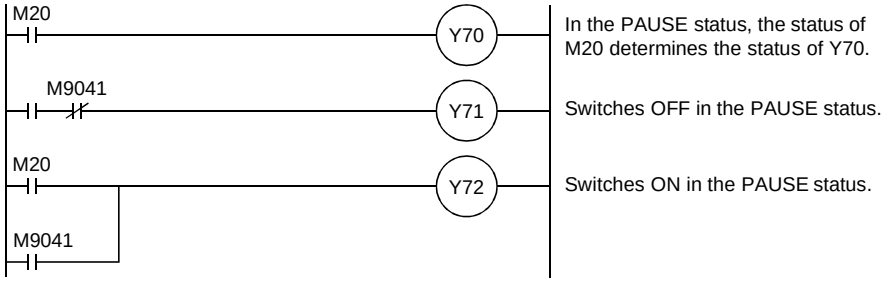


Fig. 4.9 PAUSE timing chart when using a peripheral device

POINT

(1) (M9041) is used as an interlocking contact to switch ON or OFF the output (Y) in the PAUSE status, take interlock with the PAUSE status contacts (M9041).



4.2.5 Status latch

The status latch function copies all device data to the status latch area when an SLT instruction is executed. After the data has been copied, the data in the status latch area can be monitored by a programming device.

Status latch data can be read by using the GPP function in oder to monitor it.

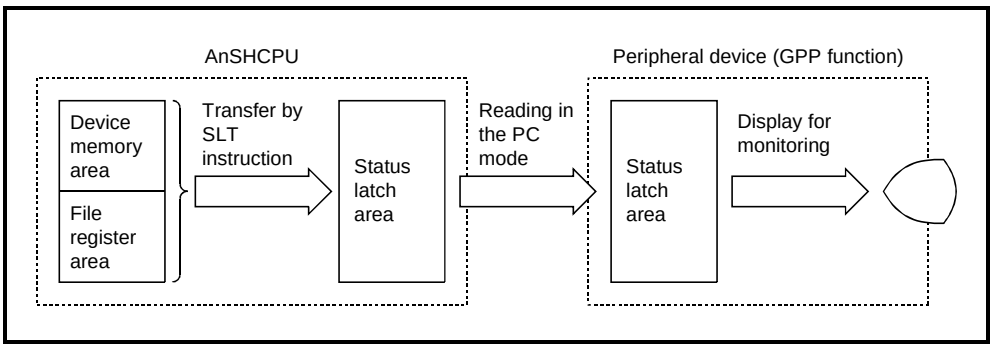


Fig. 4.10 Status latch operation

(1) Applications

The status latch function can be used to check device data when an error is found during debugging.

It is also used to find out the cause of an error during sequence program execution. This is achieved by making a program that will execute the SLT instruction if an error condition arises.

(1) Processing

(a) The following data is stored in the status latch area when an SLT instruction is executed.

1) Device memory

X, Y, M, L, S, F, B : ON/OFF data

T, C : Contact and coil ON/OFF data and present values

D, W, A, Z, V : Stored data

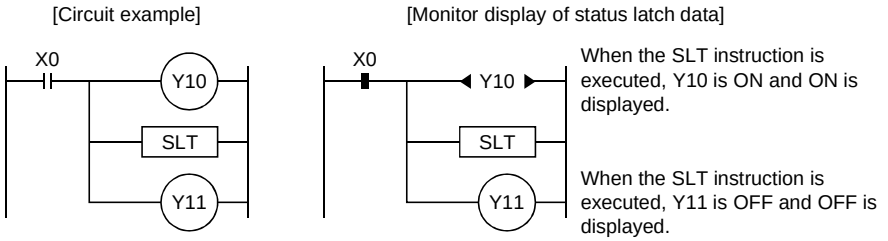
2) File register (R) : Stored data

(b) Data is stored in the status latch area when an SLT instruction is executed.

With devices which turn ON/OFF or store data using the same condition, the data to be stored in the status latch area differs before and after executing an SLT instruction.

Example :

If a device which is turned ON and OFF by the same condition occurs before and after the SLT instruction in a program, the ON/OFF status display will differ before and after the execution of the SLT instruction.



(3) Precaution

(a) Executing an SLT instruction causes the scan time to be increased by the time indicated below.

Therefore, take this into consideration when determining the watchdog timer setting and the constant scan time setting for the AnSHCPU.

	Device memory only	**Device memory and file register**
Processing time (msec)	8.5	17

4.2.6 Sampling trace

It is not possible to check the transition of the ON/OFF status of bit devices and the data in word devices using a peripheral device monitor function.

The sampling trace function samples the data from designated devices at fixed intervals and stores the sample data in the sampling trace area.

After the STRA instruction is executed, the data stored in the sampling trace area is sampled the designated number of times and the device data is latched.

Data stored in the sampling trace area can be read by using the GPP function to monitor it.

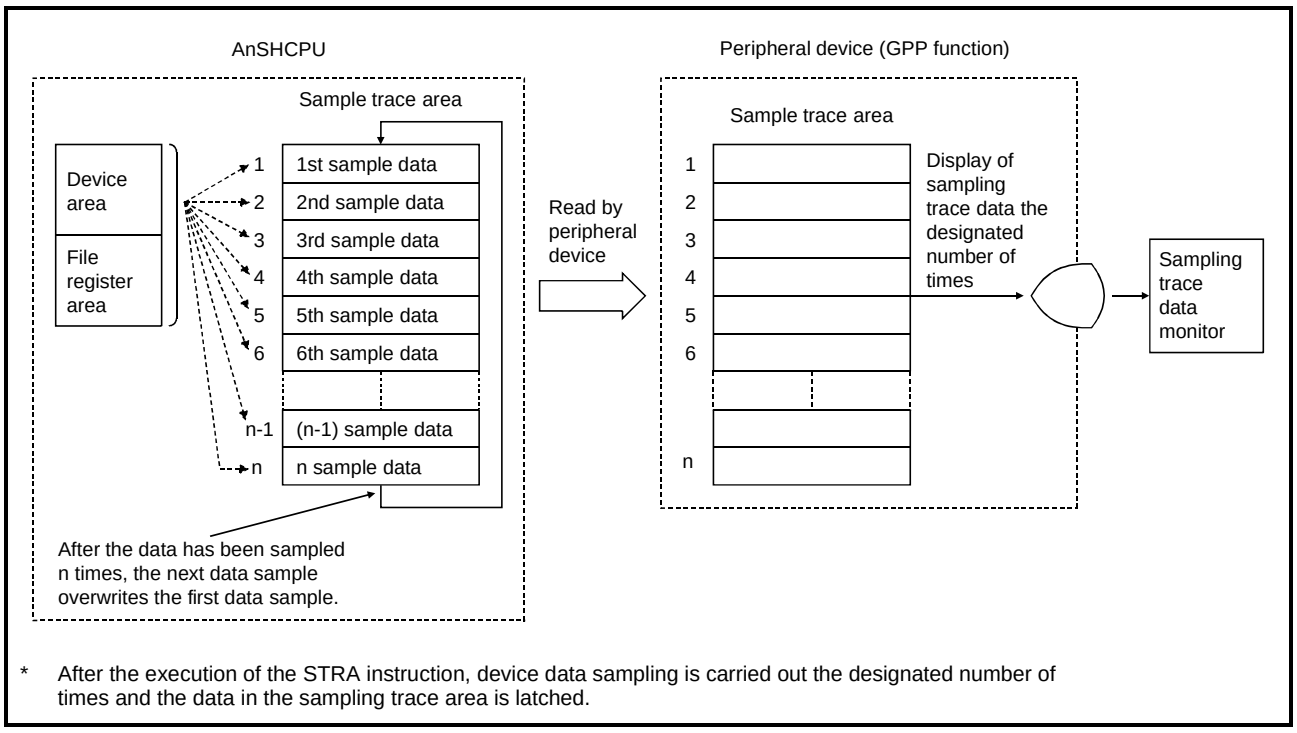


Fig. 4.11 Sampling trace

(1) Application

By using the sampling trace function, the debugging time can be shortened by verifying the data of the designated devices at defined intervals during debugging.

(2) Devices which can be sampled

The devices and the number of points which can be sampled are indicated below.

(a) Bit devices

(X, Y, M, L, S, F, B, T/C coil, T/C contact) Max. 8 points

(b) Word devices

(T/C present value, D, W, R, A, Z, V) Max. 3 points

(3) Number of sampling times

The total number of sampling times and number of sampling times after the execution of the STRA instruction need to be specified.

(a) Total number of sampling times

This number signifies the size of the area where the sampling data is stored.

The allowed setting range is 0 to 1024 times in units of 128 times.

(b) Number of sampling times after the execution of the STRA instruction

When the number of samplings reaches this number, the CPU terminates sampling and retains the sampled data.

The allowed setting range is 0 to 1024 times in units of 128 times.

The number of sampling times after the execution of the STRA instruction	≤	Total number of sampling times	≤	1024 times

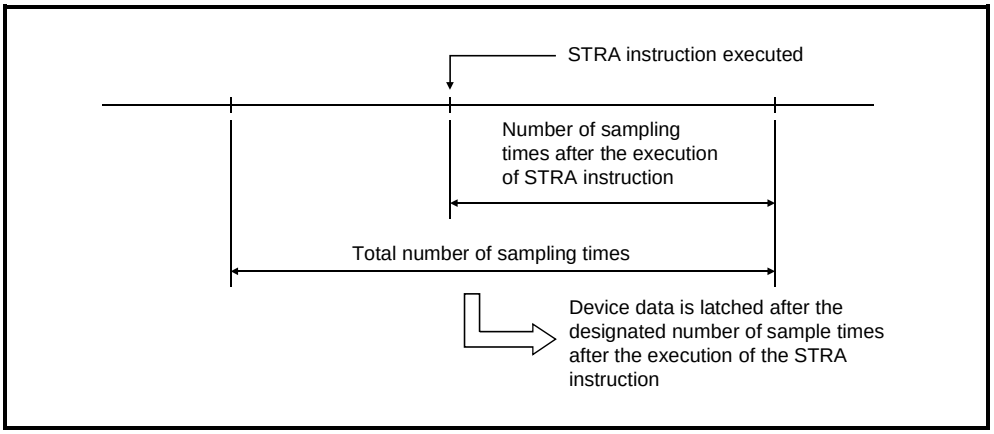


Fig. 4.12 Number of sampling times

(4) Sampling intervals

The sampling interval can be selected as either of the following: after the execution of END instruction or at defined intervals.

(a) After execution of an END instruction

Data is sampled each time an END instruction is executed.

(b) At defined intervals

Data is sampled at defined intervals, 10 × n msec (n : 0 to 199).

In this case, data is sampled even during execution of the sequence program.

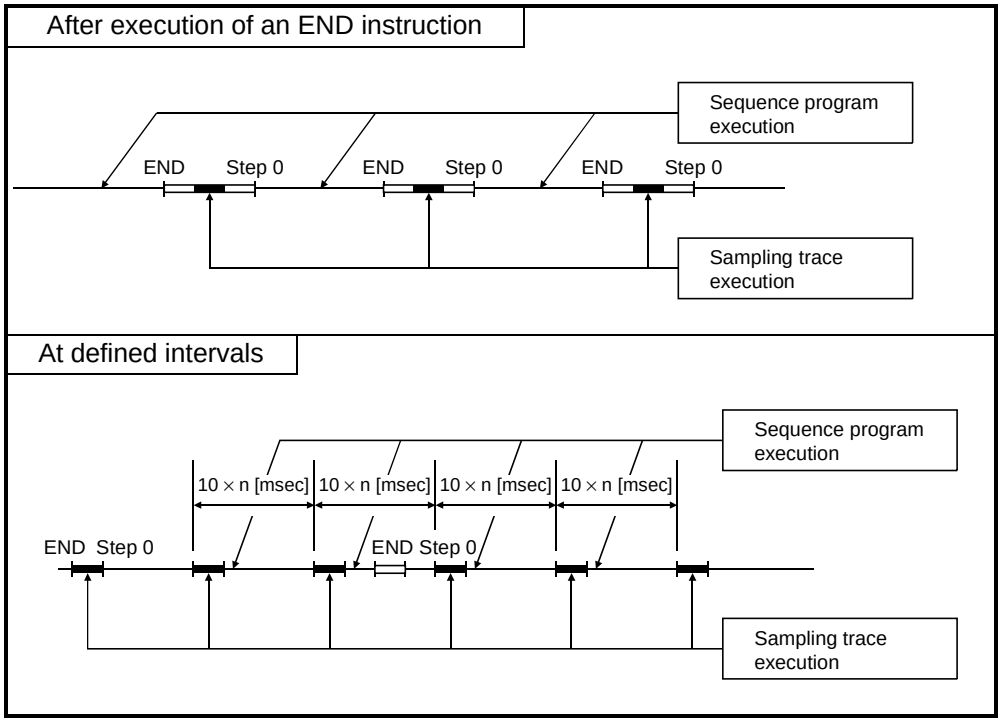


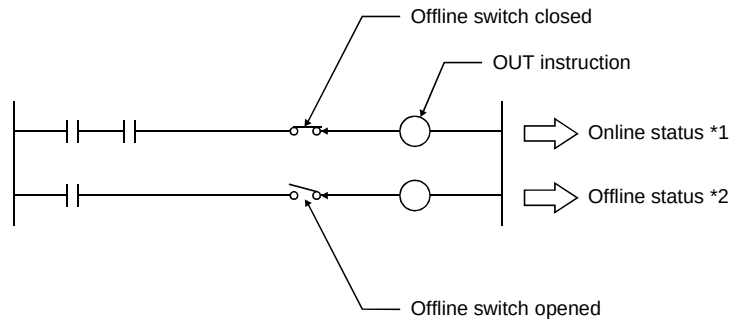
Fig. 4.13 Sampling trace executions

4.2.7 Offline switch function

While the AnSHCPU is running (during the execution of a sequence program), it is not possible to turn sequence program OUT instruction devices ON and OFF using a peripheral device test function.

The offline switch function allows these devices to be turned ON and OFF with a peripheral device test function while the AnSHCPU is running.

It is possible to check operation of OUT instruction devices, which are not turned ON and OFF by the sequence program, and to check the wiring between the output module and an external device with the offline switch function.



*1 : This online status is established when the offline switch is closed. The OUT instruction device is controlled (turned ON/OFF) by the sequence program.

*2 : The offline status is established when the offline switch is opened. The OUT instruction is isolated from the sequence program. In the offline status, it is not possible to control the OUT devices using the sequence program.

Fig. 4.14 Offline and online status

(1) Devices which can use the offline switch function

The following devices can use the offline switch function :

(a) Outputs (Y)

(b) Internal relays (M)

(c) Latch relays (L)

(d) Step relays (S)

(e) Link relays (B)

(f) Annunciators (F)

(2) Status of devices in the offline status

The status of devices in the offline status (offline switch opened) as follows.

(a) The ON/OFF status that existed just before the offline status was established is retained.

(b) When a forced set/reset is executed using a peripheral device in the offline status, the reset/set status after the forced set/reset is retained.

(3) Operating procedures

(a) To set the AnSHCPU in the offline status, use a peripheral device to set the offline switch.

(b) To return the AnSHCPU from the offline status to the online status, use either of the following two methods :

1) Reset the offline switch setting using a peripheral device.

2) Reset the AnSHCPU with the RUN/STOP keyswitch.

POINT

(1) Devices set in the offline status cannot be turned ON and OFF using a sequence program.
Devices set in the offline status during testing must be returned to the online status by resetting the off line switch after completing the test operation.

(2) Devices returned from the offline status to the online status can be turned ON and OFF using a peripheral device.
Before returning such devices to the online status, check the input conditions of OUT instructions. Make sure that no problems will arise when the devices are returned to the online status.

4.2.8 Setting priorities for ERROR LED display

By changing the setting, the following can be done :

(a) The ERROR LED can be made to stay OFF even when an error (see Table 4.7) that normally turns ON the ERROR LED occurs, if indication of the error is not necessary.

For example, the ERROR LED can be made to stay OFF when an annunciator (F) is turned ON.

However, the setting cannot be changed for errors that stop the sequence program.

(b) An LEDR instruction can be used to reset annunciators.

By setting the annunciator to the first priority, an LEDR instruction can be used to reset the annunciator even if another error occurs.

(Normally, if a higher-priority error occurs, the annunciator cannot be reset.)

(1) The default setting of priorities for ERROR LED display is shown in Table 4.7.

Table 4.7 Priority for ERROR LED display

Priority	Error contents	Error item number	ERR LED
High ▲	Error which causes the AnSHCPU to stop unconditionally	—	Lit
	I/O module verification error Blown fuse error	1	
	Special module fault Link parameter error Operation error	2	
	CHK instruction execution	3	OFF
	Annunciator (F) turning ON	4	Flashing
Low	Battery error	6	Lit

(2) Changing the priorities

The ERROR LED display priority in D9038 and D9039 (the LED display priority storage register) is changed by changing the previously set error item number.

Fig.4.15 shows the error number storage for each priority and the default values (initially set by the PC CPU).

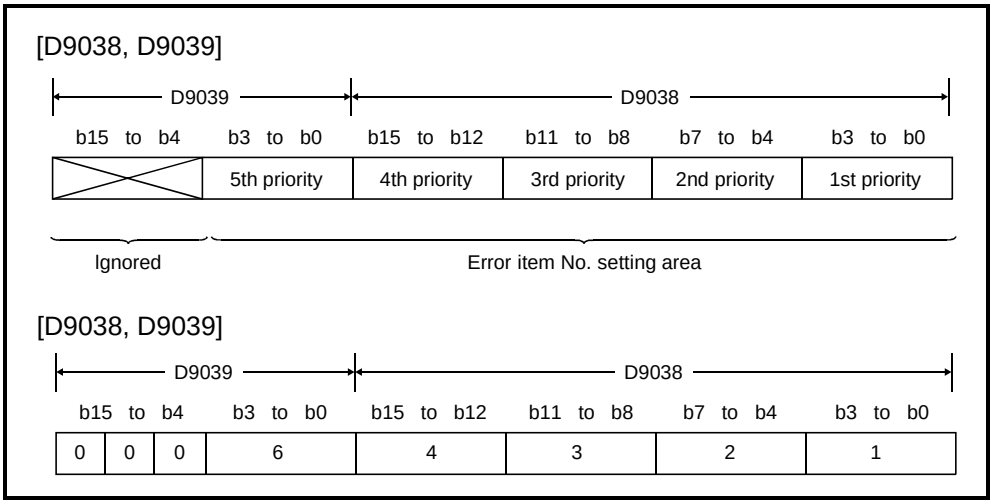
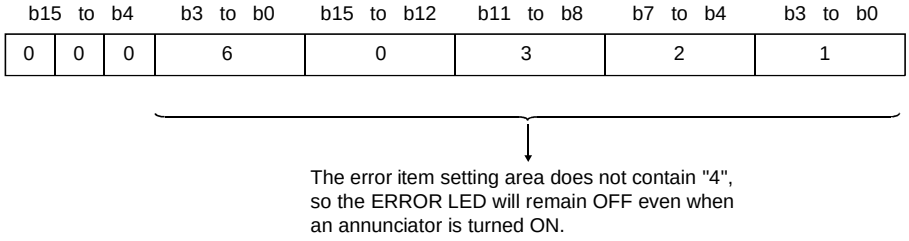


Fig. 4.15 Error priority in D9038 and D9039 and error setting items

POINT

(1) The ERROR LED is not lit if an error in Table 4.7 for which error indication priority is not set occurs. If all bits are "0" in D9038 and D9039, for example, the ERROR LED will not be lit when any errors among those corresponding to error item numbers 1 to 6 occurs.

Example : To make the ERROR LED stay OFF when an annunciator (F) is turned ON, change the error item number area initially set to "4" to "0".



(2) In this case, however, M9008 (the CPU error flag) is set and the corresponding error code is stored in D9008 (CPU error register).

In order to change the priorities, store the error item number listed in Table 4.7 in each priority area of D9038 and D9039 (the LED display priority storage registers).

4.2.9 Clock function

The AnSHCPU has an internal clock function. Time management is made possible by reading clock data.

Clock operations continue by using battery backup in the memory cassette even when the PC power is OFF or there is a momentary power interruption lasting 20 msec or longer.

(1) Clock data is the data of the clock inside the AnSHCPU. This data is shown below.

Data	Year, month, date, hour, minutes, seconds, day
Year	Last 2 digits
Month	1 to 12
Data	1 to 31 (Leap years automatically detected)
Hour	0 to 23 (24 hour)
Minutes	0 to 59
Seconds	0 to 59
Day	0 to 6 (Sunday to Saturday)

(2) Clock accuracy varies according to ambient temperature as follows :

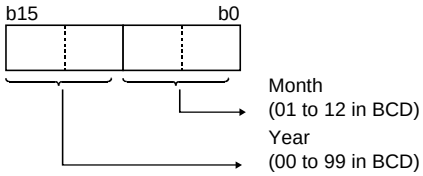
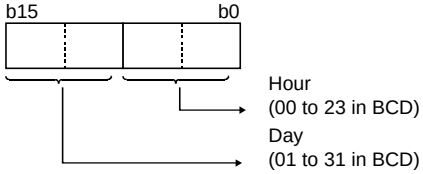
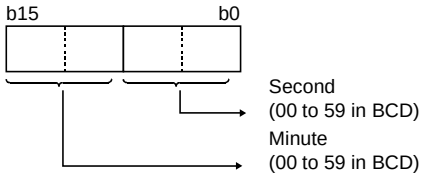
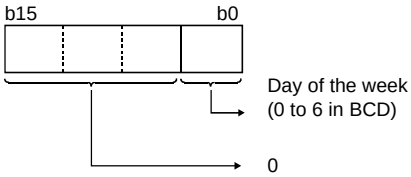
Ambient temperature (°C)	Accuracy (Weekly difference, sec)
+ 55	within ± 11
+ 25	within ± 15
0	within ± 1

(3) Clock data can be read and written using special relays, special registers or dedicated instructions.

(a) The special relays used for the clock function are as follows :

Device	Name	Description
M9025	Request to set clock data	• Clock data stored in D9025 to D9028 is written to the clock device after the execution of END in the scan in which M9025 status is changed from OFF to ON.
M9026	Clock data error	• Turned ON if set clock data is not BCD code.
M9028	Request to read clock data	• Clock is read to D9025 to D9028 after the execution of END when M9028 is ON.

(b) Special relays

Device	Contents	Description
D9025	Clock data (Year, month)	
D9026	Clock data (Day, hour)	
D9027	Clock data (Minute, second)	
D9028	Clock data (Day of the week)	 Day of the week / Store data: Sun 0, Mon 1, Tue 2, Wed 3, Thu 4, Fri 5, Sat 6

(4) Clock data setting to the clock devices

(a) Store the clock data in D9025 to D9028 in BCD code.

(b) When M9025 is turned ON, clock data stored in D9025 to D9028 is written to the clock device.

POINT

Clock data is not set at factory shipment, clock data must be once set if the clock function is necessary.

All clock data must be rewritten to the clock device even when part of the clock data needs to be changed.

Normal clock operation cannot be performed if invalid data is written.

Example

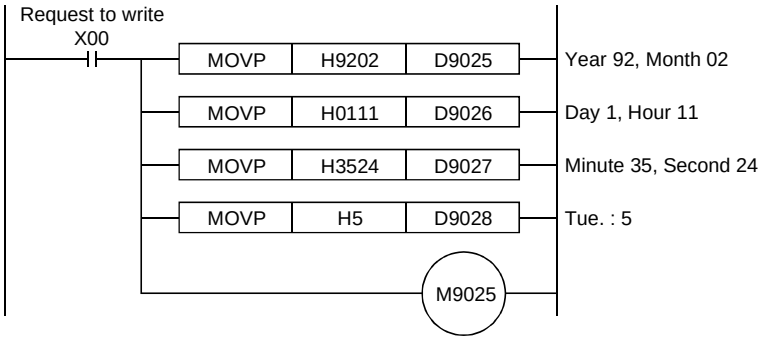
Month : 13

Day : 32

(5) Clock data read

Clock data can be read to D9025 to D9028 from the clock device by turning on M9028.

(6) Clock data write program example



4.3 Handling Instructions

This section gives handling instructions from unpacking to installation of the AnSHCPU, I/O module, extension base unit, etc.

(1) Since the case, terminal block connector, and pin connector of this PC are made of plastic, do not drop them or subject them to mechanical shock.

(2) Do not remove the printed circuit board of any module from its case. Removal may cause board damage.

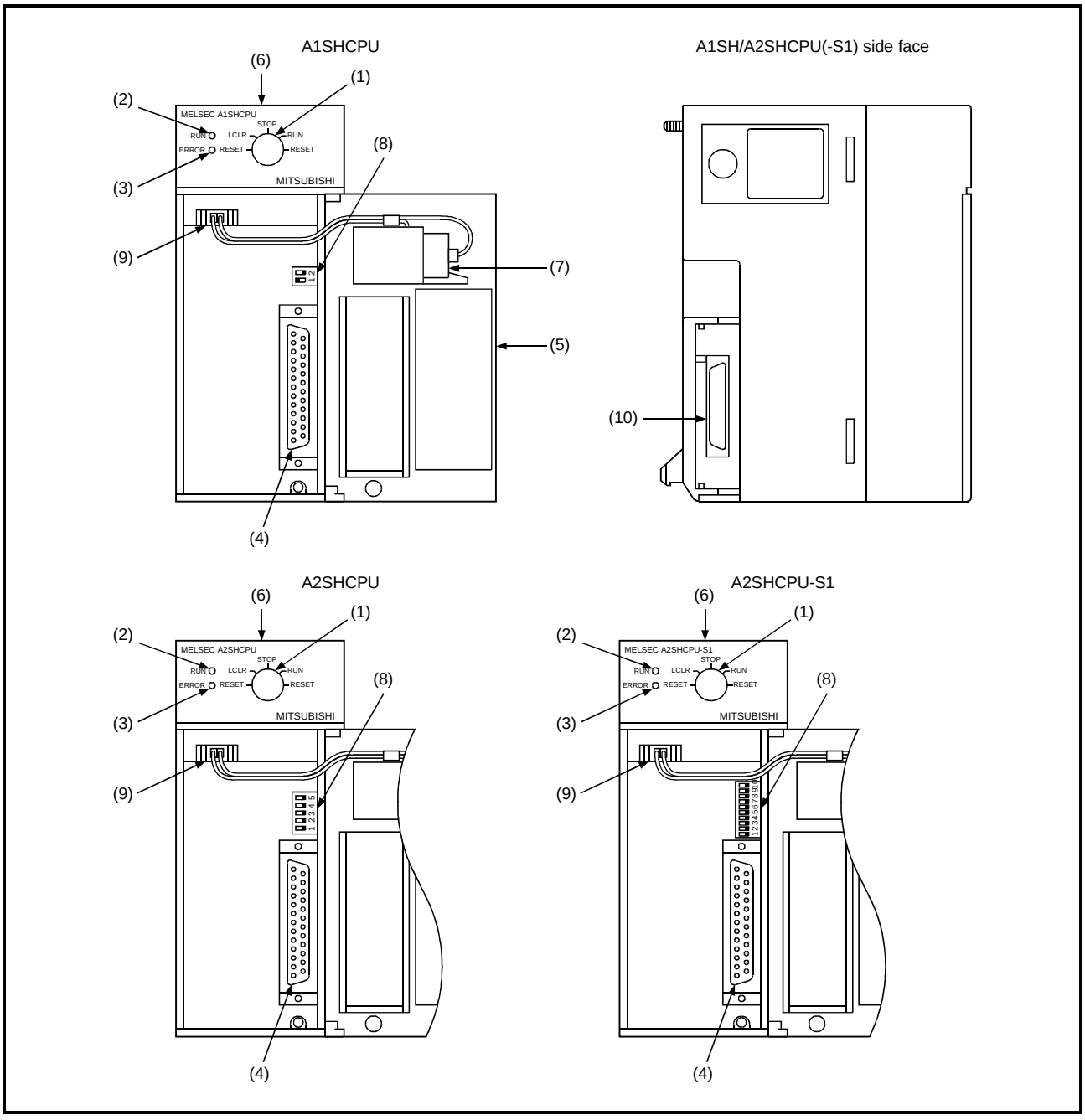
(3) When wiring, take care to prevent entry of wire offcuts into the module. If any conductive debris enters the module, make sure that it is removed.

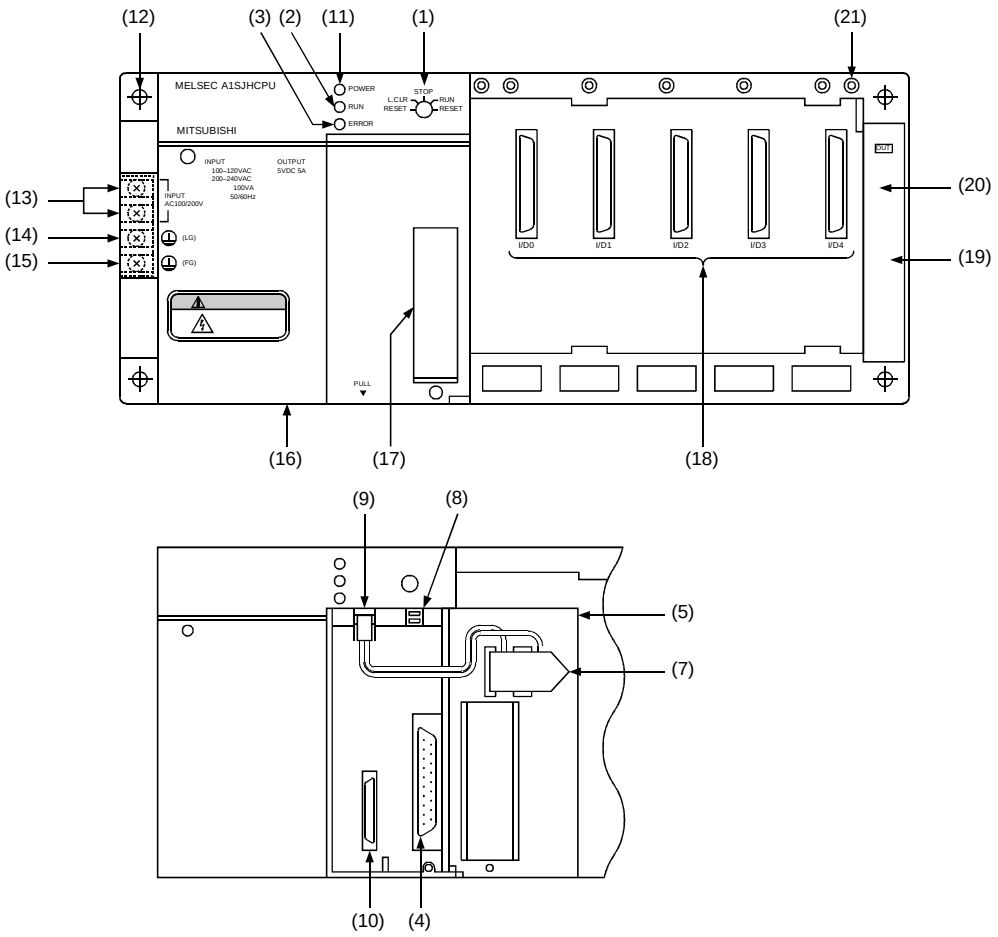
(4) Tighten the module mounting screws and terminal screws as indicated below.

Screw	Tightening torque range N · cm [kg · cm] (lb · in.)
Module mounting screw (M4 screw)	78 to 118 [8 to 12] (45 to 67)
I/O module terminal block terminal screw (M3.5 screw)	59 to 88 [6 to 9] (34 to 50)

4.4 Part Identification and Setting of AnSHCPU

4.4.1 Part identification





No.	Name	Function
(1)	RUN/STOP key switch	• RUN/STOP : To start/stop running a sequence program. • RESET : To reset the hardware. To reset an error occurring during operation to initialize operation. • LATCH CLEAR (L.CLR) : To clear (turn OFF, or clear to "0") the data in the latch range and non-latch range which are set by parameter. For the latch clear operation procedure, see Section 4.4.4
(2)	"RUN" LED	• ON : Indicates that a sequence program operation is being executed with the RUN key switch set to the RUN position. 〔The LED remains lit if an error (Section 11.3), which permits sequence operation to continue, occurs.〕 • OFF : The RUN LED goes out in the following cases : • When the RUN key switch is in the STOP position. • When the remote STOP signal is input. • When the remote PAUSE signal is input. • Flashing : The RUN LED flashes in the following cases : • When an error which causes sequence operation to stop is detected by the self-diagnosis function. • When the latch clear operation is executed.
(3)	"ERROR" LED	• ON : Indicates that the self-diagnosis function has detected an error. 〔When the detected error is set to "not lit" in the ERROR LED indication priority setting.〕 • OFF : Indicates that no error has occurred or that a malfunction has been detected by the [CHK] instruction. • Flashing : An annunciator (F) is turned ON by the sequence program.

No.	Name	Function
(4)	RS-422 connector	• Used to connect a peripheral device to write/read, monitor, or test a program using a peripheral device. • Close with the cover when not connected to a peripheral device.

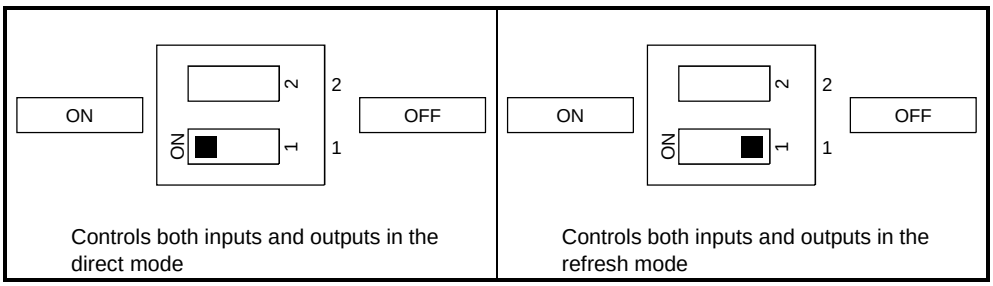
(5)	Cover	• Protects AnSHCPU printed circuit board, memory cassette, RS-422 connector, battery, etc.
		• Execute the following operations with the cover open.
		  • Memory cassette connection/disconnection
		  • Setting a dip switch
		  • Connection to battery connector
		  • For mounting the module to the base unit battery replacement

(6)	Module fixing screws	• For mounting the module to the base unit
(7)	Battery	• For retaining data such as programs, device latch ranges, file registers, etc. (See Section 7.2 for battery replacement.)
(8)	DIP switch	• Used for switching the I/O control method and for setting the memory protect function. (See Sections 4.4.2 and 4.4.3)
(9)	Battery connector	• For connection to the battery
(10)	Memory cassette installing connector	• For installing the memory cassette
(11)	"POWER" LED	• 5 V DC power display LED
(12)	Base installation hole	• Hole to install the base unit to a panel such as a control board. (M5 screw)
(13)	Power supply input terminals	• Connect the 100 V AC or 200 V AC power for the power input terminal.
(14)	LG terminals	• Power filter grounding terminal. Has half the voltage level of the input voltage.
(15)	FG terminals	• Grounding terminal connected to the shielding pattern on the print board.
(16)	DIN rail	• DIN rail installation hook (2)
(17)	RS-422 connector cover	• RS-422 connector cover
(18)	Module connector	• Connector to install the I/O module or special module. For the connector not for module installation, install supplied connector cover, or blank cover (A1SG60) to prevent dust entry.
(19)	Extension cable connector	• Connect the extension cable with the signal send/receive connector with the extension base unit.
(20)	Base cover	• Extension connector protective cover. To extend, the area surrounded by the groove below the OUT sign on the base cover must be removed using tools such as a nipper.
(21)	Module fixing screws	• Screws to fix the module to the base. (M4 × 12 screws)

4.4.2 I/O control switch setting

The I/O control system uses either the direct mode or the refresh mode. Use the DIP switch (SW1) to switch the I/O control mode.

On shipment from the factory, the direct mode is set for both inputs and outputs (SW1 : ON).



POINT

Make sure that the power is OFF be to reswitching the I/O control mode.

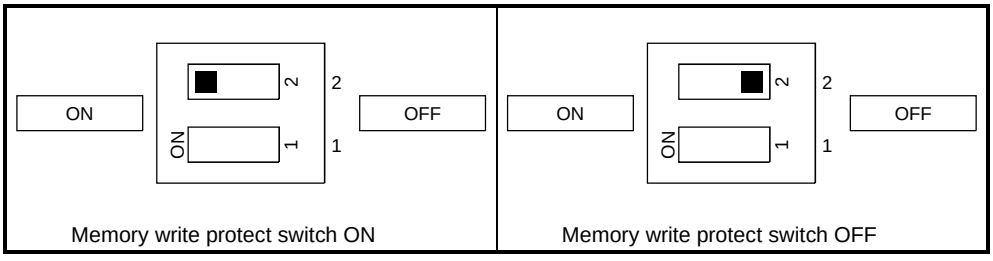
4.4.3 Memory write protect switch setting

The memory write protect switch is designed to protect data in the RAM memory from being overwritten due to incorrect operation or malfunction of a peripheral device.
It is used to prevent overwriting or deletion of created programs.
To modify data in RAM memory, the memory write protect switch must be turned OFF.
The memory write protect switch is set to OFF (SW2 : OFF) before shipment from the factory.

(1) When the A1SHCPU/A1SJHCPU is used

The memory write protect function of the A1SHCPU/A1SJHCPU is set ON/OFF by using a DIP switch (SW2). The memory write protect function protects the first 32 k bytes of the 64 k byte user memory area. (When the CPU is equipped with a memory cassette or operated using a ROM or E^2PROM, the memory write protect switch setting is invalid.)

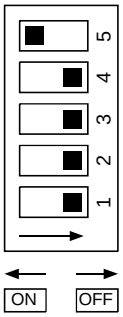
By selecting the ON position on this switch, the parameters, the program and a part of extension file register will be write-protected in the memory. (See Section 4.1.9.)



(2) When the A2SHCPU(S1) is used

The memory write protect range can be changed by changing the settings of the memory write protect DIP switches. For details, see Fig. 4.16. The SW2 may be in the ON or OFF position.

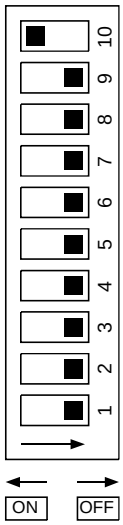
A2SHCPU



Switch No.	Application
5	I/O select switch setting ON : Direct method OFF : Refresh method
	Memory write protect setting (RAM and E^{2}PROM) ON : With memory write protection *1 OFF : Without memory write protection
	Memory write protection range
4	48 to 64 k bytes
3	32 to 48 k bytes
2	16 to 32 k bytes
1	0 to 16 k bytes

*1 When installing the memory cassette, the setting becomes invalid to RAM only.

A2SHCPU-S1



Switch No.	Application
10	I/O select switch setting ON : Direct method OFF : Refresh method
	Memory write protect setting (RAM and E^{2}PROM) ON : With memory write protection *1 OFF : Without memory write protection
	Memory write protection range
9	144 to 192 k bytes
8	112 to 144 k bytes
7	96 to 112 k bytes
6	80 to 96 k bytes
5	64 to 80 k bytes
4	48 to 64 k bytes
3	32 to 48 k bytes
2	16 to 32 k bytes
1	0 to 16 k bytes

*1 When installing the memory cassette, the setting becomes invalid to RAM only.

Fig. 4.16 Memory write protect DIP switch settings

POINT

(1) Set the memory write protect range according to the address (step number) of each memory area (sequence program, comment, sampling trace, status latch, file register).

(2) Do not use the memory write protect function when executing a sampling trace or status latch since it will make it impossible to store the data in the memory.

4.4.4 Clearing latched data

Follow the procedure described below to clear latched data using the RUN/STOP key switch. The latch clear operation also clears unlatched device data.

(1) Turn the RUN/STOP key switch from the "STOP" position to the "L.CLR" position several times to make the "RUN" LED flash quickly (ON for approximately 0.2 seconds and OFF for approximately 0.2 seconds). The quickly flashing "RUN" LED indicates that the preparation for the latch clear operation is completed.

(2) Turn the RUN/STOP key switch from the "STOP" position to the "L.CLR" position again while the "RUN" LED is flashing. The latched data will be cleared, and the "RUN" LED will go OFF.
To cancel the latch clear operation, turn the RUN/STOP key switch to the "RUN" position to make the AnSCPU start processing, or to the "RESET" position to reset the AnSCPU.

REMARK

Latched data can be cleared using the GPP function.
The A6GPP, for example, performs latch clear using "DEVICE MEMORYALL CLEAR" of the test functions of the PC mode.
See the GPP Operating Manual for details.

5. POWER SUPPLY MODULE

5.1 Specifications

(1) Table 5.1 shows the specifications of the power supply modules.

Table 5.1 Power supply modules specifications

Item		Specifications			
		A1S61P	A1S62P	A1S63P	
Base loading slot		Power supply module loading slot			
Rated input voltage		100 to 120 V AC + 10 %/-15 % (85 to 132 V AC)		24 V DC (+ 30 %/- 35 %) (15.6 to 31.2 V DC)	
		200 to 240 V AC + 10 %/-15 % (170 to 264 V AC)			
Rated input frequency		50/60 Hz ± 3 %		—	
Input voltage distortion factor		Within 5 % (See Section 8.8)			
Max. input apparent power		105 V A		41 Ω	
Inrush current		20 A 8 ms or lower		81 A 1 ms or lower	
Rated output current	5 V DC	5 A	3 A	5 A	
	24 V DC ± 10 %	—	0.6 A	—	
Overcurrent protection	5 V DC	5.5 A or higher	3.3 A or higher	5.5 A or higher	
	24 V DC	—	0.66 A or higher	—	
Overvoltage protection	5 V DC	5.5 to 6.5 V			
	24 V DC	—			
Efficiency		65 % or higher			
Allowable momentary power failure time *3		20 ms or lower		1 ms or lower	
Dielectric withstand voltage	Between primary and 5 V DC	1500 V AC *1	1500 V AC *1	500 V AC	
	Between primary and 24 V DC	—	1500 V AC *1	—	
Insulation resistor		5 M Ω or higher at insulation resistance tester			
Noise durability		Noise voltage 1500 Vp-p, Noise width 1 μs, Noise frequency 25 to 60 Hz (noise simulator condition)		Noise voltage 500 Vp-p, Noise width 1 μs, Noise frequency 25 to 60 Hz (noise simulator condition)	
Power indication		Power LED indication (light at the time of output of 5 V DC)			
Terminal screw size		M3.5 × 7			
Applicable wire size		0.75 to 2 mm^2 (AWG 18 to 14)			
Applicable solderless terminal		RAV 1.25 to 3.5, RAV 2 to 3.5			
Applicable tightening torque		59 to 88 N·cm (6 to 9 kg·cm)			
External dimension [mm (in.)]		130 × 55 × 93.6 (5.12 × 2.17 × 3.69)			
Weight [kg (lb.)]		0.53 (1.17)	0.55 (1.21)	0.5 (1.1)	

*1: Overcurrent protection

The overcurrent protection device shuts off the 5 V, 24 V DC circuit and stops the system if the current flowing in the circuit exceeds the specified value. When this device is activated, the power supply module LED is switched OFF or dimly lit. If this happens, eliminate the cause of the overcurrent and start up the system again.

*2: Overvoltage protection

The overvoltage protection device shuts off the 5 V DC circuit and stops the system if a voltage of 5.5 to 6.5 V is applied to the circuit. When this device is activated, the power supply module LED is switched OFF. If this happens, switch the input power OFF, then ON to restart the system. The power supply module must be changed if the system is not booted and the LED remains OFF.

	A1S61PEU	A1S62PEU	A1S61PN	A1S62PN
	200 to 240 V AC (10 %/- 15 %) (170 to 264 V AC)		100 to 240 V AC (+ 10 %/-15 %) (85 to 264 V AC)	
	50/60 Hz ± 5 %			
	105 V A			
	40 A 8 ms or lower		20 A 8 ms or lower	
	5 A	3 A	5 A	3 A
	—	0.6 A	—	0.6 A
	5.5 A or higher	3.3 A or higher	5.5 A or higher	3.3 A or higher
	—	0.66 A or higher	—	0.66 A or higher
	20 ms or higher			
	1780 V AC	1780 V AC	AC across input/LG and output/FG 2830 V AC rms/3 cycle (2000 m (6562 ft.))	
	—	1780 V AC		
	5 M Ω or higher at insulation resistance tester		AC across input/LG and output/FG5 M Ω or higher, measures with a 500 V DC insulation resistance tester	
	(1) Noise voltage 1500 Vp-p, Noise width 1 μs, Noise frequency 25 to 60 Hz (noise simulator condition) (2) Noise voltage IEC801-4, 2 kV			
	RAV 1.25 to 3.5, RAV 2 to 3.5		RAV 1.25 to 4, RAV 2 to 4	
	59 to 88 N·cm (6 to 9 kg·cm)		83 to 113 N·cm (8.5 to 11.5 kg·cm)	
	130 × 55 × 93.6 (5.12 × 2.17 × 3.69)		130 × 54.5 × 93.6 (5.12 × 2.15 × 3.69)	
	0.53 (1.17)	0.55 (1.21)	0.60 (1.32)	

*3: Allowable momentary power interruption time

This value indicates the momentary power interruption time allowed for the PC CPU and varies according to the power supply module used with the PC CPU module. The allowable momentary power interruption time for a system in which an A1S63P is used is defined as starting when the primary power supply of the 24 V DC stabilized power supply of the A1S63P is turned OFF and lasting until the 24 V DC becomes less than the specified voltage (15.6 V DC).

*4: A1S61PEU and A1S62PEU comply with EN61010-1 and safety aspects of IEC-1131-2 to meet the Low Voltage Directive which will be mandatory from the 1st of January 1997.

*5: Do not apply over 400 Voltage between AC and LG as the Varistor is installed between the AC and LG.

(2) Performance specifications for the A1SJHCPU built-in power supply.

Table 5.2 Performance specifications for the A1SJHCPU built -in power supply

Item \ Type	A1SJHCPU
Input power supply	100-120 V AC $^{+10\ \%}_{-15\ \%}$ (85 to 132 V AC) 500-240 V AC $^{+10\ \%}_{-15\ \%}$ (170 to 264 V AC)
Input frequency	50/60 Hz ± 3 Hz
Input voltage distortion factor	Within 5 % (See Section 8.8)
Input maximum apparent power	100 V A
Rush current	20 A 8 msec or less
Rated output	5 V DC 3 A
Overcurrent protection *1	3.3 A or over
Overvoltage protection	Not provided
Efficiency	65 % or over
Power supply indication	POWER LED indicator
Terminal screw size	M3.5 × 8
Applicable solderless terminal	0.3 to 2 mm^2
Applicable solderless terminal	RAV 1.25-3.5, RAV 2-3.5
Allowable momentary power failure	20 msec or less (100 V AC or over)

POINT

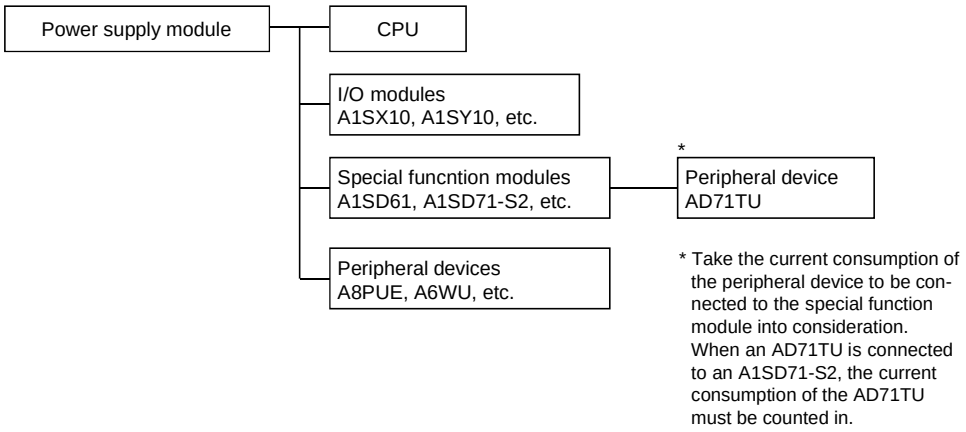
*1 : Overcurrent protection

When a current larger than the specification value flows through the 5 V DC circuit, the overcurrent protection device cuts off the circuit and stops the system.

The POWER LED turns off or lights dimly due to the voltage drop. If this device operated, remove causes of failures such current capacity shortage and short-circuit and restart the system.

5.1.1 Selection of the power supply module

Select the power supply module according to the total current consumption of I/O modules, special function modules and peripheral devices supplied by the power supply module. When an A1S52B(S1), A1S55B(S1), A1S58B(S1), A52B, A55B or A58B is used, the power is supplied from the power supply module of the main base unit. This point should also be taken into consideration.
See Section 2.3 for details of the 5 V DC current consumptions of I/O modules, special function modules, and peripheral devices.



(1) Power supply module when an extension base A1S52B(S1), A1S55B(S1), A1S58B(S1), A52B, A55B or A58B is used.

When an extension base A1S52B(S1), A1S55B(S1), A1S58B(S1), A52B, A55B or A58B is used, the 5 V DC is supplied from the power supply module of the main base unit through the extension cable. Note the following points regarding the use of an extension base from among A1S52B(S1), A1S55B(S1), A1S58B(S1), A52B, A55B and A58B :

(a) Select a power supply module for the main base unit whose 5 V DC capacity can cover the 5 V DC current consumption of the A1S52B(S1), A1S55B(S1), A1S58B(S1), A52B, A55B or A58B.

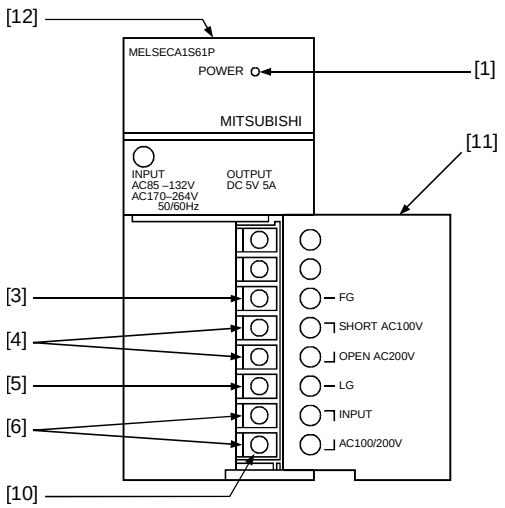
[Example]

When the 5 V DC current consumption by the main base unit is 3 A and that by the A1S55B(S1) is 1 A, the power supply module installed at the main base unit must be A61P (5 V DC, 5 A).

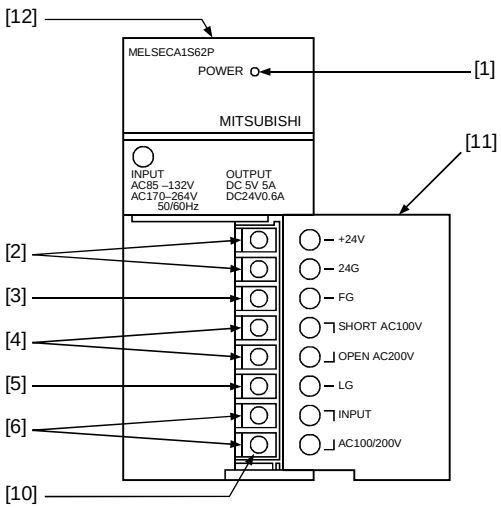
(b) Since the power is supplied to the A1S52B(S1), A1S55B(S1), A1S58B(S1), A52B, A55B or A58B through the extension cable, some voltage drop occurs in the cable. It is necessary to select a power supply module and length of cable which can provide 4.75 V DC or more at the receiving end.
For details of voltage drop and other information, see Section 6.1.3 "Application standards for extension base units".

5.2 Names of Parts and Settings

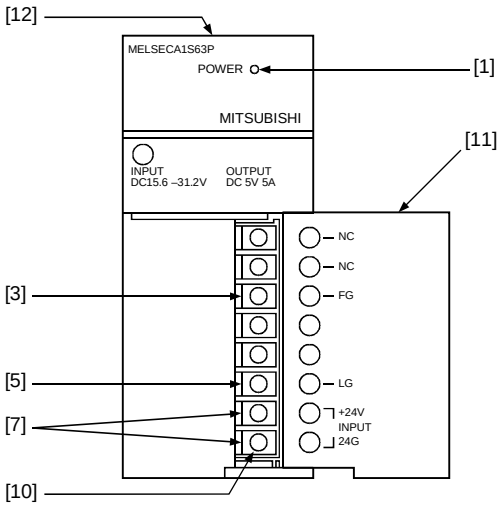
The following gives the names and description of the parts of the power supply modules :



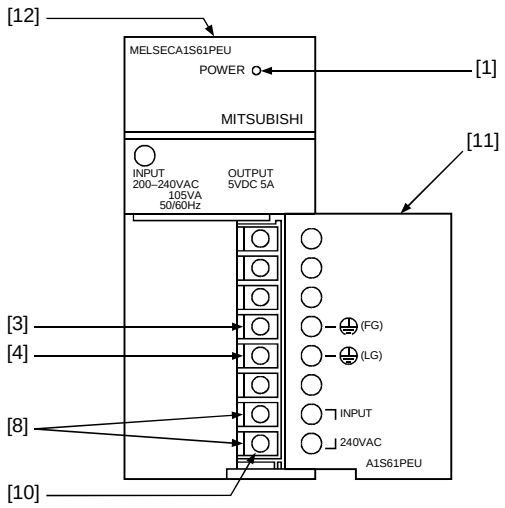
(1) A1S61P



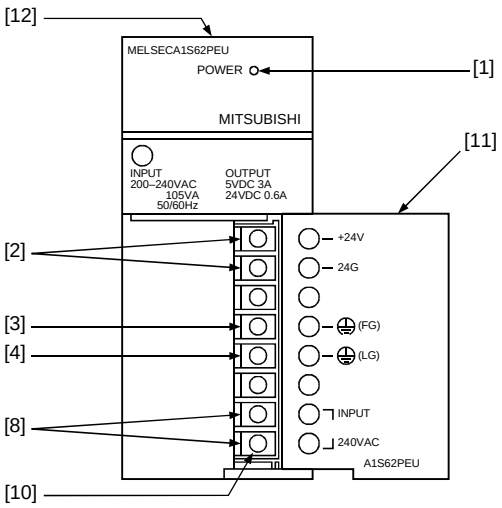
(2) A1S62P



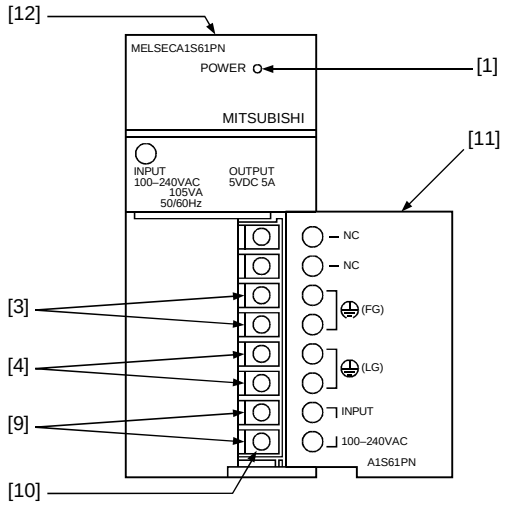
(3) A1S63P



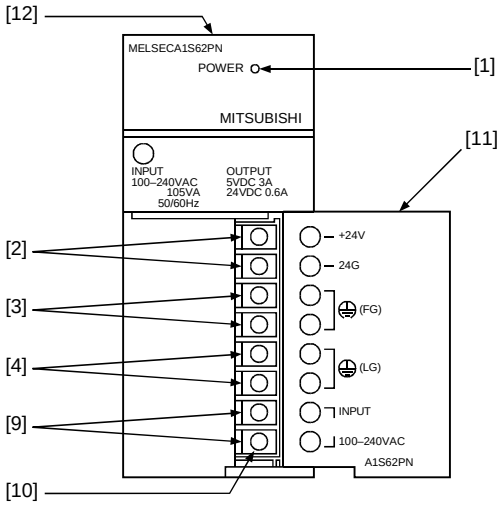
(4) A1S61PEU



(5) A1S62PEU

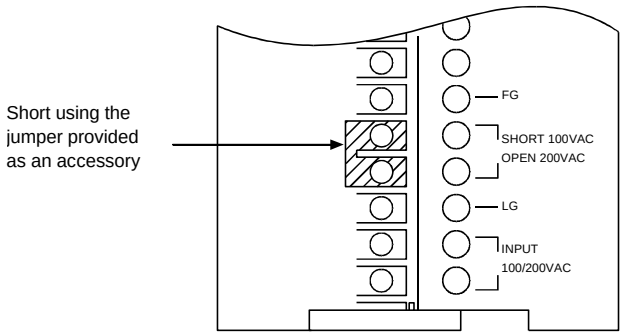


(6) A1S61PN



(7) A1S62PN

No.	Name	Description
[1]	POWER LED	The indicator LED for the 5 V DC power.
[2]	24 V and 24 G terminals	Used to supply 24 V DC to inside the output module (using external wiring).
[3]	FG terminal	The grounding terminal connected to the shield pattern of the printed circuit board.

No.	Name	Description
[4]	Input voltage select terminals	Either a 100 V AC or 200 V AC power supply can be connected: when using 100 V AC, short the two input voltage terminals with the jumper supplied as an accessory; to use 200 V AC, leave these terminals open. The jumper is not attached to the module when shipment. It is packed in a bag together with the module. < Setting when the power supply voltage is 100 V AC > 
[5]	LG terminal	Grounding for the power supply filter. The potential of A1S61P or A1S62P terminal is 1/2 of the input voltage.
[6]	Power supply input terminals	Used to connect a 100 V AC or 200 V AC power supply.
[7]	Power supply input terminals	Used to connect a 24 V DC power supply.
[8]	Power supply input terminals	Used to connect a 200 V AC power supply.
[9]	Power supply input terminals	Used to connect 100 V AC to 200 V AC power supply.
[10]	Terminal screw	M3.5 × 7
[11]	Terminal cover	The protective cover of the terminal block.
[12]	Module fixing screw	Used to fix the module to the base unit. (M4 screw, tightening torque : 59 to 88 N·cm {6 to 9 kg·cm})

POINT

(1) If the setting differs from the supply line voltage, the following results will occur. Do not make the wrong setting.

	Supply line voltage	
	100 V AC	**200 V AC**
Setting to 100 V AC (Short the input voltage select terminals.)	—	The power supply module is damaged. (The CPU is not damaged.)
Setting to 100 V AC (Open the input voltage select terminals.)	No error occurs in the module. However, the CPU does not operate.	—

(2) Do not cable to the unused terminals such as FG and LG on the terminal block (terminals whose name is not printed on the terminal cover).

(3) Be sure to ground the terminal ⏚ LG to the protective ground conductor.

6. BASE UNIT AND EXTENSION CABLE

6.1 Specifications

This section describes the specifications for the base units (main base units, extension base units) that can be used in the system, and the application standards for extension base units.

6.1.1 Specifications of base units

(1) Specifications of main base units

Table 6.1 Main base unit specifications

Item \ Model	A1S32B	A1S33B	A1S35B	A1S38B
Number of I/O modules	2 can be loaded	3 can be loaded	5 can be loaded	8 can be loaded
Extension connection	Enabled			
Installation hole size	ø6-mm (0.24 in.) slot (for M5 screw)			
External dimensions [mm(in.)]	220 × 130 × 28 (8.66 × 5.12 × 1.10)	255 × 130 × 28 (10.04 × 5.12 × 1.10)	325 × 130 × 28 (12.80 × 5.12 × 1.10)	430 × 130 × 28 (16.93 × 5.12 × 1.10)
Weight [kg(lb.)]	0.52 (1.14)	0.65 (1.43)	0.75 (1.65)	0.97 (2.13)
Accessory	Four mounting screws (M5 × 25)			

(2) Specifications of extension base units

Table 6.2 Extension base unit specifications

Item \ Model	A1S65B(S1)	A1S68B(S1)	A1S52B(S1)	A1S55B(S1)	A1S58B(S1)
Number of I/O modules	5 can be loaded	8 can be loaded	2 can be loaded	5 can be loaded	8 can be loaded
Power supply module loading	Required		Not required		
Installation hole size	ø6-mm (0.24 in.) slot (for M5 screw)				
Terminal screw size	—	—	M4 × 6 (FG terminal)		
Applicable wire size	—	—	0.75 to 2 mm^2		
Applicable solderless terminal size	—	—	(V)1.25-4, (V)1.25-YS4, (V)2-YS4A (Applicable tightening torque: 98 to 137 N·cm [10 to 14 kg·cm] (56 to 79 lb/in.)		
External dimensions mm(in.)	315 × 130 × 28 (12.40 × 5.12 × 1.10)	420 × 130 × 28 (16.54 × 5.12 × 1.10)	135 × 130 × 28 (5.31 × 5.12 × 1.10)	260 × 130 × 28 (10.24 × 5.12 × 1.10)	365 × 130 × 28 (14.37 × 5.12 × 1.10)
Weight kg(lb.)	0.71 (1.56)	0.95 (2.09)	0.38 (0.84)	0.61 (1.34)	0.87 (1.91)
Accessory	Four mounting screws (M5 × 25)		*1 One dustproof cover (for I/O module) Four mounting screws (M5 × 25)		

*1: For the installation of the dustproof cover, see Section 8.6.

POINT

When using one of the base units A1S52B(S1), A1S55B(S1) or A1S58B(S1), which do not require a supply module, see Section 5.1.1 "Selection of the power supply module" and Section 6.1.3.

6.1.2 Specifications of extension cables

Table 6.3 shows the specifications of the extension cables which can be used for the AnSHCPU system.

Table 6.3 Extension cable specifications

Item \ Model	A1SC01B	A1SC03B	A1SC07B	A1SC12B	A1SC30B	A1SC60B	A1SC05NB	A1SC07NB	A1SC30NB	A1SC50NB
Cable length [m (ft.)]	0.055 (0.18)	0.33 (1.08)	0.7 (2.3)	1.2 (3.94)	3.0 (9.84)	6.0 (19.68)	0.45 (1.48)	0.7 (2.3)	3.0 (9.84)	5.0 (16.14)
Resistance of 5 V DC supply line (Ω at 55 °C)	0.02	0.02	0.04	0.06	0.12	0.18	0.04	0.05	0.12	0.18
Application	Connection between main base unit and A1S5[ ]B (S1)/A1S6[ ]B (S1)						Connection between main base unit and A5[ ]B/A6[ ]B		Connection between main base unit and A5[ ]B/A6[ ]B	
Weight [kg (lb.)]	0.025 (0.055)	0.01 (0.022)	0.14 (0.31)	0.20 (0.44)	0.40 (0.88)	0.65 (1.43)	0.20 (0.44)	0.22 (0.48)	0.4 (0.88)	0.56 (1.23)

6.1.3 Application standards for extension base units (A1S52B(S1), A1S55B(S1), A1S58B(S1), A52B, A55B, A58B)

When an extension base unit of one of the models A1S52B(S1), A1S55B(S1), A1S58B(S1), A52B, A55B, or A58B is used, make sure a voltage of 4.75 V or higher is supplied to the receiving end (at the module installed in the last slot of the extension base unit).

With the A1S52B(S1), A1S55B(S1), A1S58B(S1), A52B, A55B, and A58B extension base units, 5 V DC is supplied from the power supply module of the main base unit via an extension cable. Therefore, some voltage drop occurs in the extension cable and the specified voltage may not be supplied to the receiving end, resulting in incorrect operation.

If the voltage at the receiving end is less than 4.75 V, use an extension base unit of one of the models A1S65B(S1), A1S68B(S1), A62B, A65B, or A68B, equipped with a power supply module.

(1) Selection conditions

The voltage received by the module installed in the last slot of an A1S52B(S1), A1S55B(S1), A1S58B(S1), A52B, A55B, or A58B extension base unit must be 4.75 V or higher.

Since the output voltage of the power supply module is set at 5.1 V or higher, the voltage drop must be 0.35 V or less.

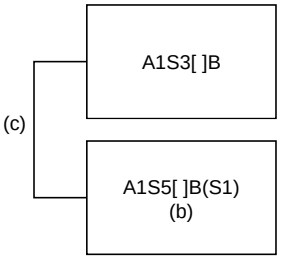
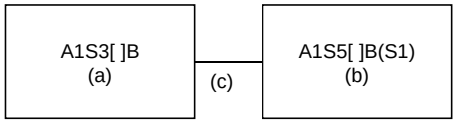
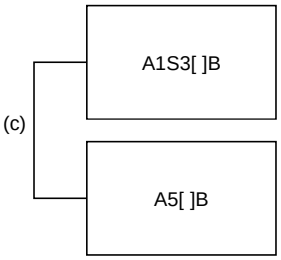
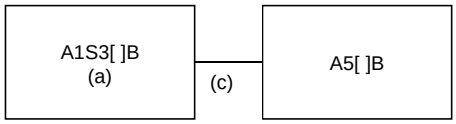
(2) Factors of voltage drop

Voltage drop may involve the following factors (a), (b), and (c) depending on the connecting method and type of extension base units.

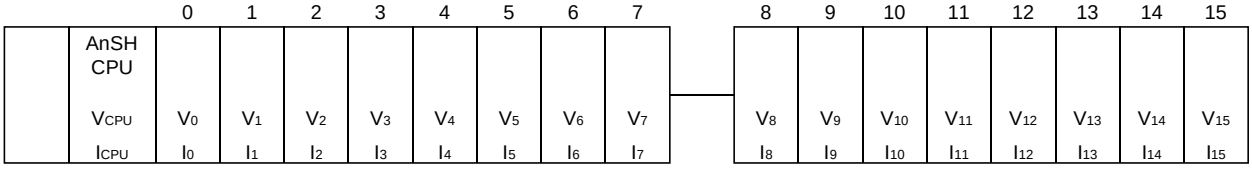
(a) Voltage drop of a main base unit

(b) Voltage drop of an extension base unit

(c) Voltage drop in an extension cable

	Extension cable connected to the left side of main base unit (serial)	Extension cable connected to the right side of main base unit (parallel)
A1S52B(S1), A1S55B(S1), or A1S58B(S1) extension base unit is used	 Voltage drop of the main base unit can be ignored.	
A52B, A55B or A58B extension base unit is used	 Voltage drop of the main and extension base units can be ignored.	 Voltage drop of the extension base units can be ignored.

(3) Calculation of the receiving-end voltage



V_{CPU}, V_0 to V_7 : Voltage drop of each slot of a main base unit
I_{CPU}, I_0 to I_7 : Current consumption of each slot of a main base unit
V_8 to V_{15} : Voltage drop of each slot of an extension base unit
I_8 to I_{15} : Current consumption of each slot of an extension base unit

(a) Calculation of voltage drop of a main base unit (A1S32B, A1S33B, A1S35B, A1S38B)

Each slot of a main base unit has a resistance of 0.007 Ω.
Calculate the voltage drop of each slot, to obtain the total voltage drop of a main base unit.

1) Voltage drop of a CPU module : V_{CPU}

$$V_{CPU} = 0.007 \times (0.4 + I_0 + I_1 + I_2 + I_3 + I_4 + I_5 + I_6 + I_7 + I_8 + I_9 + I_{10} + I_{11} + I_{12} + I_{13} + I_{14} + I_{15})$$

2) Voltage drop of slot 0 : V_0

$$V_0 = 0.007 \times (I_0 + I_1 + I_2 + I_3 + I_4 + I_5 + I_6 + I_7 + I_8 + I_9 + I_{10} + I_{11} + I_{12} + I_{13} + I_{14} + I_{15})$$

3) Voltage drop of slot 1 : V_1

$$V_1 = 0.007 \times (I_1 + I_2 + I_3 + I_4 + I_5 + I_6 + I_7 + I_8 + I_9 + I_{10} + I_{11} + I_{12} + I_{13} + I_{14} + I_{15})$$

4) Voltage drop of slot 2 : V_2

$$V_2 = 0.007 \times (I_2 + I_3 + I_4 + I_5 + I_6 + I_7 + I_8 + I_9 + I_{10} + I_{11} + I_{12} + I_{13} + I_{14} + I_{15})$$

5) Voltage drop of slot 3 : V_3

$$V_3 = 0.007 \times (I_3 + I_4 + I_5 + I_6 + I_7 + I_8 + I_9 + I_{10} + I_{11} + I_{12} + I_{13} + I_{14} + I_{15})$$

6) Voltage drop of slot 4 : V_4

$$V_4 = 0.007 \times (I_4 + I_5 + I_6 + I_7 + I_8 + I_9 + I_{10} + I_{11} + I_{12} + I_{13} + I_{14} + I_{15})$$

7) Voltage drop of slot 5 : V_5

$$V_5 = 0.007 \times (I_5 + I_6 + I_7 + I_8 + I_9 + I_{10} + I_{11} + I_{12} + I_{13} + I_{14} + I_{15})$$

8) Voltage drop of slot 6 : V_6

$$V_6 = 0.007 \times (I_6 + I_7 + I_8 + I_9 + I_{10} + I_{11} + I_{12} + I_{13} + I_{14} + I_{15})$$

9) Voltage drop of slot 7 : V_7

$$V_7 = 0.007 \times (I_7 + I_8 + I_9 + I_{10} + I_{11} + I_{12} + I_{13} + I_{14} + I_{15})$$

10) Total voltage drop of a main base unit : V_K

$$V_K = V_{CPU} + V_0 + V_1 + V_2 + V_3 + V_4 + V_5 + V_6 + V_7)$$

(b) Calculation of voltage drop of an extension base unit (A1S52B(S1), A1S55B(S1), A1S58B(S1))

Each slot of an extension base unit has a resistance of 0.006 Ω. Calculate the voltage drop of each slot, to obtain the total voltage drop of an extension base unit.

1) Voltage drop of slot 8 : V_8

$V_8 = 0.006 \times (I_8 + I_9 + I_{10} + I_{11} + I_{12} + I_{13} + I_{14} + I_{15})$

2) Voltage drop of slot 9 : V_9

$V_9 = 0.006 \times (I_9 + I_{10} + I_{11} + I_{12} + I_{13} + I_{14} + I_{15})$

3) Voltage drop of slot 10 : V_{10}

$V_{10} = 0.006 \times (I_{10} + I_{11} + I_{12} + I_{13} + I_{14} + I_{15})$

4) Voltage drop of slot 11 : V_{11}

$V_{11} = 0.006 \times (I_{11} + I_{12} + I_{13} + I_{14} + I_{15})$

5) Voltage drop of slot 12 : V_{12}

$V_{12} = 0.006 \times (I_{12} + I_{13} + I_{14} + I_{15})$

6) Voltage drop of slot 13 : V_{13}

$V_{13} = 0.006 \times (I_{13} + I_{14} + I_{15})$

7) Voltage drop of slot 14 : V_{14}

$V_{14} = 0.006 \times (I_{14} + I_{15})$

8) Voltage drop of slot 15 : V_{15}

$V_{15} = 0.006 \times I_{15}$

9) Total voltage drop of an extension base unit : V_Z

$V_Z = V_8 + V_9 + V_{10} + V_{11} + V_{12} + V_{13} + V_{14} + V_{15}$

(c) Calculation of voltage drop in extension cables

[1] Total current consumption of an extension base unit : I_Z

$I_Z = I_8 + I_9 + I_{10} + I_{11} + I_{12} + I_{13} + I_{14} + I_{15}$

[2] Voltage drop in an extension cable : V_C

V_C = (Resistance of an extension cable) $\times$ I_Z

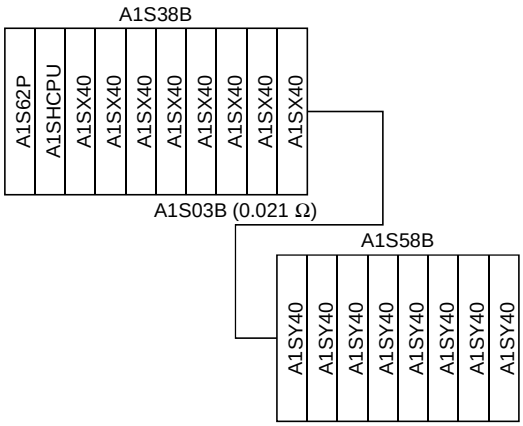
Resistance of extension cables

A1SC01B ····· 0.02 Ω	A1SC30B ····· 0.121 Ω
A1SC03B ····· 0.021 Ω	A1SC60B ····· 0.182 Ω
A1SC07B ····· 0.036 Ω	A1SC05NB ··· 0.037 Ω
A1SC12B ····· 0.055 Ω	A1SC07NB ··· 0.045 Ω

(d) Voltage at the receiving end

$(5.1\ (V) - VK - VZ - VC) \geq 4.75\ (V)$

(4) Examples



(a) Calculation of voltage drop of the main base unit

$VK = 0.007 \times \{0.4 + 0.05 \times (8 + 7 + 6 + 5 + 4 + 3 + 2 + 1) + (0.27 \times 8) \times 8\} = 0.13636$

(b) Calculation of voltage drop of the extension base unit

$VZ = 0.006 \times 0.27 \times (8 + 7 + 6 + 5 + 4 + 3 + 2 + 1) = 0.05832$

(c) Calculation of voltage drop in the extension cable

$VC = 0.036 \times (0.27 \times 8) = 0.07776$

(d) Voltage at the receiving end

5.1 - 0.13636 - 0.05832 - 0.07776 = 4.82756 (V)

Since the voltage at the receiving end is more than 4.75 V, the system can be put into operation.

(5) Minimizing the voltage drop

Try the following measures to minimize the voltage drop :

(a) Change the positions of modules.

Install the modules of the main base unit from slot 0 in descending order of current consumption. Install modules with small current consumption in the extension base units.

(b) Connect the base units in series.

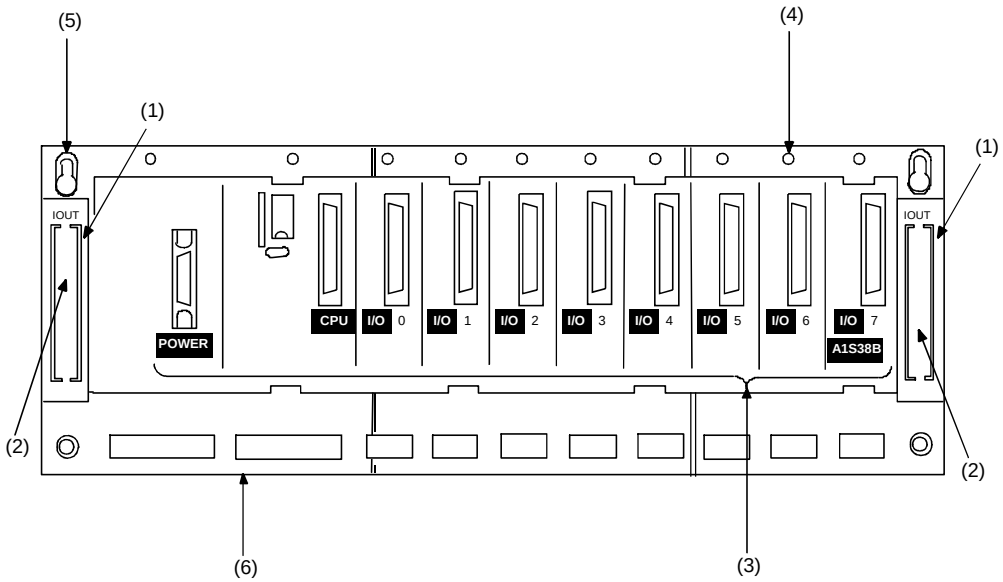
By connecting the base units in series (connecting an extension cable to the left side of a main base unit, see Section 8.4.2), the voltage drop of the main base unit can be minimized. But when a long extension cable is used for this connection, the extension cable may cause a larger voltage drop than that of the main base unit. In such case, calculate the voltage drop as described in (3).

(c) Use a short extension cable.

The shorter the extension cable, the lower and the smaller its voltage drops. Use extension cables that are as short as possible.

6.2 Nomenclature and Settings

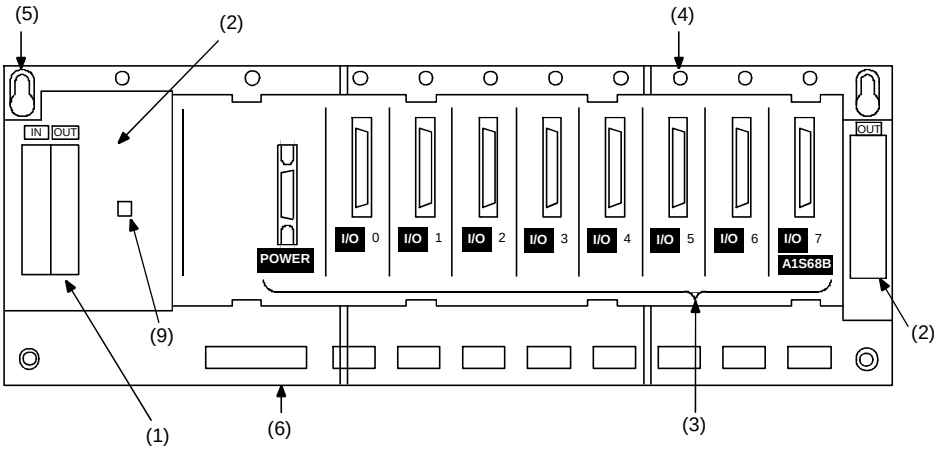
(1) Main base unit (A1S32B, A1S35B, A1S38B)



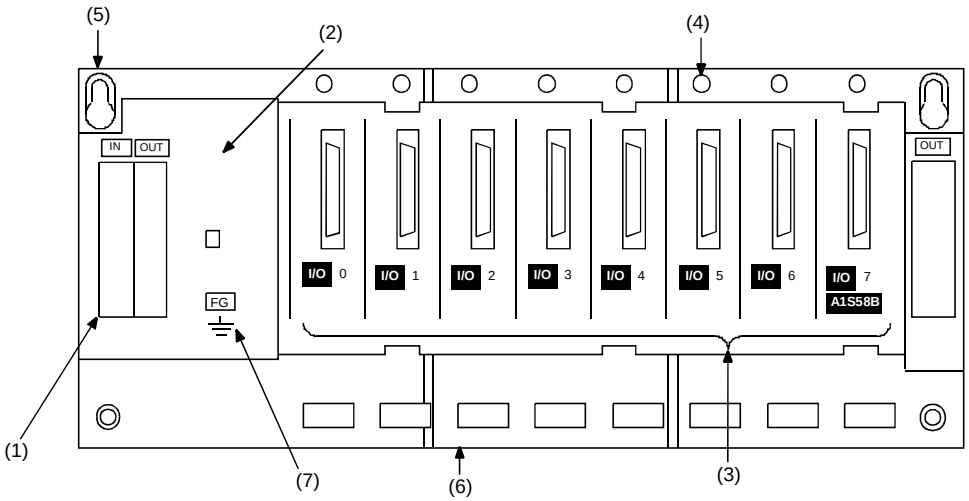
No.	Name	Application
(1)	Connector for extension cable	Connector for sending and receiving signals to and from the extension base unit.
(2)	Base cover	Cover to protect the connector for the extension cable. When connecting an extension cable, remove the appropriate base cover located below the word "OUT" with nippers or a similar tool.
(3)	Module connectors	Connectors where the power supply module, CPU module, I/O module, special function modules are loaded. Fit the connector cover or blank cover (A1SG60) to vacant connectors, in order to protect the module from dust.
(4)	Module fixing screw	Screw to fix a module to the base unit. Screw size : M4 × 12 screw
(5)	Guide hole for base installation	Slot for mounting this base unit to the panel of control box, etc. (For M5 screw)
(6)	DIN rail hook	Hook to install on a DIN rail. A1S32B, A1S33B·····1 A1S35B, A1S38B·····2

(2) Main base modules (A1S52B(S1), A1S55B(S1), A1S58B(S1), A1S65B(S1), A1S68B(S1))

A1S65B (S1), A1S68B (S1)



A1S52B (S1), A1S55B (S1), A1S58B (S1)



No.	Name	Purpose
(1)	Extension cable connector	Used to connect an extension cable to a main base module. Remove the connector cover attached to the module and connect the extension cable.
(2)	Base cover	Extension cable connector protective cover.
(3)	Module connector	Used to load a power supply module, I/O or special function module. Put a supplied cover or blank cover (A1SG60) on any unused connector to protect it from dust.
(4)	Module fixing screw	Used to secure a module to the base module. Screw size : M4 × 12
(5)	Base mounting hole	Used to mount the base module to a control panel. (for M5 screw)
(6)	DIN rail hook	Used to install on a DIN rail. A1S52B(S1), A1S55B(S1) : One hook A1S65B(S1), A1S68B(S1), A1S58B(S1) : Two hooks
(7)	FG terminal	Grounding terminal connected to the shield pattern on the PC board.

6.3 Installing on a DIN Rail

Both main base units and extension base units are equipped with hooks for mounting on a DIN rail.

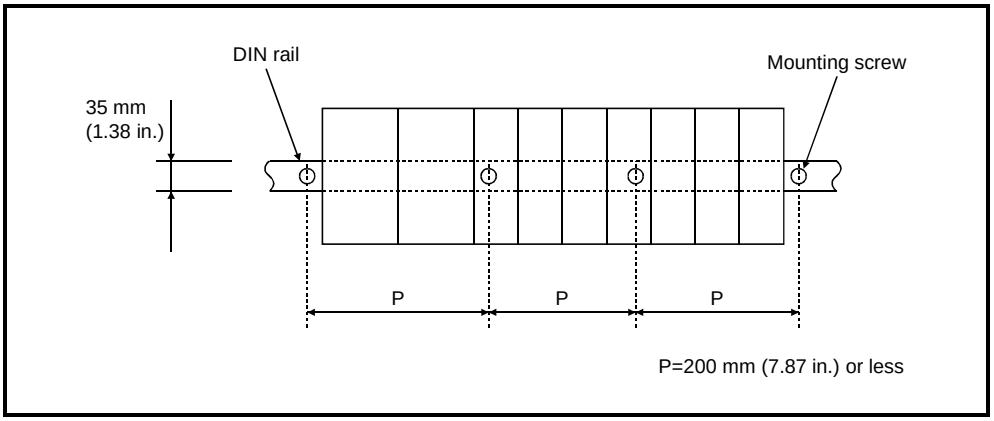
The method for mounting them on a DIN rail is explained below :

(1) Applicable DIN rails (JIS-C2B12)

TH35-7.5 Fe
TH35-7.5 Al
TH35-15 Fe

(2) Mounting screw interval

When a TH35-7.5 Fe or TH35-7.5 Al rail is mounted, fix it with screws spaced no more than 200 mm (7.87 in.) apart.



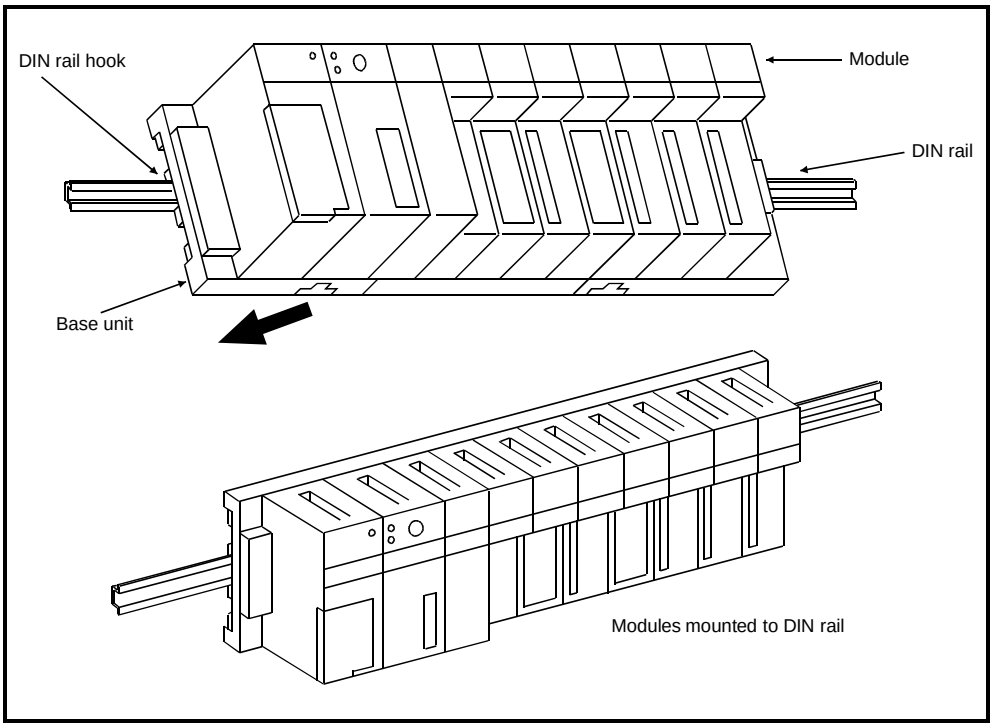
(3) Mounting/removing on/from a DIN rail

(a) Mounting procedure

Mount a base unit on a DIN rail as follows :

1) Engage the hook of the base unit with the rail from above rail.

2) Push the base unit onto the rail and fix it in position.

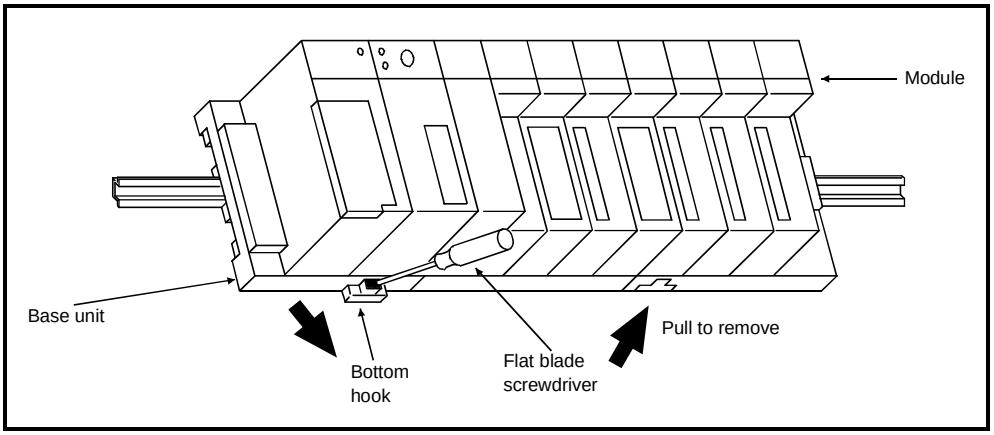


(b) Removing procedure

Remove a base unit from the DIN rail as follows :

1) Pull down the bottom hook of the base unit using a flat blade screwdriver.

2) Pull the base unit away from the rail while pulling down the bottom hook.



7. MEMORY ICs AND BATTERY

7.1 Memory ICs

This section describes the specifications, handling instructions and installation of the memory ICs used in the AnSHCPU.

7.1.1 Specifications

Table 7.1 and 7.2 show the specifications of the ROMs.

Table 7.1 Memory specifications (A1SHCPU)

Item \ Model	New memory cassette			Conventional memory cassette		
	A1SNMCA-2KE	A1SNMCA-8KE	A1SNMCA-8KP	A1SMCA-2KE	A1SMCA-8KE	A1SMCA-8KP
Memory specifications	E^2PROM		EPEOM	E^2PROM		EPEOM
Memory capacity	8 k bytes (max. 2 k steps)	32 k bytes (max. 8 k steps)	32 k bytes (max. 8 k steps)	8 k bytes (max. 2 k steps)	32 k bytes (max. 8 k steps)	32 k bytes (max. 8 k steps)
E^2PROM service life for writing	10000 times	100000 times	—	10000 times	100000 times	—
Outside dimension [mm (in.)]	15 × 69.6 × 40.5 (0.59 × 2.75 × 1.59)			15 × 68.6 × 42 (0.59 × 2.70 × 1.65)		
Weight [kg (lb.)]	0.03 (0.06)					
A1SHCPU	ϒ	ϒ	ϒ	×	×	×
A1SJHCPU	ϒ	ϒ	ϒ	ϒ	ϒ	ϒ

Table 7.2 Memory specifications (A2SHCPU)

Item \ Model	New memory cassette	Conventional memory cassette	
	A2SNMCA-30KE	A2SMCA-14KE	A2SMCA-14KP
Memory specifications	E^2PROM	E^2PROM	EPROM
Memory capacity	64 k bytes A2SHCPU : (max. 14 k steps) A2SHCPU-S1 : (max. 30 k steps)	64 k bytes (max. 14 k steps)	64 k bytes (max. 14 k steps)
E^2PROM service life for writing	100000 times		—
Outside dimension [mm (in.)]	15 × 69.6 × 40.5 (0.59 × 2.75 × 1.59)	15 × 68.6 × 42 (0.59 × 2.70 × 1.65)	
Weight [kg (lb.)]	0.03 (0.06)		
A2SHCPU (S1)	ϒ	×	×

7.1.2 Handling instructions

(1) Handle memory cassettes and pin connectors with care since their plastic bodies cannot resist strong impacts.

(2) Do not remove the printed circuit board from its enclosure.

(3) Take care not to let chips of wires and other foreign material enter the memory cassette.

(4) When installing a memory cassette in an AnSHCPU module, push it in so that the connectors engage securely.

(5) Never place a memory cassette on metal, which may allow current flow, or on an object which is charged with static electricity, such as wood, plastic, vinyl, fiber, cable or paper.

(6) Do not touch or bend the leads of memory chips.

(7) Do not touch the connectors of a memory cassette. This could cause insecure contact.

IMPORTANT

(1) Always turn OFF the power to an AnSHCPU module when installing or removing a memory cassette. If a memory cassette is installed or removed with the power to the CPU ON, the data contents of the memory may be destroyed while the AnSCPU power is live.

(2) If the power is turned ON when the memory cassette is installed, the program in the built-in RAM memory of the AnSHCPU is overwritten by that of the memory cassette.
If the program in the RAM memory needs to be saved, install the memory cassette after making a backup of the program by using a programming device.

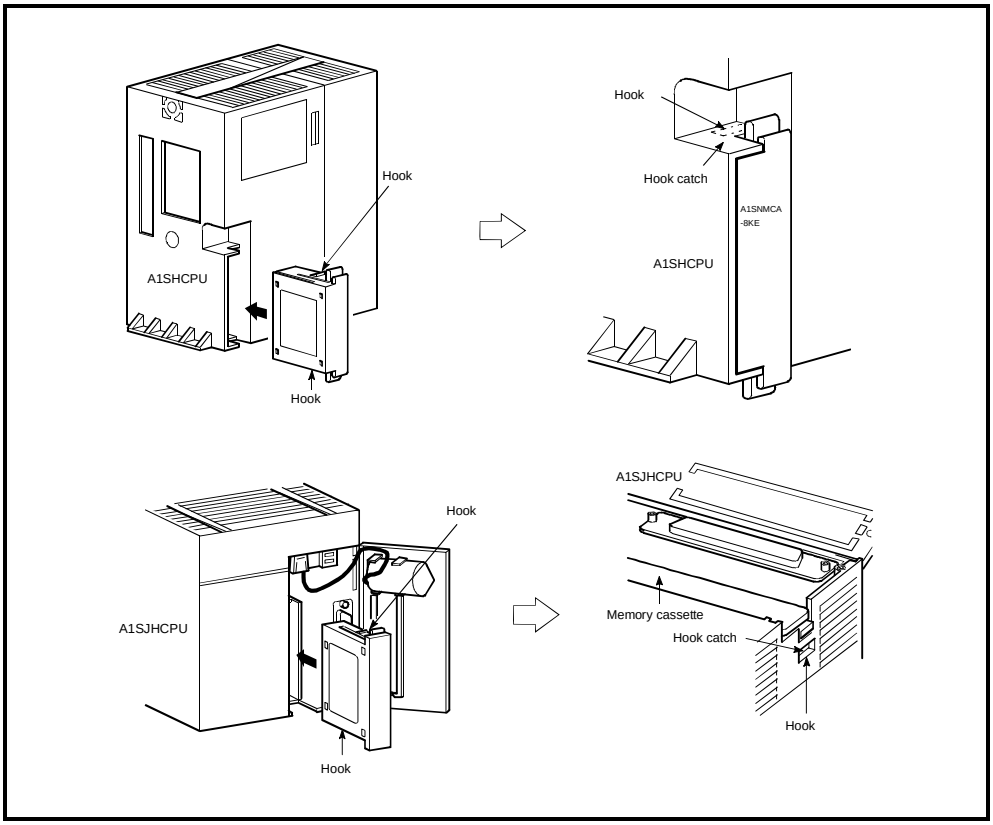
7.1.3 Installing and removing a memory cassette

The installation/removal method of the memory cassette is common in all AnSHCPU models, but the installation position is unique to each model.

Memory cassette installation position: A1SHCPU/A2SHCPU(-S1) ----- Left side

A1SJHCPU --- Front

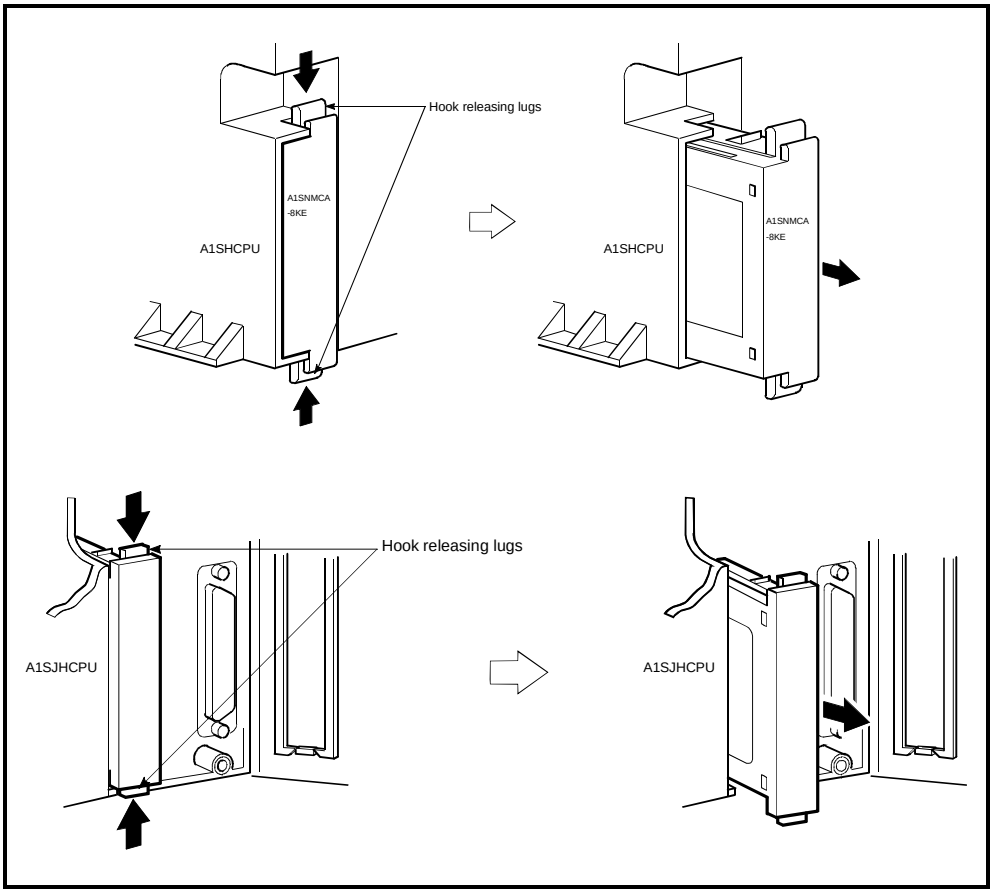
(1) Installing a memory cassette



(a) Hold the memory cassette vertically so that its model name is right side up and its connector faces the AnSHCPU module. Insert the memory cassette all the way in the AnSHCPU module so that the hooks of the memory cassette are completely engaged (they will click).

(b) Make sure the hooks are completely engaged.

(2) Removing a memory cassette



(a) Pull out the memory cassette while pushing the hook releasing lugs that are provided at the top and the bottom of the memory cassette.

7.1.4 Writing a sequence program to a memory cassette

A sequence program can be written to, or erased from, an A1SMCA-8KP or A1SNMCA-8KP using a ROM writer/eraser.

If a memory cassette is installed in the ROM socket of an A6GPP or A6WU, use either of the following memory write adapters.

CPU model	Memory cassette model	Memory write adapter
A1SHCPU	A1SNMCA-8KP	A6WA-28P
A1SJH/A1SHCPU	A1SMCA-8KP, A1SNMCA-8KP	A6WA-28P

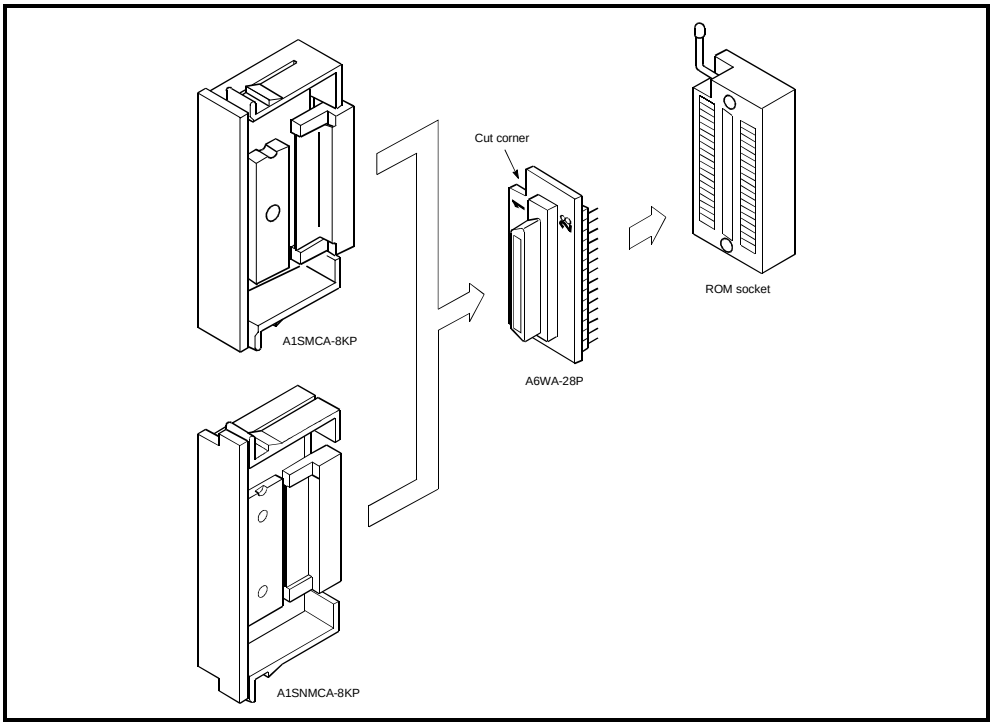
POINT

(1) When writing to an A1SHCPU/A1SJHCPU using an A6WU series P-ROM writer module, SERIAL must be selected.

(2) The start-up file type name will need to be changed when using a SW♦GP-GPPA ROM writer/eraser on an A1SHCPU/A1SJHCPU.
Set "A0J2H" for Version Q or earlier; "A1S" for Version R or later. Then select SERIAL.
In addition, it will be necessary to select "27256" for ROM setting type.

(1) Mount a memory cassette to the memory write adapter. Couple the connectors correctly.

(2) Mount the memory write adapter coupled with the memory cassette to the ROM socket of an A6GPP or A6WU in the correct orientation. The pin on the cut corner side of the memory write adapter is pin No.1.

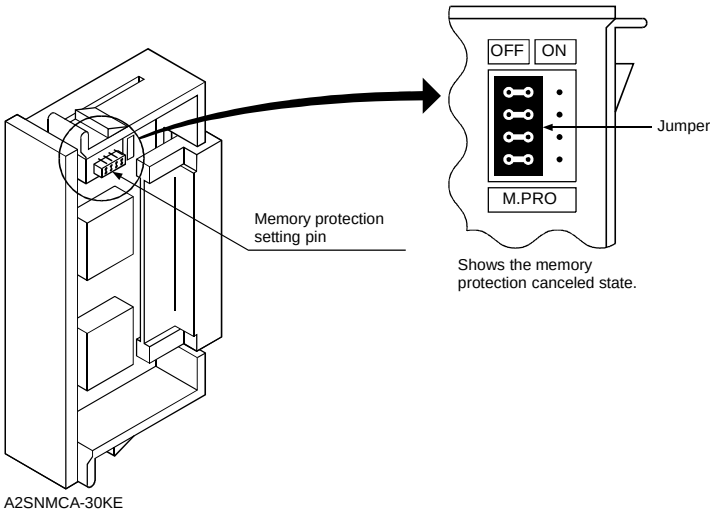


7.1.5 Memory write-protect setting for an A2SNMCA-30KE

When an A2SNMCA-30KE is installed on an A2SHCPU, misuse of peripheral devices can cause the E^2PROM memory to be over-written. In order to prevent this from occurring, the A2SNMCA-30KE has been provided with a memory write-protect setting.

When the memory write-protect setting pin is in the ON position, all 64 k bytes of the user memory area will be protected.

The memory write-protect setting pin must be moved to the OFF position in order to allow the contents of the ROM memory to be corrected.
The pin is set to the OFF position before shipment from the factory.
See Section 4.1.9 regarding memory area allocation.



7.2 Battery

This section describes the specifications, handling instructions, and installation procedure for the battery.

7.2.1 Specifications

Table 7.3 shows specifications of the battery used to retain the data stored in memory when a power interruption occurs.

Table 7.3 Battery specifications

Item \ Model	A6BAT
Normal voltage	3.6 V DC
Guaranteed life	5 years
Application	For IC-RAM memory backup and power interruption compensation function
External dimensions [mm (in.)]	ϕ16 (0.63) $\times$ 30 (1.18)

7.2.2 Handling instructions

(1) Do not short circuit.

(2) Do not disassemble.

(3) Do not expose to naked flame.

(4) Do not heat.

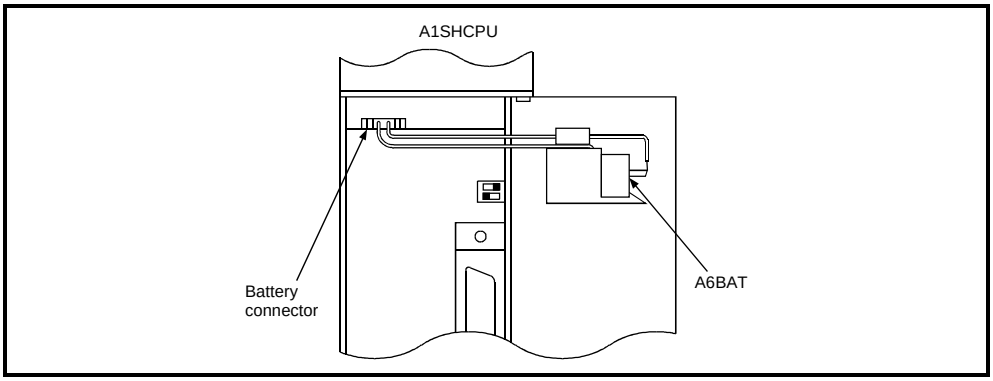
(5) Do not solder the battery terminals.

7.2.3 Installation

The battery lead connector is disconnected from the battery connector on the AnSHCPU board to prevent discharge during transportation and storage.

Before starting the AnSHCPU, plug the battery connector into the battery connector on the AnSHCPU board.

- To use a sequence program stored in the user program area in the AnSHCPU if a power interruption occurs.
- To retain the data if a power interruption occurs.



8. LOADING AND INSTALLATION

This chapter describes the procedure for loading and installation and gives relevant precautions to ensure that the system performs with high reliability and that its functions are used to best effect.

8.1 Safety Consideration

When the power to the system is turned ON or OFF, the process output may not perform normally at times due to the difference between the delay time and the rise time of the power supply of the PC CPU main module and the external power supply (especially DC). Also, if there is an error in the external power supply, the output process may malfunction.

For example, if the power supply to the PC is switched on after switching on the external power supply for the sequence program operation at a DC output module, the DC output module may temporarily output erroneous signals when the power to the PC is switched on. A circuit that allows the power to the PC to be switched on first must therefore be provided.

In addition, if there is an abnormality in the external power supply or trouble in the PC, this could cause malfunction.

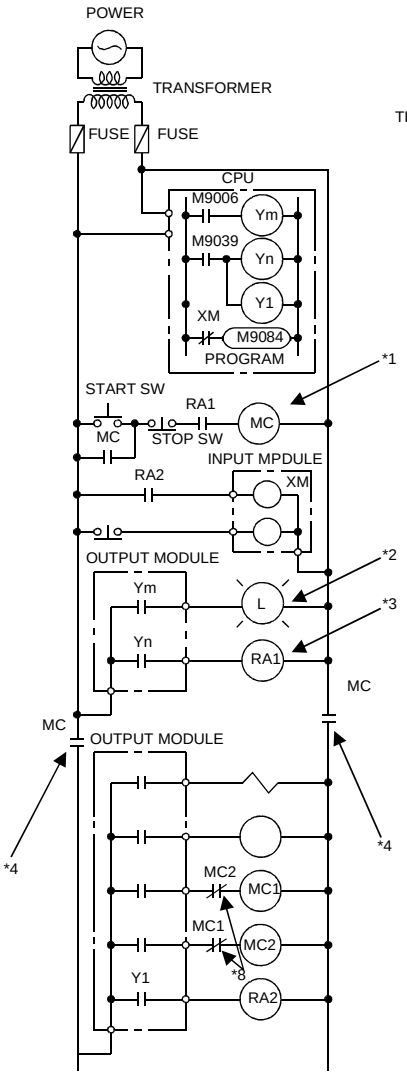
To (a) prevent erroneous operation of the entire system, and (b) ensure safety, prepare circuits (such as an emergency stop circuit, protection circuit, and interlock circuit) that prevent machine damage and/or accidents due to erroneous operation of peripheral devices. An example system design circuit based on this concept is shown on the following page.

POINT

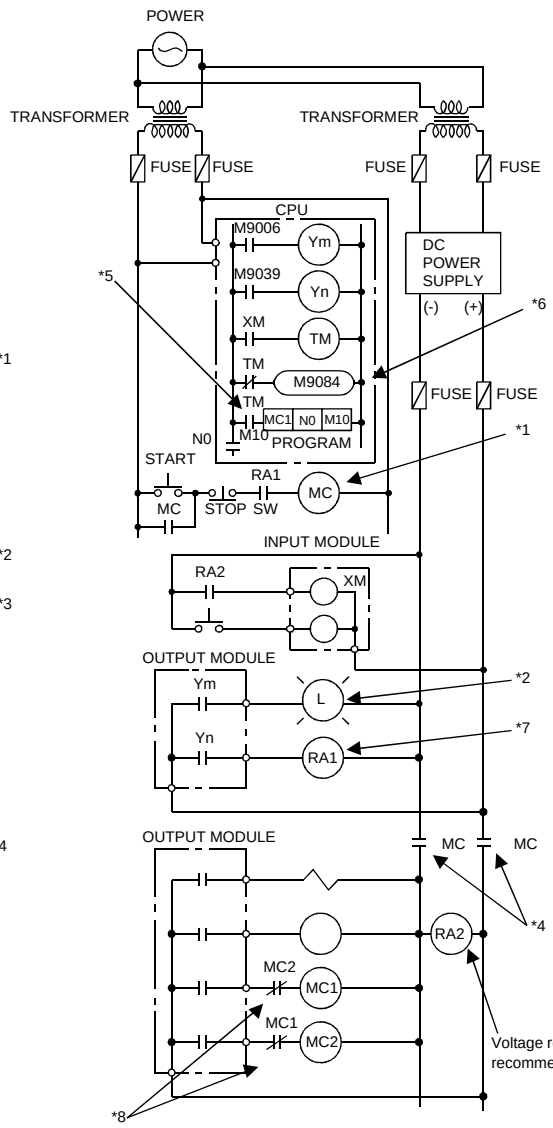
Some types of AnS series output module detect a blown fuse error as soon as the external power supply is turned OFF.
In the example circuit illustrated on the next page, since the start-up of the AnSHCPU takes place earlier than the rise of the external power supply to the output module, a blown fuse error is detected.
To solve this problem, the system is designed to keep the M9084 ON until the external power supply rises so as not to check for blown fuses.
(When M9084 is ON, the I/O module comparison and battery checks are not performed.)

(1) System design circuit example

ALL AC



Mixed AC and DC



*1 : RUN/STOP circuit interlocked with RA1 (run monitor relay)
*2 : Low battery alarm
*3 : RA1 switched ON by M9039 (run monitor relay)
*4 : Power to output equipment switched OFF when the STOP signal is given.
*5 : Input switched when power supply established.
*6 : Set time for DC power supply to be established.
*7 : ON when run by M9039
*8 : Interlock circuits as necessary.

The power-ON procedure is as follows :

For AC

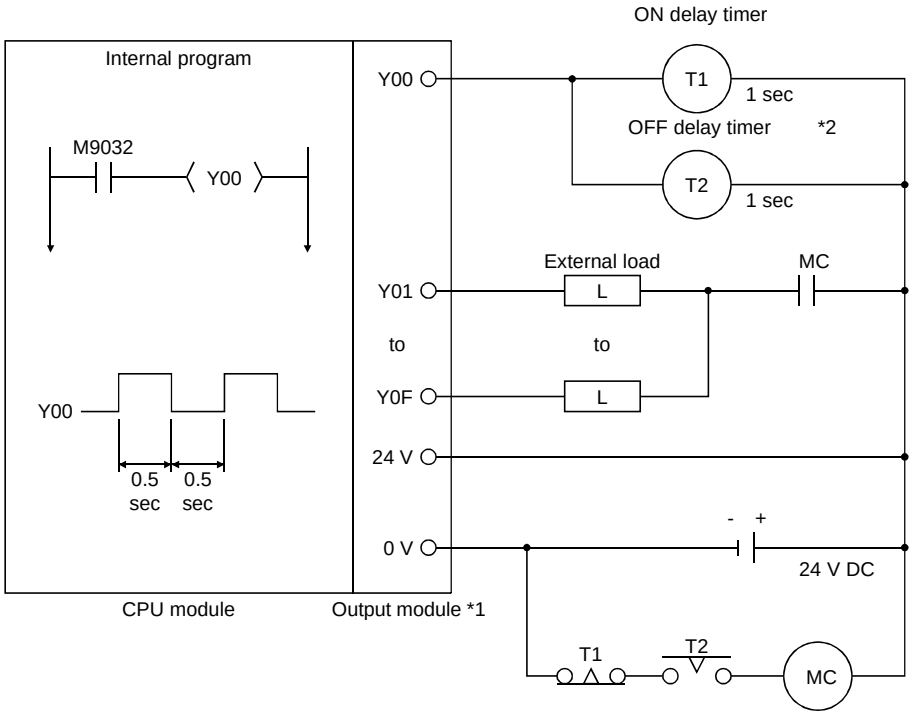
1) Set the CPU to RUN.
2) Switch ON the power.
3) Turn ON the start switch.
4) When the magnetic contactor (MC) comes in, the output equipment is powered and may be driven by the program.

For AC/DC

1) Set the CPU to RUN.
2) Switch ON the power.
3) Turn ON the start switch.
4) When DC power is established, RA2 comes ON.
5) Timer (TM) times out after the DC power reaches 100 %. (The TM set value should be the period of time from when RA2 comes ON to the establishment of 100 % DC voltage. Set this value to approximately 0.5 seconds.)
6) When the magnetic contactor (MC) comes in, the output equipment is powered and may be driven by the program. (If a voltage relay is used at RA2, no timer (TM) is required in the program.)

(2) Fail-safe measures against PC failures

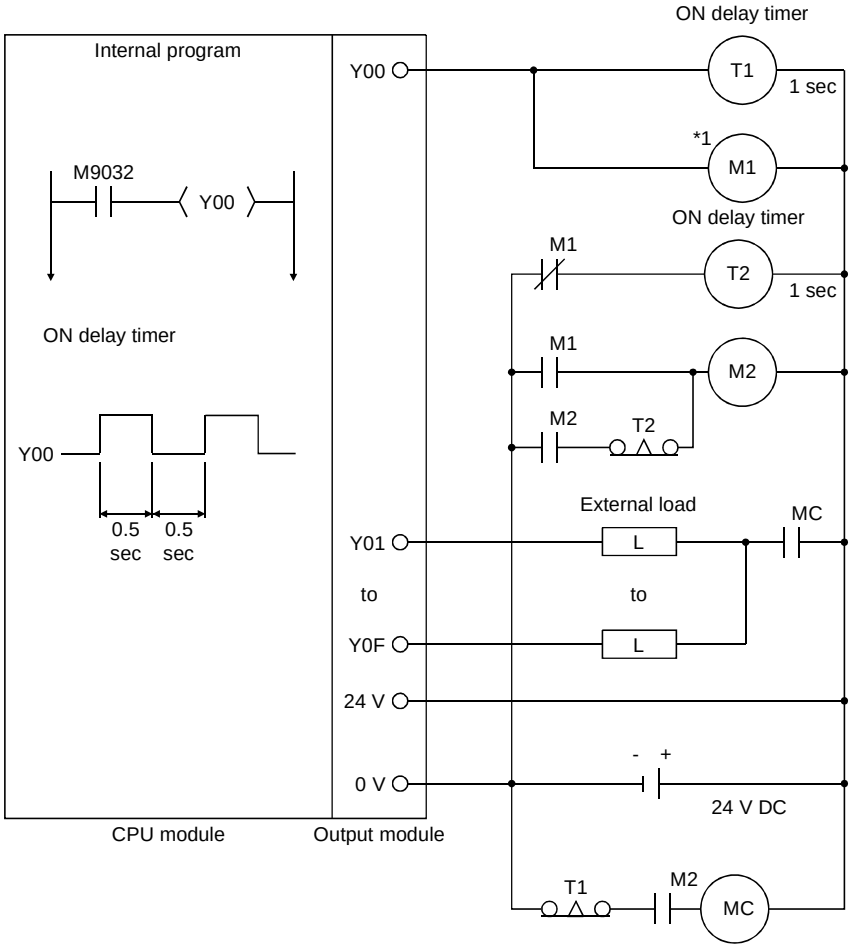
Problems with the CPU or memory can be detected by the self-diagnosis function. However, problems with the I/O control area may not be detected by the CPU.
If such a problem arises, all I/O points turn ON or OFF depending on the nature of the problem, and it may not be possible to maintain normal operating conditions and operating safety.
Although Mitsubishi PCs are manufactured under strict quality control, they may fail or operate abnormally due to unspecifiable reasons. To prevent the abnormal operation of the whole system, machine breakdown, and accidents, build a fail-safe circuit outside the PC.
The following is an example of a fail-safe circuit.



*1 : Y00 repeats turning ON and then OFF at 0.5 second intervals. Use a no-contact output module (transistor in the example shown above).

*2 : If an OFF delay timer (especially a miniature timer) is not available, use ON delay timers to make a fail-safe circuit as shown on the next page.

A fail-safe circuit built with ON delay timers



*1 : Use a solid-state relay for the M1 relay.

8.2 Installation Environment

Never install the AnSHCPU system in the following environments :

(1) Locations where the ambient temperature is outside the range of 0 to 55 °C.

(2) Locations where the ambient humidity is outside the range of 10 to 90 % RH.

(3) Locations where dew condensation takes place due to sudden temperature changes.

(4) Locations where there are corrosive and/or combustible gasses.

(5) Locations where there is a high level of conductive powder (such as dust and iron filings, oil mist, salt, and organic solvents).

(6) Locations exposed to the direct rays of the sun.

(7) Locations where strong power and magnetic fields are generated.

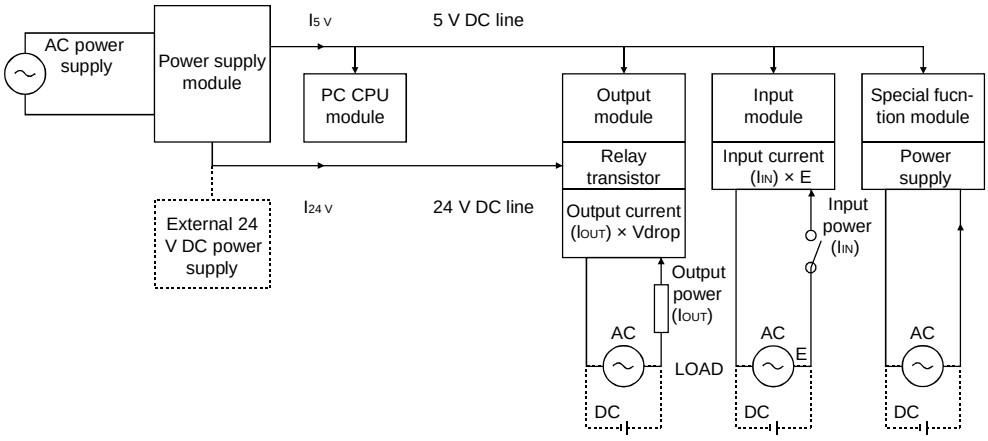
(8) Locations where vibration and shock are directly transmitted to the main module.

8.3 Calculation of Heat Generated by the Programmable Controller System

The operating ambient temperature of the PC must be kept below 55 °C. In order to plan a heat dissipating design for the panel that houses the equipment, the average power consumption (heat generation) of the devices and equipment housed in the panel must be known. Therefore, the method for determining the average power consumption of an AnSHCPU system is described here. Calculate the temperature rise inside the panel from the power consumption.

Average power consumption

Power is consumed by the following PC areas :



(1) Power consumption of a power supply module

Approximately 70 % of the power supply module current is converted into power and 30 % of that 70 % is dissipated as heat, i.e., 3/7 of the output power is actually used.

$$Wpw = \frac{3}{7} \{(I_{5V} \times 5) + (I_{24V} \times 24)\} (W)$$

Where, I_{5V} = V DC logic circuit current consumption of each module.
I_{24V} = current consumption of the output modules (with an average number of points switched ON) ...(Not for 24 V DC input power supply modules)

(2) Total 5 V DC power consumption

5 V DC is supplied to each module via the base plate, which powers the logic circuitry.

$W_{5V} = I_{5V} \times 5 (W)$

(3) Total 24 V DC output module power consumption (with an average number of points switched ON)

24 V DC is supplied to drive output devices.

$W_{24V} = I_{24V} \times 24 (W)$

(4) Power consumption of output circuits (with an average number of points switched ON)

$W_{OUT} = I_{OUT} \times Vdrop \times$ average number of outputs on at one time (W)

Where, I_{OUT} = output current (actual operating current) (A)
Vdrop = voltage dropped across each output load (V)

(5) Power consumption of input circuits (with an average number of points switched ON)

$W_{IN} = I_{IN} \times E \times$ average number of inputs on at one time (W)

Where, I_{IN} = input current (effective value for AC) (A)
E = input voltage (actual operating voltage) (V)

(6) Power consumption of the special function module power supply is expressed as :

$Ws = I_{5V} \times 5 + I_{24V} \times 24 + I_{100V} \times 100$ (W)

The sum of the above values is the power consumption of the entire PC system.

$W = W_{PW} + W_{5V} + W_{24V} + W_{OUT} + W_{IN} + W_S$ (W)

Further calculations are necessary to work out the power dissipated by the other equipment in the panel.

Generally, the temperature rise in the panel is expressed as :

$$T = \frac{W}{UA} \ (^{\circ}C)$$

Where, W = power consumption of the entire PC system (obtained as shown above)

A = panel inside surface area (m^2)

U = 6 (if the panel temperature is controlled by a fan, etc.)
4 (if the panel air is not circulated)

POINT

If the temperature rise inside the panel exceeds the stipulated range, you are recommended to install a heat exchanger in the panel to lower the temperature.

If an ordinary ventilation fan is used, dust will be sucked in along with the air from outside the panel and this may affect the performance of the PC.

8.4 Module Mounting

This section gives the mounting instructions for the main base unit and extension base units.

8.4.1 Mounting instructions

The instructions for mounting the PC to a panel, etc. are presented below :

(1) To improve ventilation and facilitate the replacement of the module, provide 30 mm (1.18 in.) or more of clearance around the PC.

However, when an extension base unit of one of models A52B, A55B, A58B, A62B, A65B, and A68B is used, allow a clearance of 80 mm (3.15 in.) or more between the top face of the module and the surface of a structure or component.

(2) Do not mount the base unit vertically or horizontally since this will obstruct ventilation.

(3) Ensure that the base unit mounting surface is uniform to prevent strain. If excessive force is applied to the printed circuit boards, this will result in incorrect operation. Therefore, mount the base unit on a flat surface.

(4) Avoid mounting the base unit close to vibration sources, such as large magnetic contactors and no-fuse breakers, install the base unit in another panel or distance the base unit from the vibration source.

(5) Provide a wiring duct as necessary.

However, if the dimensions from the top and bottom of the PC are less than those shown in Fig. 8.1, note the following points :

(a) When the duct is located above the PC, the height of the duct should be 50 mm (1.97 in.) or less to allow for sufficient ventilation.

Between the duct and the top of the PC, provide a sufficient distance to allow the cable to be removed by opening the cable connector fixing the lever.

If the lever at the top of the module cannot be opened, it will not be possible to replace the module.

(b) If a duct is built under the PC, provide a clearance between the bottom surface of the PC and the surface of the duct so that the input power cable (100/200 V AC) of the power supply module and the I/O cables and the cable for 12/24 V DC of I/O modules are not affected or bent.

(6) If an equipment which generates noise or heat is positioned in front of the PC (i.e, mounted on the back side of a panel door), allow a clearance of 100 mm (3.94 in.) or more between the PC and the equipment.

Also allow a clearance of 50 mm (1.97 in.) or more between the right/left side of a base unit and this equipment.

8.4.2 Installation

This section explains how to mount main and extension base units.

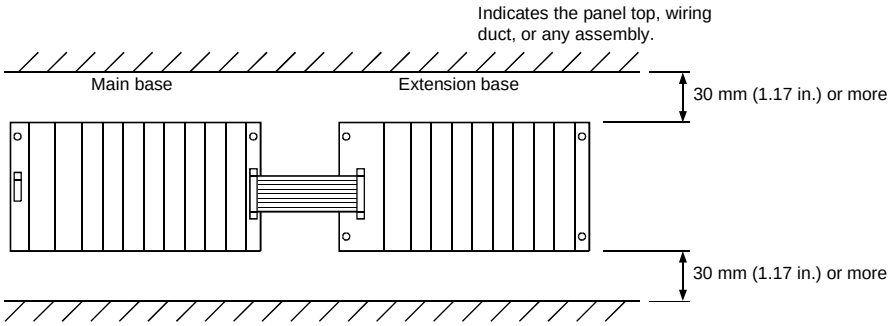


Fig. 8.1 Parallel mounting

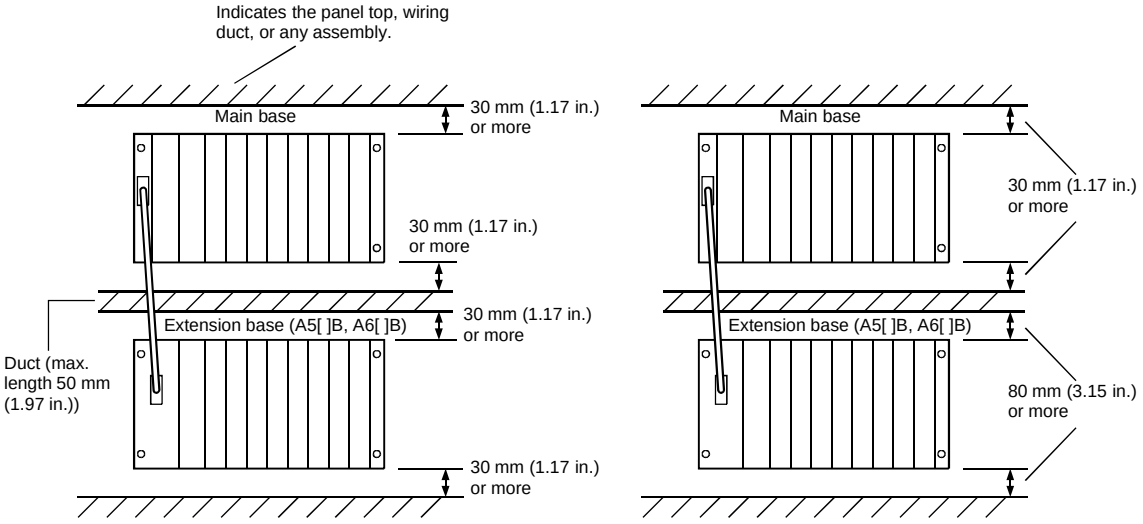


Fig. 8.2 Serial mounting

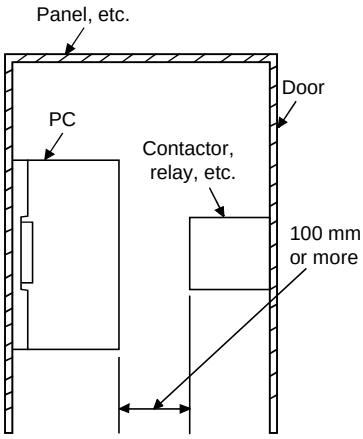


Fig. 8.3 Minimum front clearance with panel door

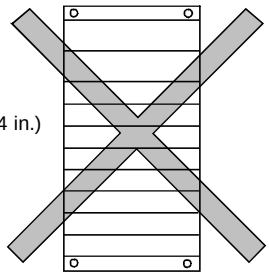


Fig. 8.4 Vertical mounting (not allowed)

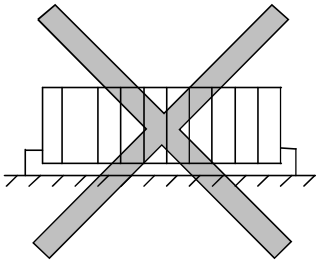


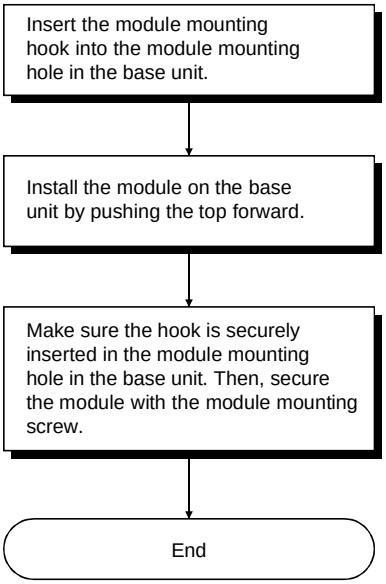
Fig. 8.5 horizontal mounting (not allowed)

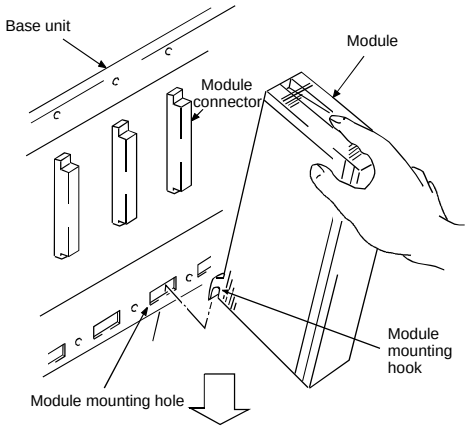
8.5 Installation and Removal of Module

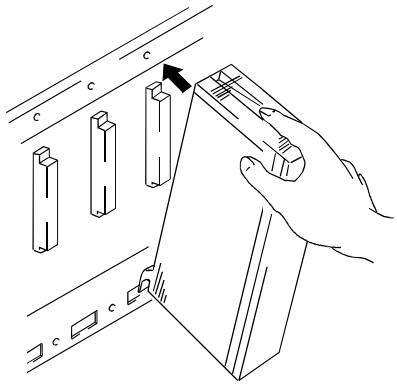
This section explains the mounting and removal of the I/O module and special function module, etc., to and from the base module.

(1) Module mounting

The module mounting procedure is as follows.



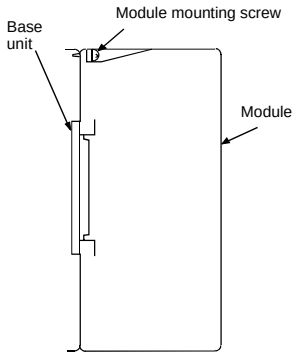




POINT

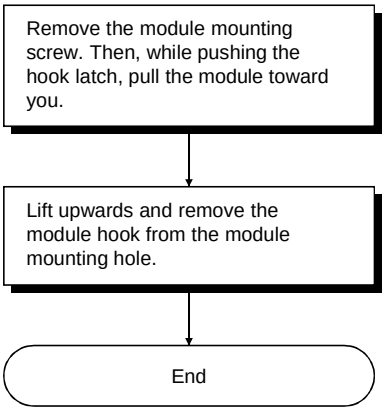
(1) When securing the module, be sure to insert the module mounting hook into the module mounting hole. If the module is forcibly secured without insertion, the module's connector or the module itself may be damaged.

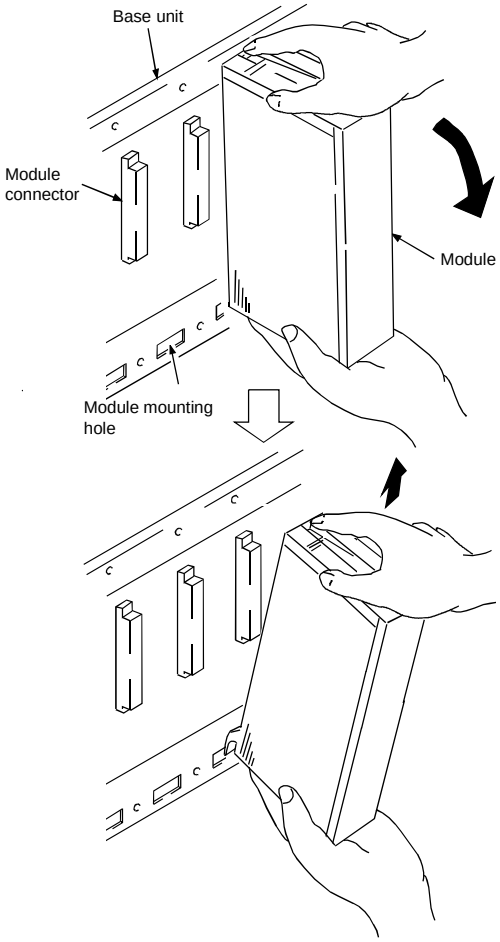
(2) Always turn the power supply OFF before mounting or removing any module.



(2) Module removal

The module removal procedure is as follows.





POINT

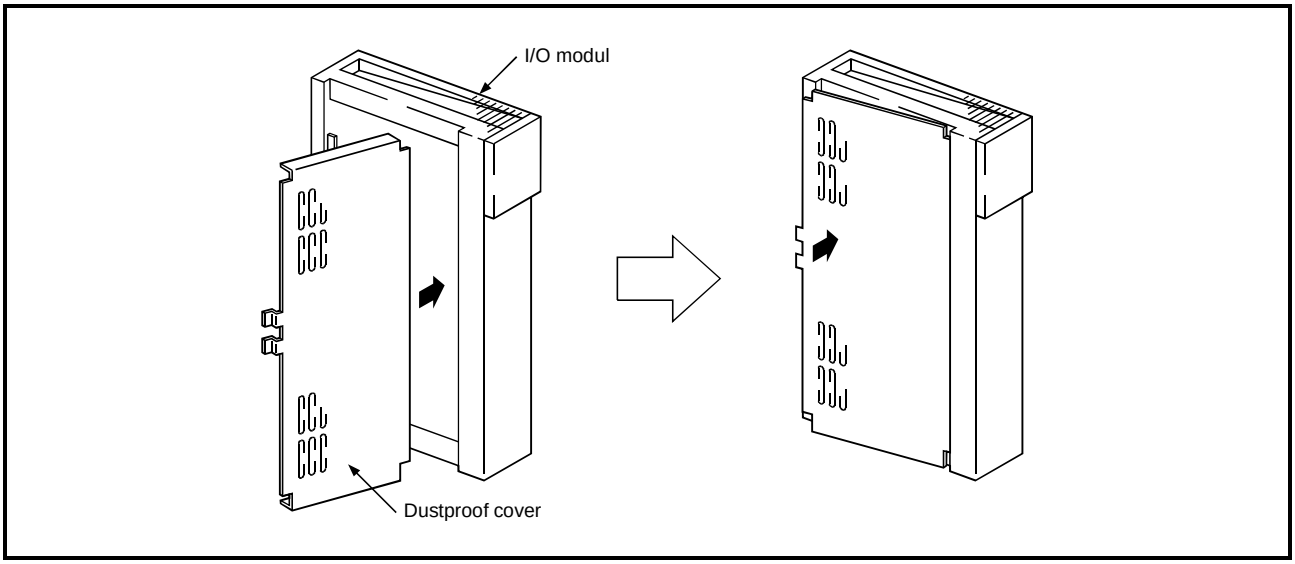
(1) When removing the module, be sure to remove the module mounting screw first and then remove the module mounting hook from the module mounting hole. If the module is forcibly removed, the screw or module mounting hook will be damaged.

(2) Always turn the power supply OFF before mounting or removal.

8.6 Installing and Removing the Dustproof Cover

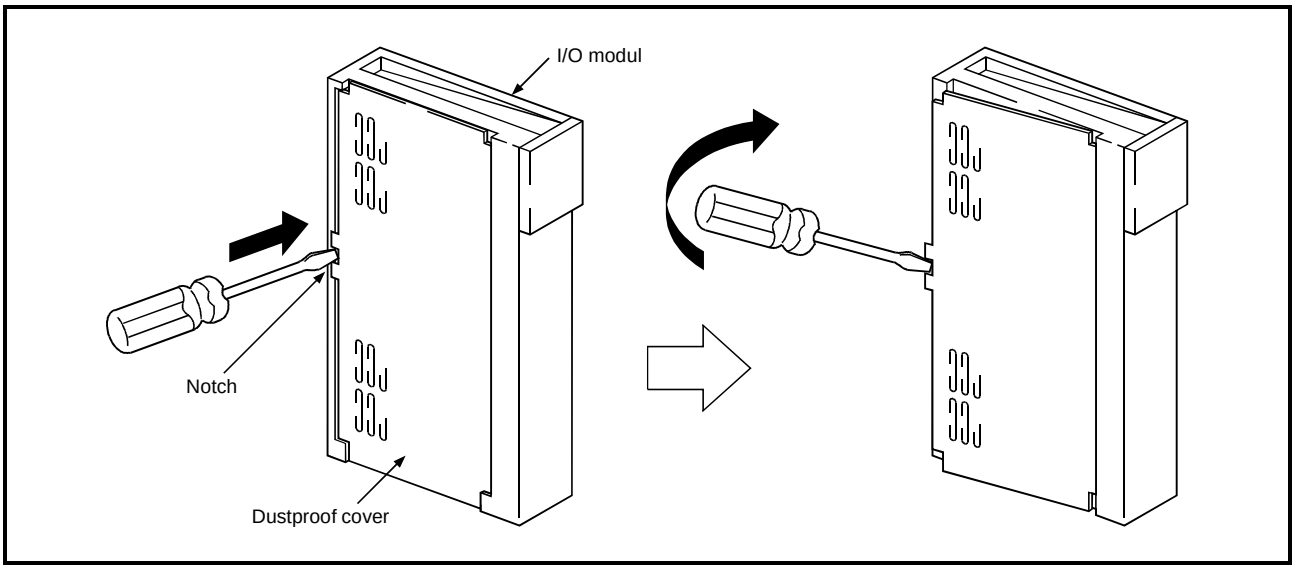
When an A1S52B(S1), A1S55B(S1), or A1S58B(S1) is used, it is necessary to mount the dustproof cover, which is supplied with the base, to the I/O module loaded at the left end to prevent foreign matter from entering the I/O module. If the dustproof cover is not mounted, foreign matter will enter the I/O module, resulting in malfunction. The following explains the installation and removal of the dustproof cover.

(1) Installation



To fit the dustproof cover to the I/O module, first insert it at the terminal side and then press it against the I/O module as shown in the figure.

(2) Removal



Fit the tip of a flat blade screwdriver into the notch on the left side of the dustproof cover. While keeping the screwdriver tip in the notch, gently move the screwdriver to the left (as shown above) until the cover snaps open.

8.7 Wiring

This section gives the wiring instructions for the system.

8.7.1 Wiring instructions

⚠ DANGER

- Before biginning any installation or wiring work, make sure all phases of the power supply have been obstructed from the outside. Failure to completely shut off the power supply phases may cause electric shock and/or damage to the module.
- When turning on the power or operating the module after installation or wiring work, be sure the module's terminal covers are correctly attached. Failure to attach the terminal covers may result in electric shock.

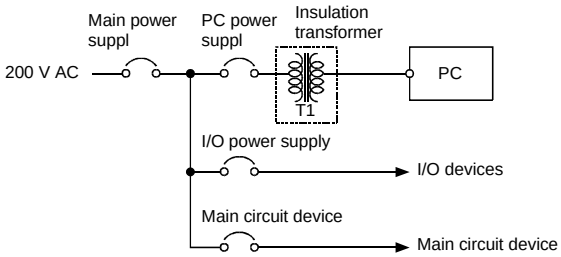
⚠ CAUTION

- Be sure to ground the FG terminals and LG terminals to the protective ground conductor. Not doing so could result in electric shock or erroneous operation.
- When wiring the PC, check the rated voltage and terminal layout of the wiring, and make sure the wiring is done correctly. Connecting a power supply that differs from the rated voltage or wiring it incorrectly may coups fire or breakdowns.
- Tighten the terminal screws with the specified torque. If the terminal screws are loose, it may result in short circuits, fire or malfunction.
  If the terminal screws are tightened too much, it may damage the screws and the module result in short circuits, malfunction or cause the module to fall out.
- Be careful not to let foreign matter such as filings or wire chips gear inside the module. These can cause fire, breakdowns and malfunction.
- Perform correct pressure-welding, crimp-contact or soldering for connectors for the outside using the specified tools. See the User's Manual of the corresponding I/O module for tools required to perform pressure-welding and crimp-contact.
  Incorrect connection may cause short circuits, fire, or malfunction.
- Do not bunch the control wires or communication cables with the main circuit or power wires, or install them close to each other. They should be installed 100 mm (3.94 in.) or more from each other. Failure to do so may result in nose that would cause malfunction.

Precautions when wiring power supply cable are described.

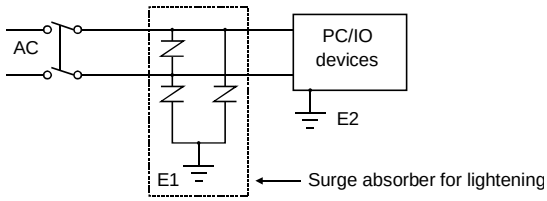
(1) Wiring power supply

(a) Separate the PC's power supply line from the lines for I/O devices and power devices as shown below.
When there is much noise, connect an insulation transformer.



(b) 100 V AC, 200 V AC and 24 V DC wires should be twisted as dense as possible. Connect the modules with the shortest distance.
Also, to reduce the voltage drop to the minimum, use the thickest wires possible (maximum 2 mm^2).

(c) As a countermeasure to power surge due to lightening, connect a surge absorber for lightening as shown below.



POINT

(1) Separate the ground of the surge absorber for lightening (E_1) from that of the PC (E_2).

(2) Select a surge absorber for lightening whose power supply voltage does no exceed the maximum allowable circuit voltage even at the time of maximum power supply voltage elevation.

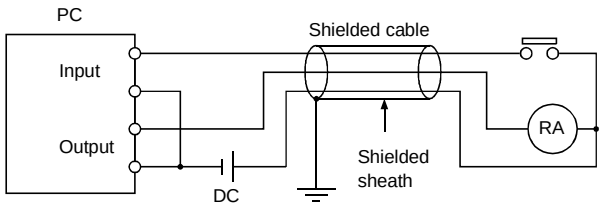
(2) Wiring of I/O equipment

(a) The applicable size of wire for connection to the terminal block connector is 0.75 (18) to 1.25 mm^2 (14 AWG). However, it is recommended to use wires of 0.75 mm^2 (18 AWG) for convenience.

(b) Separate the input and output lines.

(c) I/O signal wires must be at least 100 mm (3.94 in.) away from high-voltage and large-current main circuit wires.

(d) If the I/O signal wires cannot be separated from the main circuit wires and power wires, ground at the PC side with batch-shielded cables. Under some conditions, it may be preferable to ground at the other side.



(e) If wiring has been done with piping, ground the piping.

(f) Separate the 24 V DC I/O cables from the 100 V AC and 200 V AC cables.

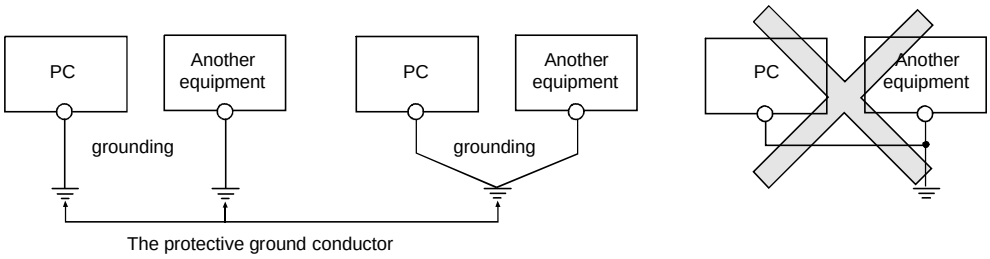
(g) <u>If wiring over 200 m (0.12 mile) or longer distances, problems can be caused by leakage currents due to line capacity. Take corrective action as described in Section 10.4.</u>

(2) Grounding

Grounding must be done in conformance with (a) to (d) below

(a) Ground the PC as independently as possible. Be sure to ground to the protective ground conductor (grounding resistance 100 Ω or less).

(b) If independent grounding is impossible, use the joint grounding method as shown in the figure below (2).



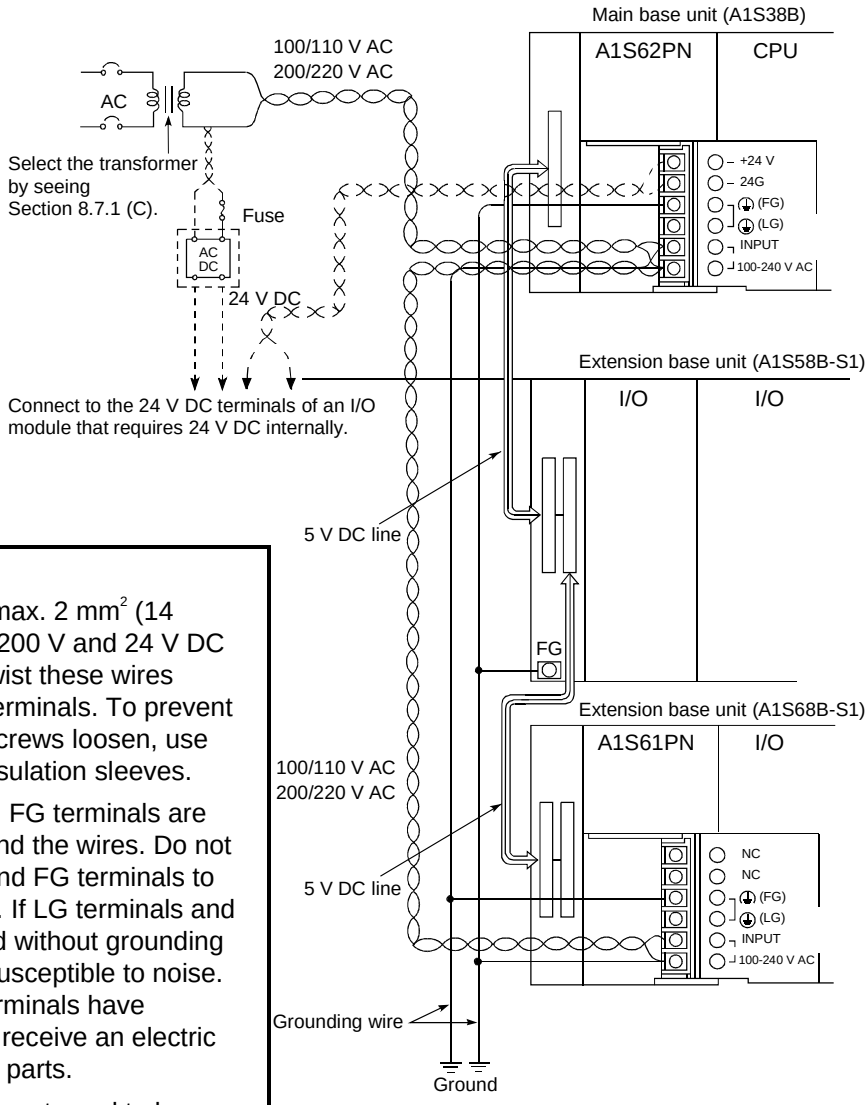
(1) Independent grounding…Best (2) Joint grounding…..Good (3) Joint grounding…..Not allowed

(c) Use a wire with a cross-sectional area of at least 2 mm^2 for grounding. Make the grounding point as close to the PC as possible so that the grounding wire is not too long.

(d) If any malfunction occur due to grounding, disconnect either or both of the LG and FG terminals of the base unit from the ground.

8.7.2 Wiring to module terminals

This section explains the wiring of power lines and grounding lines to the main and extension bases .



POINT

(1) Use the thickest possible (max. 2 mm^2 (14 AWG)) wires for the 100 V/200 V and 24 V DC power cables. Be sure to twist these wires starting at the connection terminals. To prevent a short-circuit should any screws loosen, use solderless terminals with insulation sleeves.

(2) When the LG terminals and FG terminals are connected, be sure to ground the wires. Do not connect the LG terminals and FG terminals to anything other than ground. If LG terminals and FG terminals are connected without grounding the wires, the PC may be susceptible to noise. In addition, since the LG terminals have potential, the operator may receive an electric shock when touching metal parts.

(3) A1S61PN and A1S62PN do not need to be switched as the are 100-240 V AC wide-range.

8.8 Precaution when Connecting the Uninterruptive Power Supply (UPS)

Be sure of the following items when connecting the AnSHCPU system to the uninterruptive power supply (abbreviated as UPS hereafter) :

Use a UPS which employs the constant inverter power supply method with 5 % or less voltage fluctuation.

Do not use a UPS with the constant commercial power supply method.

9. EMC DIRECTIVE AND LOW-VOLTAGE INSTRUCTION

9.1 Requirements for Compliance to EMC Directive (89/336/EEC)

The EMC Directive (89/336/EEC) will become mandatory within Europe from January 1st 1996. The EMC directive in essence defines the amount of electromagnetic output a product is allowed to produce and how susceptible that product is to electromagnetic interference. Any manufacturer or importer of electrical/electronic apparatus must before releasing or selling products within Europe after that date have either a CE mark attached to their goods. Testing to comply with the directive is done by use of agreed European standards which define limits for radiated and mains conducted electromagnetic emissions from equipment, levels of immunity to radiated emissions, ability for equipment to cope with transient voltage surges and electro-static discharges.

When installed in the specified manner this unit will be compliant with the relevant standards EN50081-2 and prEN50082-2 as applicable in the EMC directive. Failure to comply with these instructions could lead to impaired EMC performance of the equipment and as such Mitsubishi Electric Corporation can accept no liability for such actions.

9.1.1 EMC standards

When the PC is installed following the directions given in this manual its EMC performance is compliant to the following standards and levels as required by the EMC directive.

Specifications	Test Item	Test Description	Standard Values
EN50081-2 : 1995	EN55011 Radiated noise	Measure the electric wave released by the product.	30 M-230 M Hz QP : 30 dBμ V/m (30 m measurement) *1 230 M-1000 M Hz QP : 37 dBμ V/m (30 m measurement)
	EN55011 Conduction noise	Measure the noise released by the product to the power line.	150 K-500k Hz QP: 79 dB, Mean : 66 dB *1 500 K-30M Hz QP : 73 dB, Mean: 60 dB
prEN50082-2 : 1991	IEC801-2 Static electricity immunity *2	Immunity test by applying static electricity to the module enclosure.	4 k V contact discharge 8 k V air discharge
	IEC801-3 Radiated electromagnetic field *2	Immunity test by radiating an electric field to the product.	10 V/m, 27-500 M Hz
	IEC801-4 First transient burst noise	Immunity test by applying burst noise to the power line and signal cable.	2 k V
EN50082-2 : 1995	EN61000-4-2 Static electricity immunity *2	Immunity test by applying static electricity to the module enclosure.	4 k V contact discharge 8 k V air discharge
	EN61000-4-4 First transient burst noise	Immunity test by applying burst noise to the power line and signal cable., 2 k V	2 k V
	ENV50140 Radiated electromagnetic field AM modulation *2	Immunity test by radiating an electric field to the product.	10 V/m, 80-1000 M Hz, 80 % AM modulation@1 k Hz
	ENV50204 Radiated electromagnetic field Pulse modulation *2	Immunity test by radiating an electric field to the product.	10 V/m, 900 M Hz, 200 Hz pulse modulation, 50 % duty
	ENV50141 Conduction noise	Immunity test by inducting electromagnetic field to the power line signal cable.	10 Vrms, 0.15-80 M Hz, 80 % modulation@1 k Hz

(*1) QP: Quasi-peak value, Mean : Average value

(*2) The PC is an open type device (device installed to another device) and must be installed in a conductive control box.
The tests for the corresponding items were performed while the PC was installed to inside the control box.

9.1.2 Installation instructions for EMC

9.1.2.1 Control cabinet

When constructing a control cabinet where the PC system will be installed, the following instructions must be followed.

(1) Use a conductive control cabinet.

(2) When attaching the control cabinet's top plate or base plate, mask painting and weld so that good surface contact can be made between the cabinet and plate.

(3) To ensure good electrical contact with the control cabinet, mask the paint on the installation bolts of the inner plate in the control cabinet so that contact between surfaces can be ensured over the widest possible area.

(4) Earth the control cabinet with a thick wire so that a low impedance connection to ground can be ensured even at high frequencies. (22 mm^2 wire or thicker is recommended.)

(5) Holes made in the control cabinet must be 10 cm (3.94 in.) diameter or less. If the holes are 10 cm (3.94 in.) or larger, radio frequency noise may be emitted.

(6) Connect the door of cabinet to the main body with flat braided wires at as many points as possible so that a low impedance can be ensured even at high frequencies.

9.1.2.2 Connection of power and earth wires

Earthing and power supply wires for the PC system must be connected as described below.

(1) Provide an earthing point near the power supply module. Earth the power supply's LG and FG terminals (LG : Line Ground, FG : Frame Ground) with the thickest and shortest wire possible. (The wire length must be 30 cm (11.18 in.) or shorter.) The LG and FG terminals function is to pass the noise generated in the PC system to the ground, so an impedance that is as low as possible must be ensured. As the wires are used to relieve the noise, the wire itself carries a large noise content and thus short wiring means that the wire is prevented from acting as an antenna.

Note) A long conductor will become a highly efficient antenna at high frequency.

(2) The earth wire led from the earthing point must be twisted with the power supply wires. By twisting with the earthing wire, noise flowing from the power supply wires can be relieved to the earthing. However, if a filter is installed on the power supply wires, the wires and the earthing wire may not need to be twisted.

(3) Except for A1S61PEU and A1S62PEU, short between FG and LG terminals by a short jumper wire.

9.1.2.3 Cables

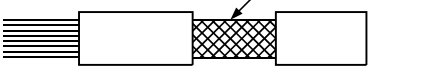
The cables led from the control cabinet contain a high frequency noise element and outside the control panel these cables act as antennae and radiate noise. The cables connected to input/output modules or special modules which leave the control panel must always be shielded cables.
Mounting of a ferrite core on the cables is not required (excluding some models) but if a ferrite core is mounted, the noise radiated through the cable can be suppressed further.
Use of a shielded cable is also effective for increasing the noise immunity level. The PC system's input/output and special function module provide a noise immunity level of equivalent to that stated in IEC801-4 : 2 k V when a shielded cable is used. If a shielded cable is not used or if the shield earthing treatment is not suitable even when used (See Section 9.1.2.4), the noise immunity level is less than 2 k V.

Note) prEN50082-2 specifies the noise resistance level based on the signal wire application.
Signals involved in process control : 2 k V
Signals not involved in process control : 1 k V

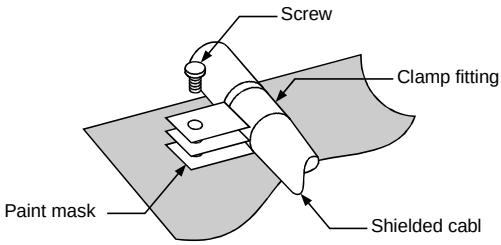
The meaning of "involved in process control" is not defined in prEN50082-2. However, when the purposes of the EMC Directive are considered, the signals that could cause personal injury or risks in the facility if a malfunction occurs should be defined as "signals involved in process control". Thus, it is assumed that a high noise immunity level is required.

9.1.2.4 Shield earthing

When a shield of the shielded cable is earthed to the cabinet body, please ensure that the shield contact with the body is over a large surface area. If the cabinet body is painted it will be necessary to remove paint from the contact area. All fastenings must be metallic and the shield and earthing contact must be made over the largest available surface area. If the contact surfaces are too uneven for optimal contact to be made either use washers to correct for surface inconsistencies or use an abrasive to level the surfaces. The following diagrams show examples of how to provide good surface contact of shield earthing by use of a cable clamp.

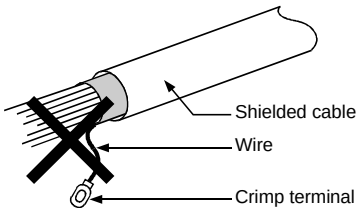


(a) Peal the cable insulation off and expose the shield section.



(b) Sandwich the exposed shield section with the and earth to the control cabinet over a wide area.

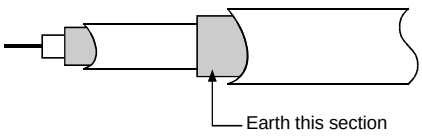
Note) The method of earthing by soldering a wire onto the shield section of the shielded cable as shown below is not recommended. The high frequency impedance will increase and the shield will be ineffective.



9.1.2.5 MELSECNET/II module

The following requirements apply to A1SJ71AR21, A1SJ71BR11, AnNCPUR21, AnACPUR21.

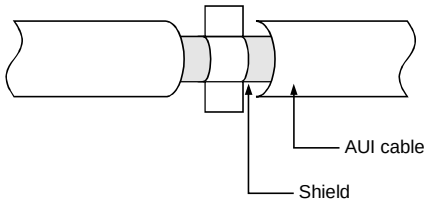
(1) Always use a triaxial cable for the module. The radiated noise in the band of 30 M Hz or higher can be suppressed by using a triax cable. Earth the outer shield by the method described in Section 9.1.2.4.



(2) Always mount a ferrite core onto the triaxial cable. Mount the ferrite core near the control cabinet outlet of each cable. Use of the TDK ZCAT3035 ferrite core is recommended.

9.1.2.6 Ethernet module

(1) Always earth the AUI cable connected to the A1SJ71E71-B5. The AUI is a shielded cable so remove the outer insulation and connect to earth the exposed shield section using as wide a surface area as possible in the manner shown below.



(2) Always use a triaxial cable for the coaxial cable connected to the A1SJ71E71-B2. The earthing precautions are the same as Section 9.1.2.5.

(3) For A1SJ71E71-B2/B5, always mount a ferrite core in addition to items (1) and (2) above. Use of the TDK ZCAT3035 ferrite core is recommended.

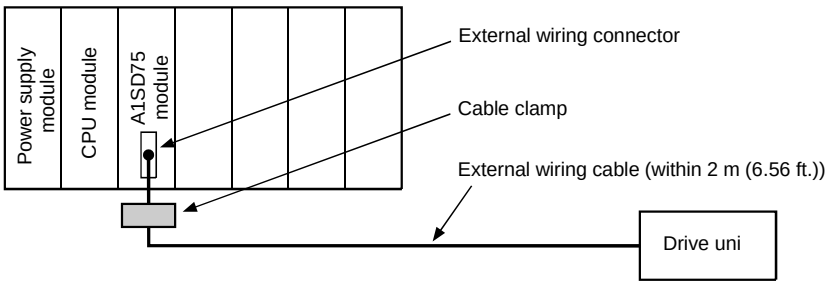
9.1.2.7 Positioning Modules

(1) When wiring with a 2 m (6.6 ft.) or less cable

Ground the shield section of the external wiring cable with the cable clamp. (Ground the shield at the closest location to the A1SD75 external wiring connector.)

Wire the external wiring cable to the drive unit and external device with the shortest distance.

Install the drive unit in the same panel.

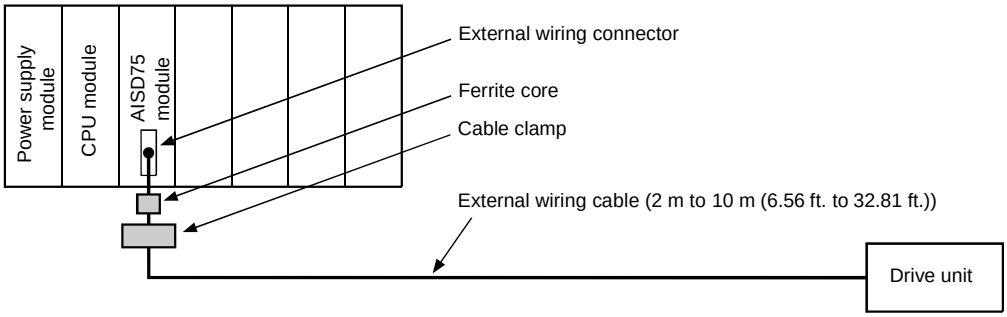


(2) When wiring with cable that exceeds 2 m (6.6 ft.), but is 10 m (32.8 ft.) or less

Ground the shield section of the external wiring cable with the cable clamp. (Ground the shield at the closest location to the AISD75 external wiring connector.)

Install a ferrite core.

Wire the external wiring cable to the drive unit and external device with the shortest distance.



(3) Ferrite core and cable clamp types and required quantities

(a) Cable clamp

Type : AD75Ck (Mitsubishi Electric)

(b) Ferrite core

Type : ZCAT3035-1330 (TDK ferrite core)

(c) Required quantity

Cable length	Prepared part	Required Qty		
		1 axis	2 axes	3 axes
Within 2 m (6.6 ft.)	AD75CK	1	1	1
2m (6.6 ft.) to 10m (32.8 ft.)	AD75CK	1	1	1
	ZCAT3035-1330	1	2	3

9.1.2.8 I/O and other communication cables

Always earth the shield section of the I/O signal cables and other communication cables (RS-232-C, RS-422, etc.) in the same manner as described in Section 9.1.2.4 if the cables go outside of the control cabinet.

9.1.2.9 Power supply module

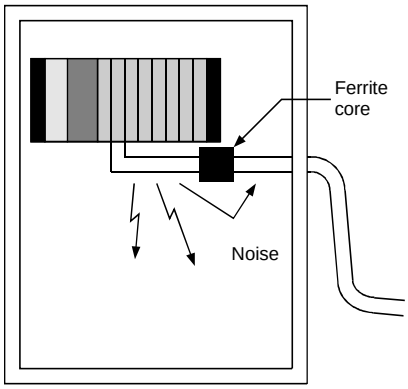
The precautions required for each power supply module are described below. Always observe the items noted as precautions.

Model	Precautions
A1S61P A1S62P A1S63P (*1)	Always mount one of the filters listed in Section 9.1.2.10 to the incoming power supply lines.
A1S61PEU A1S62PEU A1S61PN A1S62PN	None
A1SJCPU-S3 A1SJHCPU	Always ground the LG and FG terminals after short-circuiting them.

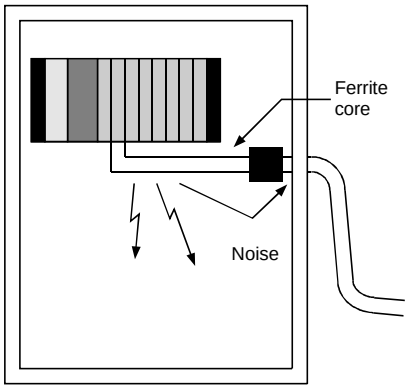
(*1) If a sufficient filter circuitry is built into a 24 V DC external power supply module, the noise generated by A1S63P will be absorbed by that filter circuit, so a line filter may not be required.

9.1.2.10 Ferrite core

A ferrite core is effective for reducing noise in the band of 30 M Hz to 100 M Hz. Mounting of a ferrite core is not necessary except for some particular models described in Section 9.1.2.5 and 9.1.2.6. However if further attenution of noise is necessary, mounting of a ferrite core on cables which radiate noise is recommended. When a ferrite core is mounted, mount the ferrite core just before the point where the cable goes outside of the cabinet. The ferrite will not be effective if the mounting position is not adequate.



(a) When there is a distance from the cable exit hole, the noise will jump over the ferrite, thus the effect will be halved.



(b) When mounted by the cable exit hole, the noise will not jump over the ferrite.

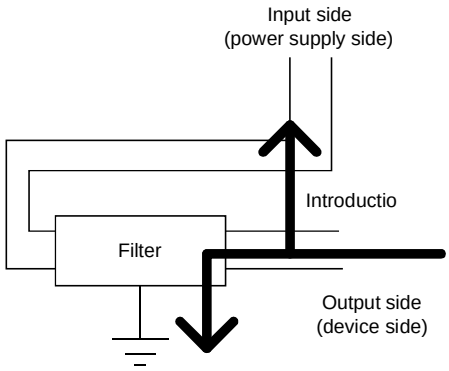
9.1.2.11 Noise filter (power supply line filter)

The noise filter (power supply line filter) is a device effective to reduce conducted noise. Except some particular models described in Section 9.1.2.8, installation of a noise filter onto the power supply lines is not necessary. However conducted noise can be reduced if it is installed. (The noise filter is generally effective for reducing conducted noise in the band of 10 M Hz or less.) Usage of the following filters is recommended.

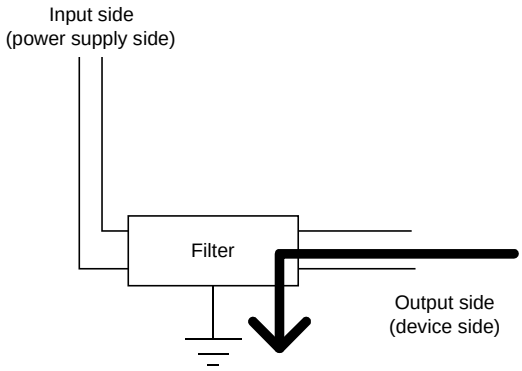
Model name	FN343-3/01	FN660-6/06	ZHC2203-11
Manufacturer	SCHAFFNER	SCHAFFNER	TDK
Rated current	3 A	6 A	3 A
Rated voltage	250 V		

The precautions required when installing a noise filter are described below.

(1) Do not bundle the wires on the input side and output side of the noise filter. When bundled, the output side noise will be induced into the input side wires from which the noise was filtered.



(a) The noise will be included when the input and output wires are bundled.



(b) Separate and lay the input and output wires.

(2) Earth the noise filter earthing terminal to the control cabinet with the shortest wire possible (approx. 10 cm (3.94 in.)).

9.2 Requirement to Conform to the Low-Voltage Instruction

The low-voltage instruction, one of the European Instructions, is now regulated.

The low-voltage instruction require each device which operates with power supply ranging from 50 V AC to 1000 V and 75 V DC to 1500 V to satisfy necessary safety items.

In the Sections from 9.2.1 to 9.2.8, cautions on installation and wiring of the MELSEC-AnS series PC to conform to the low-voltage instruction regulation are described.

We have put the maximum effort to develop this material based on the requirements and standards of the regulation that we have collected. However, compatibility of the devices which are fabricated according to the contents of this manual to the above regulation is not guaranteed. Each manufacturer who fabricates such device should make the final judgement about the application method of the low-voltage instruction and the product compatibility.

9.2.1 Standard applied for MELSEC-AnS

The standard applied for MELSEC-AnS is EN61010-1 safety of devices used in measurement rooms, control rooms, or laboratories.

For the modules which operate with the rated voltage of 50 V AC/75 V DC or above, we have developed new models that conform to the above standard. (See Appendix 4.)

For the modules which operate with the rated voltage under 50 V AC/75 V DC, the conventional models can be used, because they are out of the low-voltage instruction application range.

9.2.2 Precautions when using the MELSEC-AnS series PC

Module selection

(1) Power module

For a power module with rated input voltage of 100/200 V AC, select a model in which the internal part between the first order and second order is intensively insulated, because it generates hazardous voltage (voltage of 42.4 V or more at the peak) area. (See Appendix 4.)

For a power module with 24 V DC rated input, a conventional model can be used.

(2) I/O module

For I/O module with rated input voltage of 100/200 V AC, select a model in which the internal area between the first order and second order is intensively insulated, because it has hazardous voltage area. (See Appendix 4.)

For I/O module with 24 V DC rated input, a conventional model can be used.

(3) CPU module, memory cassette, base unit

Conventional models can be used for these modules, because they only have a 5 V DC circuit inside.

(4) Special module

Conventional models can be used for the special modules including analog module, network module, and positioning module, because the rated voltage is 24 V DC or smaller.

(5) Display device

Use an A870GOT CE compatible model.

9.2.3 Power supply

The insulation specification of the power module was designed assuming installation category II. Be sure to use the installation category II power supply to the PC.

The installation category indicates the durability level against surge voltage generated by a thunderbolt. Category I has the lowest durability; category IV has the highest durability.

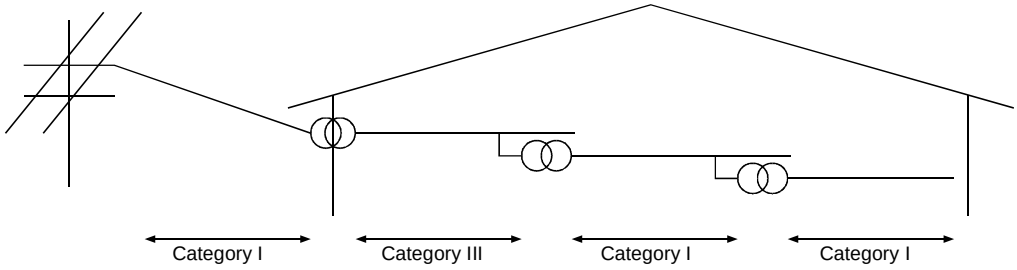


Figure 1. : Installation Category

Category II indicates a power supply whose voltage has been reduced by two or more levels of isolating transformers from the public power distribution.

9.2.4 Control box

Because the PC is an open device (a device designed to be stored within another module), be sure to use it after storing in the control box.

(1) Electrical shock prevention

In order to prevent persons who are not familiar with the electric facility such as the operators from electric shocks, the control box must have the following functions :

(a) The control box must be equipped with a lock so that only the personnel who has studied about the electric facility and have enough knowledge can open it.

(b) The control box must have a structure which automatically stops the power supply when the box is opened.

(2) Dustproof and waterproof features

The control box also has the dustproof and waterproof functions. Insufficient dustproof and waterproof features lower the insulation withstand voltage, resulting in insulation destruction. The insulation in our PC is designed to cope with the pollution level 2, so use in an environment with pollustion level 2 or below.

Pollution level 1 :	An environment where the air is dry and conductive dust does not exist.
Pollution level 2 :	An environment where conductive dust does not usually exist, but occasional temporary conductivity occurs due to the accumulated dust. Generally, this is the level for inside the control box equivalent to IP54 in a control room or on the floor of a typical factory.
Pollution level 3 :	An environment where conductive dust exits and conductivity may be generated due to the accumulated dust. An environment for a typical factory floor.
Pollution level 4 :	Continuous conductivity may occur due to rain, snow, etc. An outdoor environment.

As shown above, the PC can realize the pollution level 2 when stored in a control box equivalent to IP54.

9.2.5 Module installation

(1) Installing modules contiguously

In AnS series PCs, the left side of each I/O module is left open. When installing an I/O module to the base, do not make any open slots between any two modules. If there is an open slot on the left side of a module with 100/200 V AC rating, the printed board which contains the hazardous voltage circuit becomes bare. When it is unavoidable to make an open slot, be sure to install the blank module (A1SG60).

When using the A1S5oB expansion base with no power supply, attach the cover packaged with the expansion base to the side of the leftmost module.

9.2.6 Grounding

There are two kinds of grounding terminals as shown below. Either grounding terminal must be used grounded.

Be sure to ground the protective grounding for the safety reasons.

Protective grounding ⏚ : Maintains the safety of the PC and improves the noise resistance.

Functional grounding ⏚ : Improves the noise resistance.

9.2.7 External wiring

(1) 24 V DC external power supply

For special modules that require a 24 V DC I/O module or external power supply, use a model whose 24 V DC circuit is intensively insulated from the hazardous voltage circuit.

(2) External devices

When a device with a hazardous voltage circuit is externally connected to the PC, use a model whose circuit section of the interface to the PC is intensively insulated from the hazardous voltage circuit.

(3) Intensive insulation

Intensive insulation refers to the insulation with the dielectric withstand voltage shown in Table 2.

Table 2 : Intensive Insulation Withstand Voltage (Installation Category II, source : IEC664)

Rated voltage of hazardous voltage area	Surge withstand voltage (1.2/50 μs)
150 V AC or below	2500 V
300 V AC or below	4000 V

10. MAINTENANCE AND INSPECTION

This chapter describes items to be checked in daily and periodic maintenance and inspection in order to maintain the programmable controller in the normal and optimum condition.

10.1 Daily Inspection

Table 10.1 shows the inspection and items which are to be checked daily.

Table 10.1 Daily inspection

No.	Check item		Check point	Judgement	Corrective action
1	Base unit mounting conditions		Check for loose mounting screws and cover	The base unit should be securely mounted.	Retighten screws.
2	Mounting conditions of I/O module, etc.		Check if the module is disengaged and if the hook is securely engaged.	The hook should be securely engaged and the module should be positively mounted.	Securely engage the hook.
3	Connecting conditions		Check for loose terminal screws.	Screws should not be loose.	Retighten terminal screws
			Check distance between Solderless terminals.	The proper clearance should be provided between Solderless terminals	Correct.
			Check connectors of extension cable.	Connections should no be loose.	Retighten connector mounting screws.
4	CPU module indicator lamps	"POWER" LED	Check that the LED is ON.	ON (OFF indicates an error.)	See Section 11.2.2
		"RUN" LED	Check that the LED is ON during RUN.	ON (OFF or flashing indicates an error.)	See Sections 11.2.3 and 11.2.4
		"ERROR" LED	Check that the LED is ON when an error occurred.	OFF (ON when an error occurred.)	See Sections 11.2.5 and 11.2.6
		Input LED	Check that the LED turns ON and OFF.	ON when input is ON. OFF when input is OFF. (Display, other than above, indicates an error.)	See Sections 11.2.7
		Output LED	Check that the LED turns ON and OFF.	On when output is ON. OFF when output is OFF. (Display, other than above, indicates an error.)	See Sections 11.2.7

10.2 Periodic Inspection

This section explains the inspection items which are to be checked every six months to one year. This inspection should also be performed when the equipment is moved or modified or the wiring is changed.

Table 10.2 Periodic inspection

No.	Check item		Check point	Judgement	Corrective action
1	Ambient environment	Ambient temperature	Measure whit thermometer and hygrometer. Measure corrosive gas.	0 to 55 °C	When PC is used inside a panel, the temperature in the panel is the ambient temperature.
		Ambient humidity		10 to 90 % RH	
		Ambience		There should be no corrosive gases.	
2	Line voltage check.		Measure voltage across 100/200 V AC terminal.	85 to 132 V AC	Change supply power.
				170 to 264 V AC	
3	Mounting conditions	Looseness, play	Move the module.	The module should be mounted securely and positively.	Retighten screws.
		Ingress of dust or foreign material	Visual check.	There should be no dust or foreign material in the vicinity of the PC.	Remove and clean.
4	Connecting conditions	Loose terminal screws	Retighten.	Connectors should not be loose.	Retighten.
		Distances between Solderless terminals.	Visual check.	The proper clearance should be provided between Solderless terminals.	Correct.
		Loose connector	Visual check.	Connectors should not be loose.	Retighten connector mounting screws.
5	Battery		Check battery status by mounting special auxiliary relays M9006 and M9007.	Preventive maintenance	If battery capacity reduction is not indicated, change the battery when specified service life is exceeded.

10.3 Replacement of Battery

M9006 or M9007 turns ON when the voltage of the battery for program backup and power interruption compensation falls.

Even if this special relay turns ON, the contents of the program and the power interruption compensation function are not lost immediately.

However, if the ON state is overlooked, the PC data contents may be lost.

Special auxiliary relays M9006 and M9007 are switched ON to indicate that the battery has reached the life time (minimum) indicated in Table 10.3 and it must be replaced if continued use of the power interruption RAM and /or data backup is required.

The following sections give the battery service life and the battery changing procedure.

10.3.1 Service life of battery

Table 10.3 shows the service life of the battery.

Table 10.3 Battery life

Battery life / CPU model	Battery life (Total power interruption time) [Hr]		
	Guaranteed value (MIN)	Actual service value (TYP)	After M9006 or M9007 is turned ON
A1SJHCPU A1SHCPU A2SHCPU	4000	20000	100
A2SHCPU-S1	2200	12000	56

* The actual service value indicates a typical life time and the guaranteed value indicates the minimum life time.

Preventive maintenance is as follows :

(1) Even if the total power interruption time is less than the guaranteed value in the above table, change the battery after four to five years.

(2) When the total power interruption time has exceeded the guaranteed value in the table above and M9006 has turned ON, change the battery.

10.3.2 Battery replacement procedure

When the service life of the battery has expired, replace the battery using the following procedure :

Even if the battery is removed, the memory is backed up by a capacitor for some time.

However, if the replacement time exceeds the guaranteed value shown in the following table, the contents of the memory may be lost. Therefore, replace the battery as quickly as possible.

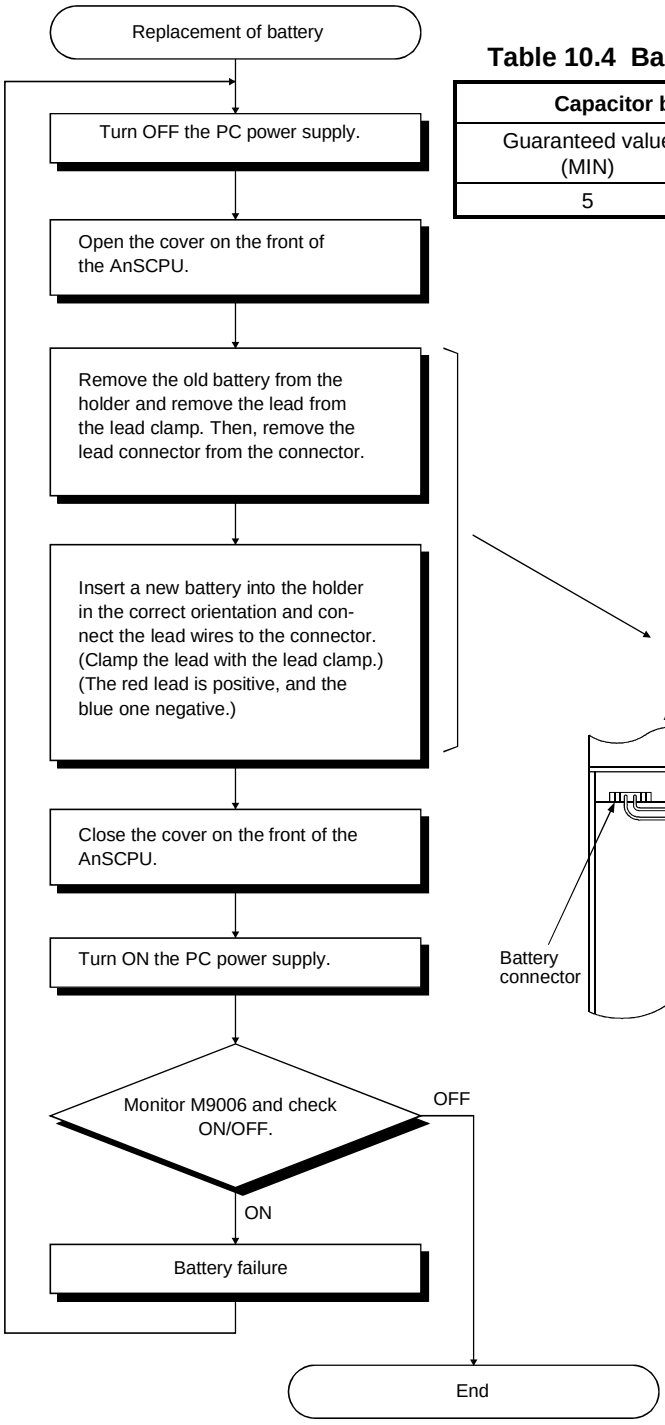


Table 10.4 Backup time by capacitor

Capacitor backup time (Minutes)	
Guaranteed value (MIN)	Actually applied value (TYP)
5	15

11. TROUBLESHOOTING

This chapter describes various procedures for troubleshooting, and corrective action.

11.1 Basic Troubleshooting

System reliability depends not only on reliable equipment but also on short down-times in the event of faults.

The three basic points to be kept in mind in troubleshooting are :

(1) Visual checks

Check the following points

(a) Machine motion (in the stopped and operating status)

(b) Power ON or OFF

(c) Status of I/O equipment

(d) Condition of wiring (I/O wires, cables)

(e) Display status of various indicators (such as the POWER LED, RUN LED, ERROR LED, and I/O LED)

(f) Status of various setting switches (such as extension base and power interruption compensation)

After checking (a) to (f), connect the peripheral equipment and check the running status of the PC CPU and the program contents.

(2) Trouble check

Observe any changes in the error condition when performing the following operations :

(a) Set the RUN/STOP keyswitch to the STOP position.

(b) Reset using the RUN/STOP keyswitch.

(c) Turn the power ON and OFF.

(3) Narrow down the possible causes of the trouble :

Deduce where the fault lies, i.e :

(a) Inside or outside the PC CPU.

(b) In the I/O module or another module.

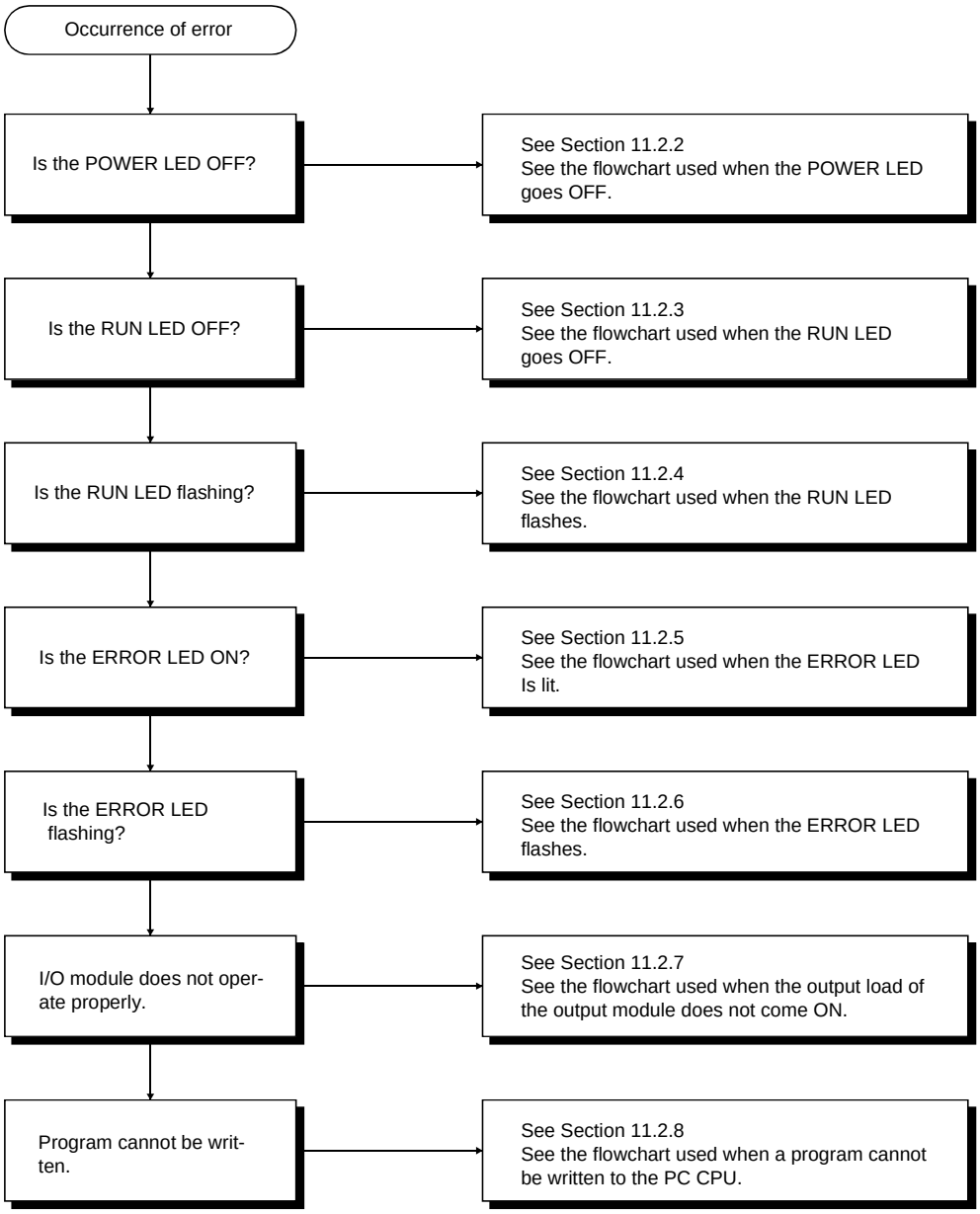
(c) In the sequence program.

11.2 Troubleshooting

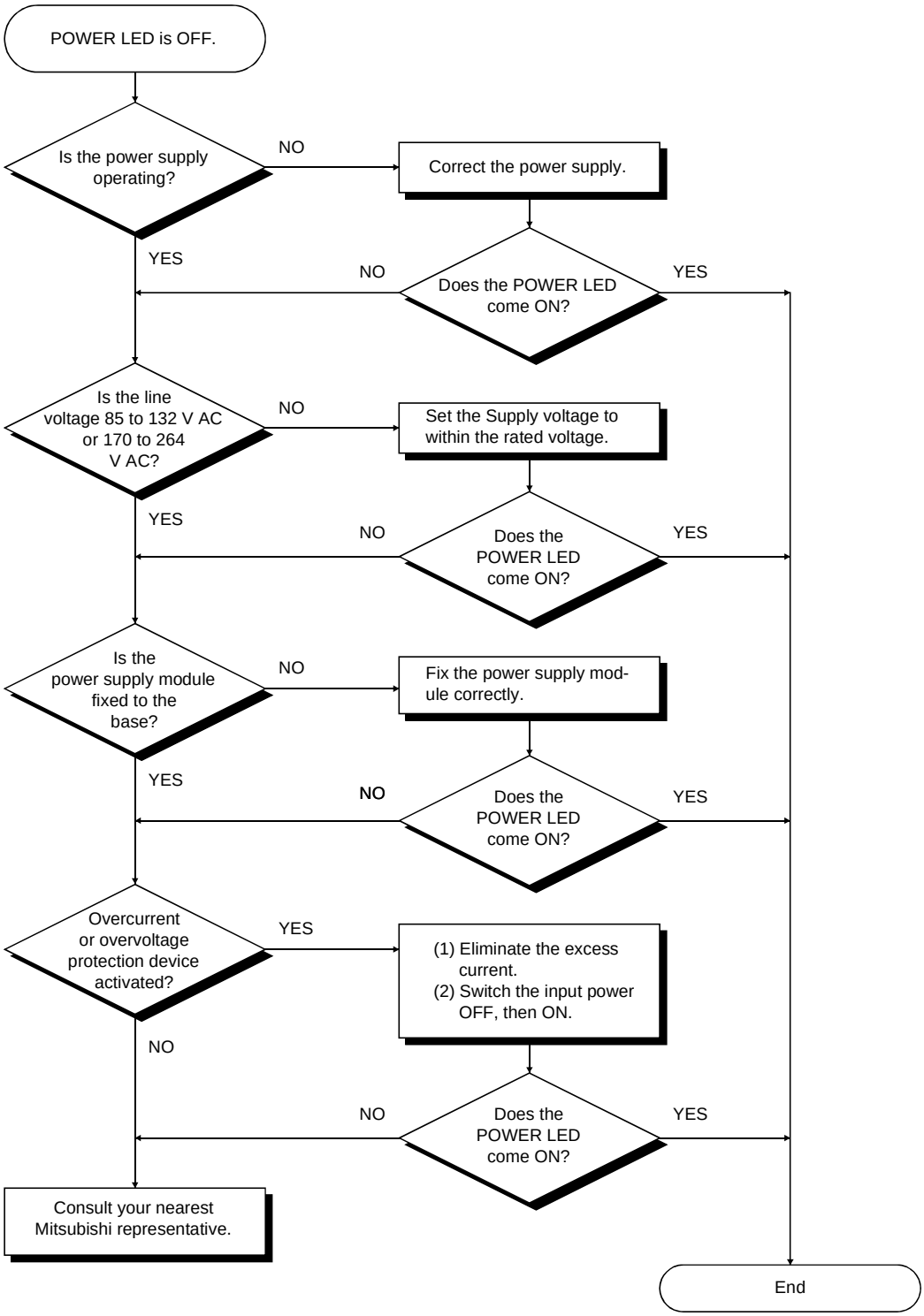
This section explains the procedure for determining the cause of problems, errors, and corrective action to be taken in response to error codes.

11.2.1 Troubleshooting flowcharts

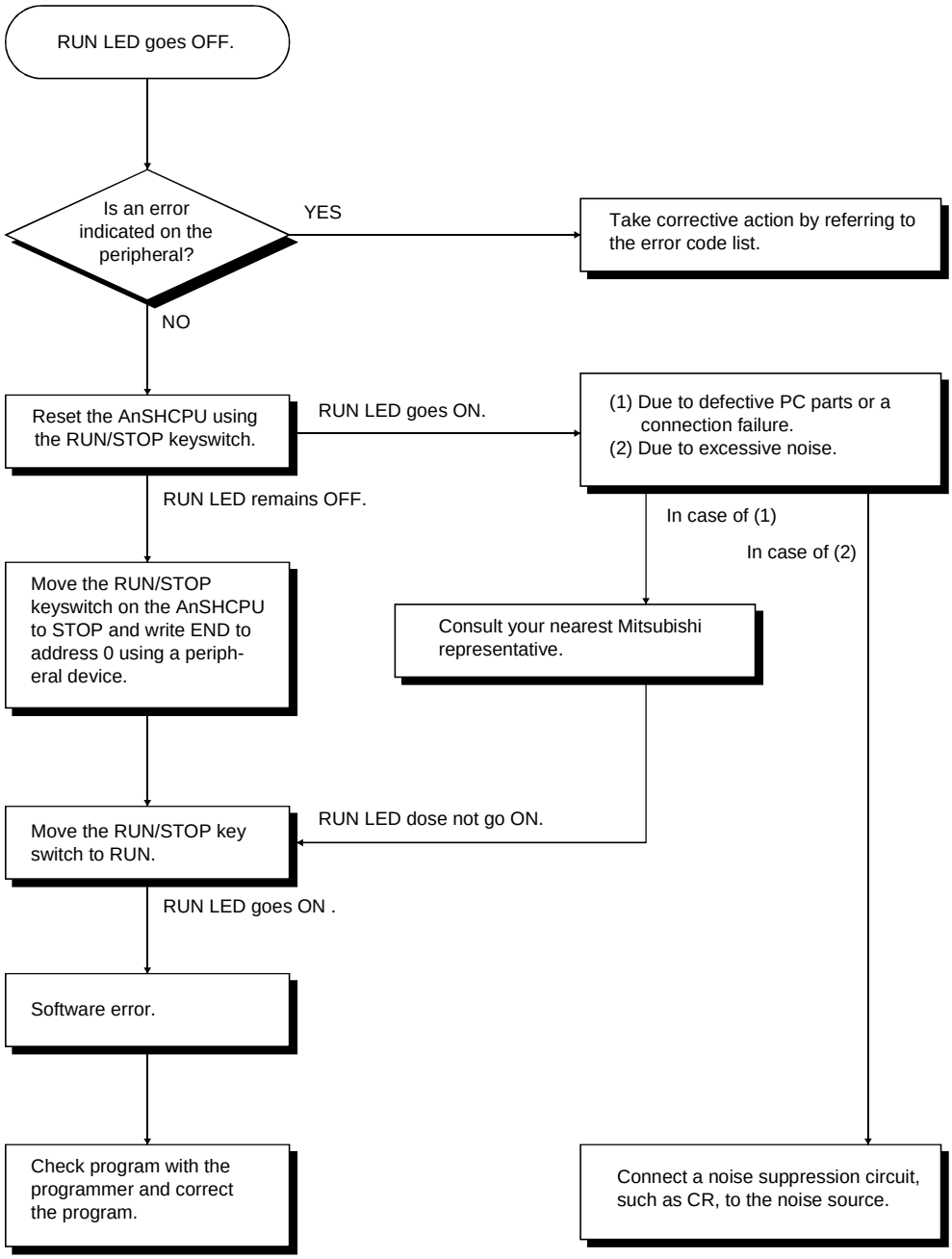
The procedures for troubleshooting are given in the following flowcharts :



11.2.2 Flowchart used when the POWER LED goes OFF

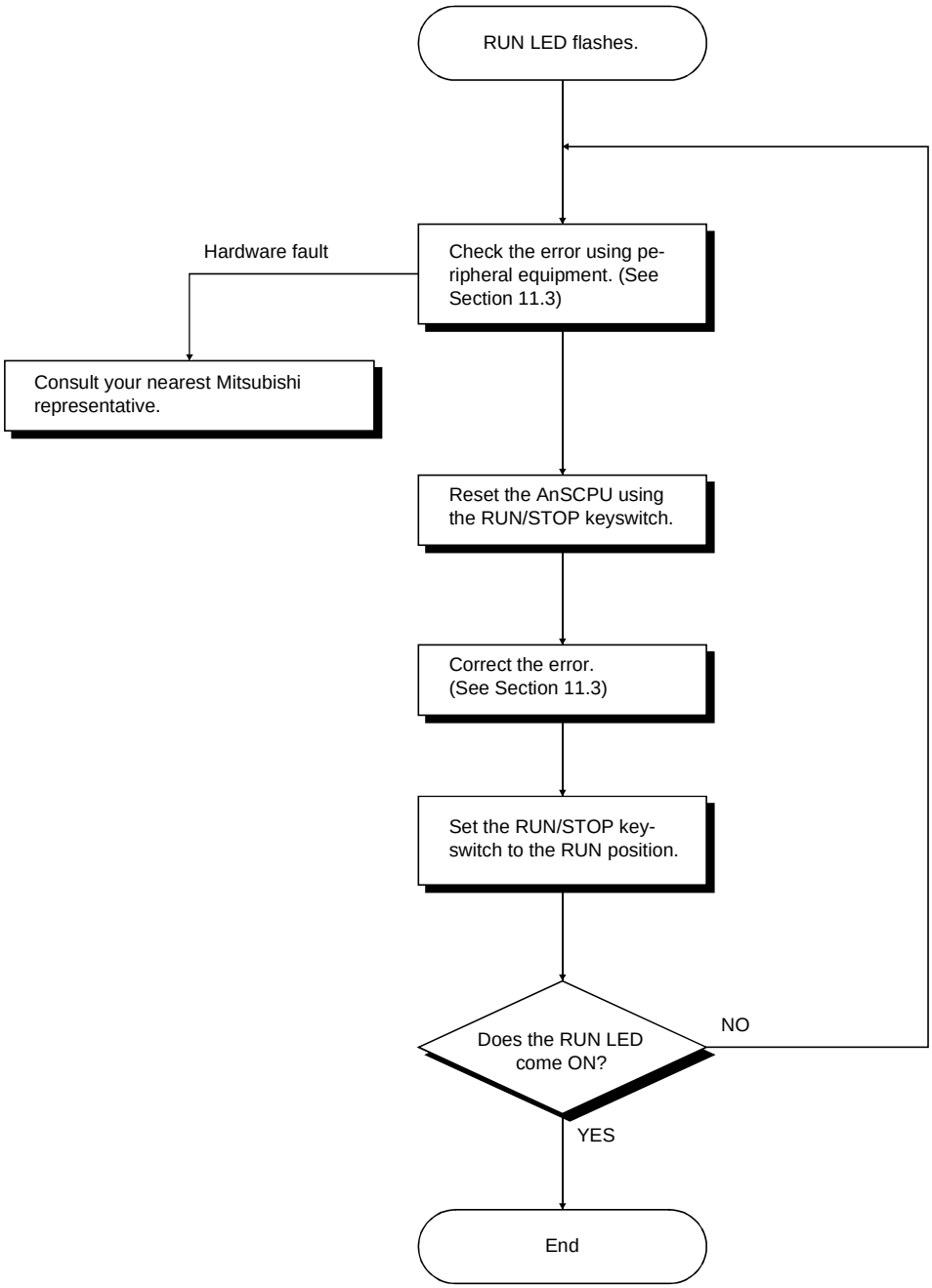


11.2.3 Flowchart used when the RUN LED goes OFF



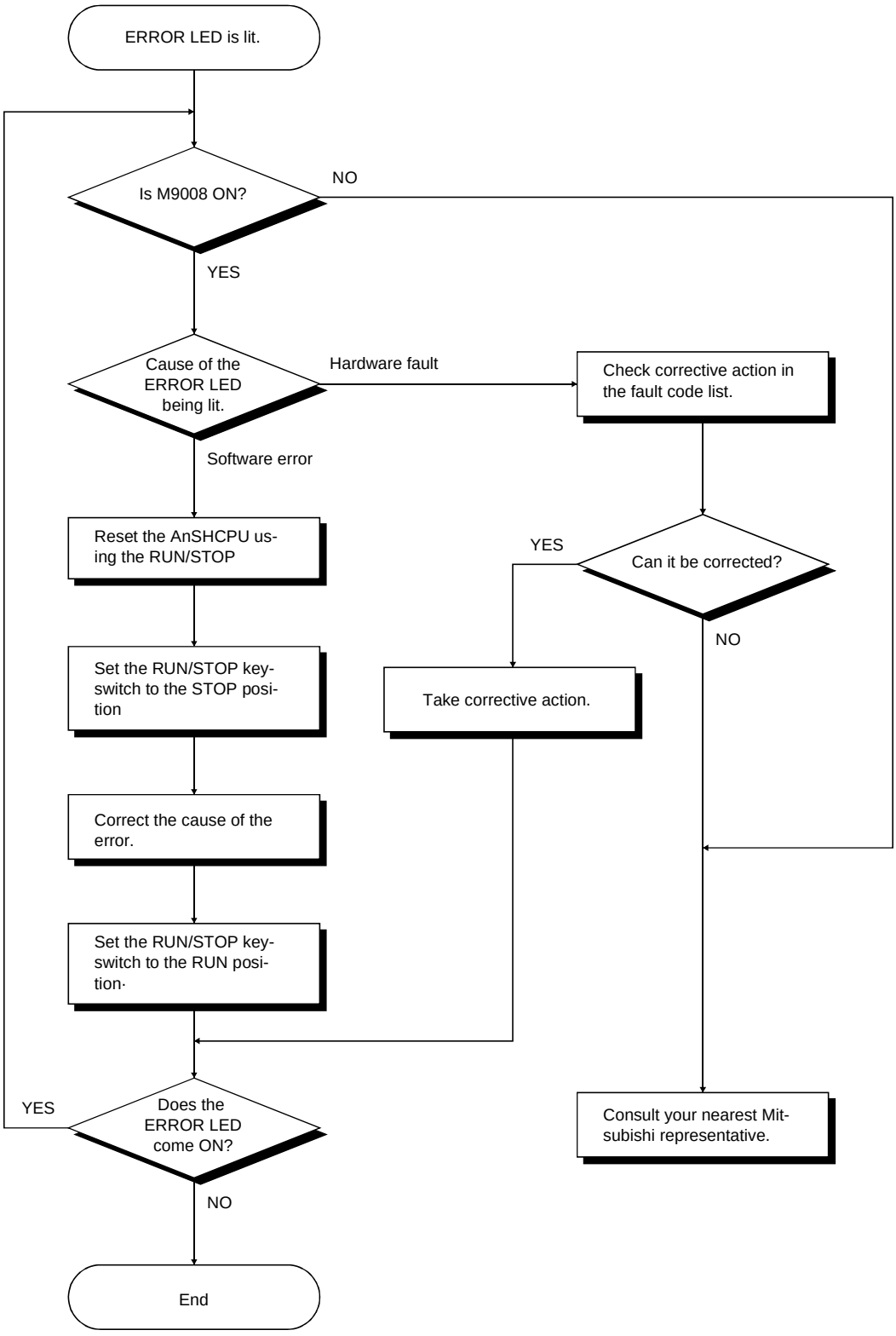
11.2.4 Flowchart used when the RUN LED flashes

The following shows the corrective measures to take if the RUN LED flashes when the power is switched ON, when operation is started, or during operation.



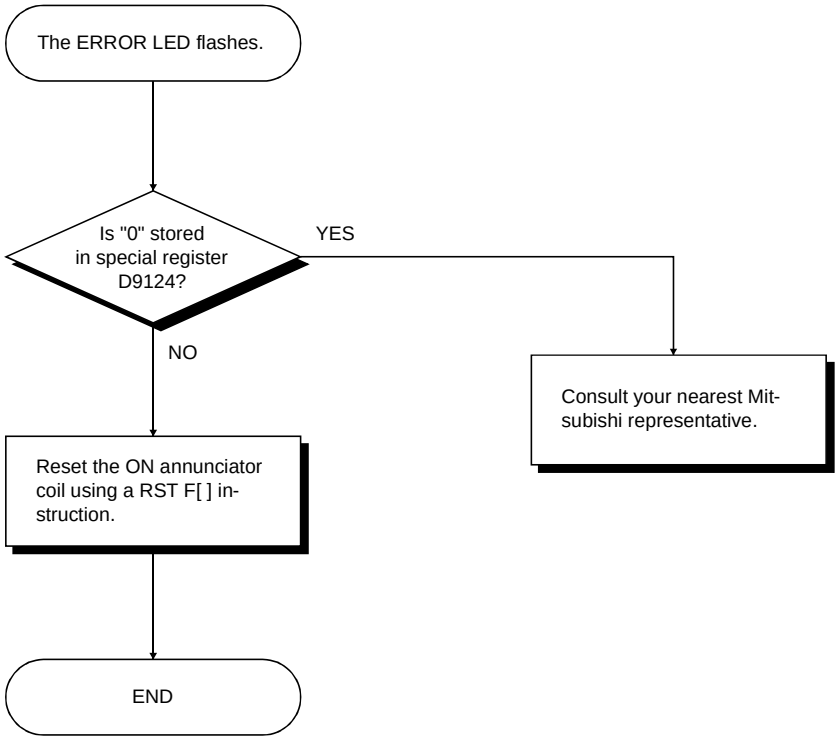
11.2.5 Flowchart used when the ERROR LED is lit

The following shows the corrective measures when the ERROR LED is lit in the RUN status.

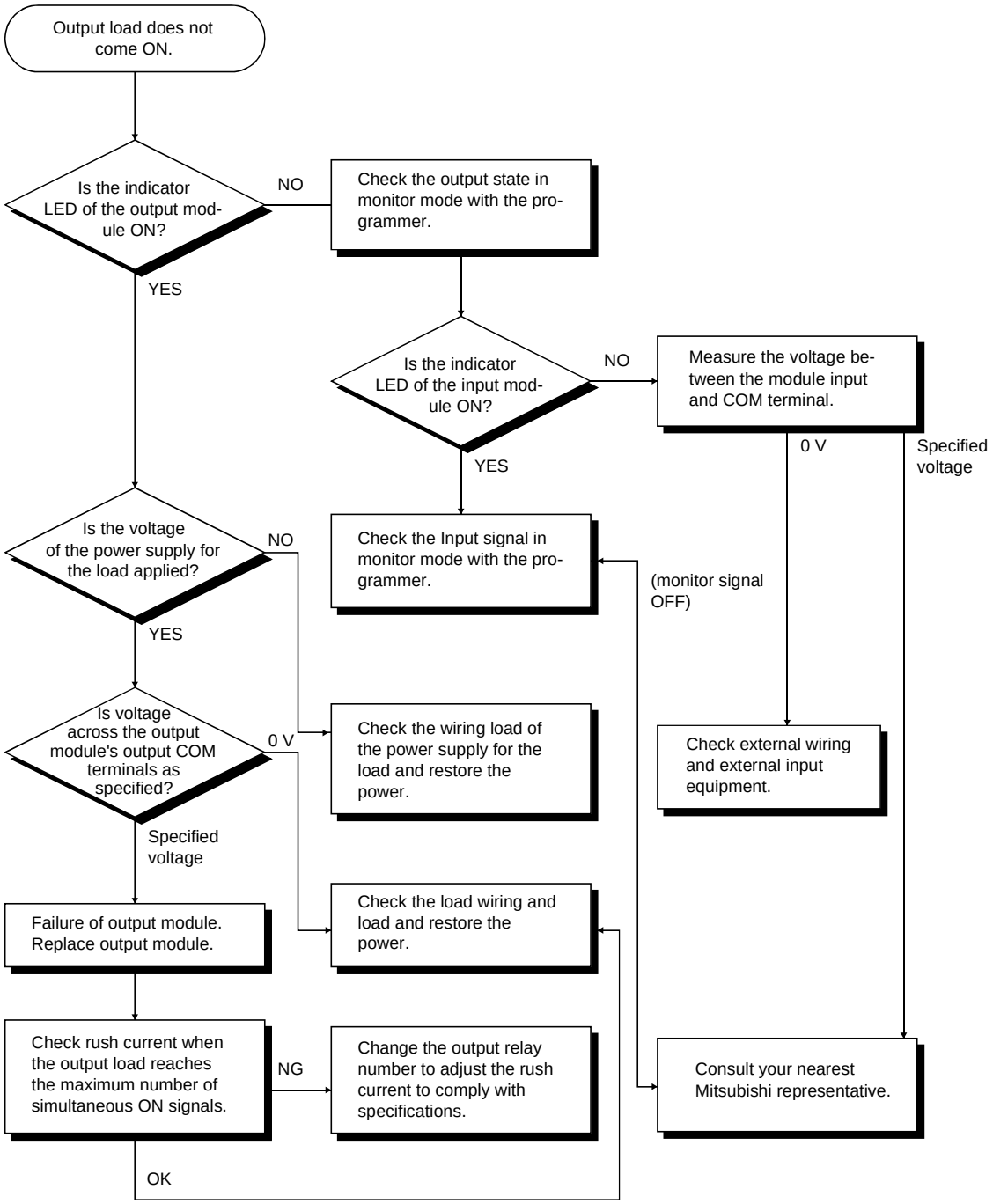


11.2.6 Flowchart used when the ERROR LED flashes

The following shows the corrective measures when the ERROR LED flashes.



11.2.7 Flowchart used when the output load of the output module does not come ON

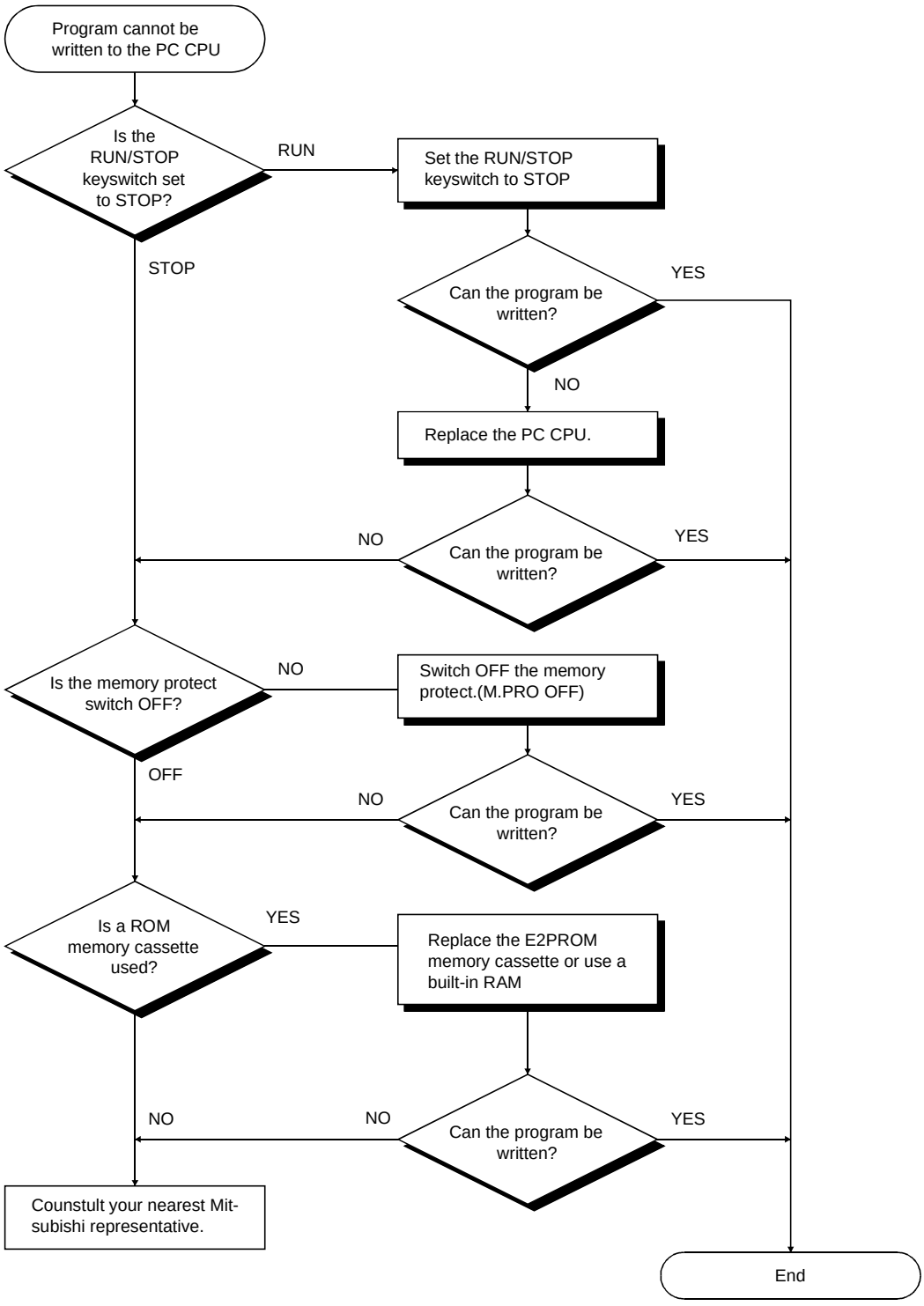


POINT

If the input or load signals are not switched OFF, see Section 11.4 I/O Connection Troubleshooting and take corrective measures.

11.2.8 Flowchart used when a program cannot be written to the PC CPU

The following shows the corrective measures when a program cannot be written to the PC CPU.



11.3 Error Code List

If an error occurs in the RUN mode, an error display or error code (including a step number) is stored in the special register by the self-diagnosis function. The error code reading procedure and the causes of and corrective actions for errors are shown in Table 11.1.

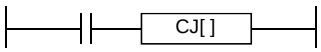
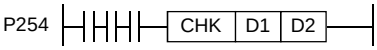
11.3.1 Error codes

The followings are the explanation about the descriptions and the causes of the error messages, error codes and the detailed error codes, and their corrective actions.

The detailed error codes are stored in D9092 only when using the dedicated instruction for CC-Link.

Table 11.1 Error codes

Error message	Contents of special register D9008 (BIN value)	Deaile error code (D9092)	CPU status	Error and cause	Corrective action
INSTRUCT CODE ERR.	10	—	STOP	An instruction code which cannot be decoded by the CPU is included in the program. (1) A memory cassette containing an invalid instruction code has been loaded. (2) The occurrence of an error destroyed the memory contents, adding an instruction code that cannot be read to the memory.	(1) Read the error step by using a peripheral device and correct the program at that step. (2) In the case of the memory cassette, rewrite the contents of the ROM, or replace with a memory cassette whose contents have been correctly written.
		101		An instruction code which cannot be decoded by the CPU is included in the program. (1) A memory cassette containing an invalid instruction code has been loaded. (2) The occurrence of an error destroyed the memory contents, adding an instruction code that cannot be read to the memory.	(1) Read out the steps where the error occurred using a peripheral device, and correct the program. (2) Check if the used ROM contains instruction codes that cannot be interpreted, and insert the correct ROM.
		103		The device specified in the extension applied instruction is incorrect.	Read the error step by using a pheripheral device and correct the program at that step.
		104		Program configuration of the extension applied instruction is incorrect.	
		105		The command name of the extension applied instruction is incorrect.	
PARAMETER ERROR	11	—	STOP	The contents of the memory installed in the PC CPU have been destroyed because of noise, or the failure of the memory cassette.	(1) Check the loading of the PC CPU memory cassette and load it correctly. (2) Read the parameter data from the PC CPU by using a periperhal device. Make any necessary corrections and write it to the PC CPU again.
MISSING END INS.	12	—	STOP	(1) There is no END (FEND) instruction in the program.	(1) Write END at the end of the program.

Error message	Contents of special register D9008 (BIN value)	Deaile error code (D9092)	CPU status	Error and cause	Corrective action
CAN'T EXECUTE (P)	13	—	TOP	(1) There is no jump destination for plural destinations specified by the CJ, SCJ, CALL, CALLP or JMP instructions. (2) Although there is no CALL instruction, the RET instruction exists in the program and has been executed. (3) The CJ, SCJ, CALL, CALLP or JMP instruction has been executed with its jump destination located below the END instruction. (4) The number of FOR instructions does not match the number of NEXT instructions. (5) The JMP instruction specified between FOR and NEXT has caused the execution to deviate from between FOR and NEXT. (6) The JMP instruction has caused the execution to deviate from the subroutine before the RET instruction is executed. (7) The JMP instruction has caused execution to jump to a step or subroutine between FOR and NEXT.	(1) Read the error step by using a peripheral device and correct the program at that step. (Make corrections such as the insertion of a jump destination or the changing of jump destinations to one destination.)
CHK FORMAT ERR.	14	—	STOP	(1) There are instructions (including NOP) other than LDX, LDIX, ANDX and ANIX in the CHK instruction circuit block. (2) There is more than one CHK instruction. (3) The number of contact points in the CHK instruction circuit block exceeds 150. (4) The X device number in the CHK instruction circuit block exceeds X7FE. (5) There is no circuit block in front of the CHK instruction circuit block.  (6) D1 device (number) of the CHK/D1/D2 instructions is different from the contact device (number) above the CJ [ ] instruction. (7) Pointer P254 is not attached to the start of the CHK instruction circuit block. 	(1) Check the program of the CHK instruction circuit block (1) to (7) in the left column. Correct errors using a peripheral device and restart the operation. (2) This error code is only valid when the direct method is used for I/O control.
CAN'T EXECUTE (I)	15	—	STOP	(1) Although the interrupt module is used,, there is no number for interrupt pointer I, which corresponds to that module,, in the program, or more than one number for pointer I exists in the program. (2) No IRET instruction has been entered in the interrupt program. (3) There is an IRET instruction somewhere besides the interrupt program.	(1) Check for the presence of interrupt program which corresponds to the interrupt module and create an interrupt program or reduce the number of Is to one. (2) Check if there is an IRET instruction in the interrupt program and enter the IRET instruction. (3) Check if there is an IRET instruction somewhere besides the interrupt program and delete that IRET instruction.

Error message	Contents of special register D9008 (BIN value)	Deaile error code (D9092)	CPU status	Error and cause	Corrective action
ROM ERR (for A1SHCPU)	17	—	STOP	(1) Parameters and/or sequence programs are not correctly written to the installed memory cassette.	(1) Write parameters and/or sequence programs correctly to the memory cassette. (2) Remove a memory cassette which does not have any parameter and/or sequence program.
RAM ERROR	20	—	STOP	(1) The PC CPU has checked if write and read operations can be performed properly with respect to the data memory area of the PC CPU. Normal writing and/or read/write turned out to be impossible.	Since this is a PC CPU hardware fault, consult your nearest Mitsubishi representative.
OPE. CIRCUIT ERR.	21	—	STOP	(1) The operation circuit, which performs the sequence processing in the PC CPU, does not operate properly	
WDT ERROR	22	—	STOP	Scan time exceeds watchdog monitoring time. (1) Scan time of user program is excessive. (2) Scan time has lengthened due to instantaneous power interruption which occurred during the scan.	(1) Calculate and check the scan time of the user program and reduce the scan time by the use of CJ instructions, etc. (2) Monitor the contents of special register D9005 by using a peripheral device. If the contents are other than 0, the line voltage is insufficient. Therefore, check the power and eliminate the voltage fluctuation.
END NOT EXECUTE	24	—	STOP	(1) When the END instruction is executed, it is read as another instruction code due to noise, etc. (2) The END instruction has changed to another instruction code.	(1) Perform reset and RUN. If the same error is displayed again, it is a PC CPU hardware fault. Therefore, consult your nearest Mitsubishi representative.
WDT ERROR	25	—	STOP	The END instruction cannot be executed with the program looped.	Check for an endless loop and correct the program.
module VERIFY ERR.	31	—	STOP (RUN)	I/O module data is different from that at power ON. (1) The I/O module (including the special function module) is incorrectly disengaged or has been removed, or a different module has been loaded.	(1) Among special registers D9116 to D9123, the bit corresponding to the module verify error is set to "1". Therefore, monitor the registers by using a peripheral device and check for the module whose bit is "1". (2) When the fault has been corrected, reset the PC CPU.
FUSE BREAK OFF	32	—	STOP (RUN)	(1) There is an output module with a blown fuse. (2) The external power supply for the output load is OFF or not connected.	(1) Check the blown fuse indicator LED of the output module and change the fuse in the module whose LED is ON. (2) Checking modules for blown fuses can also be done with a peripheral device. Among special registers D9100 to D9107, the bit corresponding to the module with a blown fuse is set to "1". Therefore, check by monitoring the registers. (3) heck the ON/OFF status of the external power supply for the output load.

Error message	Contents of special register D9008 (BIN value)	Deaile error code (D9092)	CPU status	Error and cause	Corrective action
CONTROL-BUS ERR.	40	—	STOP	The FROM and TO instructions cannot be executed. (1) Control bus error in the special function module.	(1) This is a special function module, CPU module or base module hardware fault. Therefore, change the module and check the defective module. Consult your nearest Mitsubishi representative about the defective module.
SP. module DOWN	41	—	STOP	When FROM and TO instructions cannot be executed. (1) Control bus error in the special function module.	This is a hardware fault in a special function module to which access has been made. Therefore, consult your nearest Mitsubishi representative about the defective module.
I/O INT. ERROR	43	—	STOP	Although the interrupt module is not installed, an interruption has occurred.	(1) This is a module hardware fault. Therefore, change the module and check the defective module. Consult your nearest Mitsubishi representative about the defective module.
SP. module LAY. ERR.	44	—	STOP	(1) Three or more computer link modules are installed in a single CPU module. (2) Two or more data link modules are installed. (3) Two or more interrupt modules are installed. (4) In the parameter setting of the peripheral device, while an I/O module is actually installed, a special function module has been set in the I/O assignment, or vice versa.	(1) Reduce the number of computer link modules to two or less. (2) Use one data link module. (3) Use one interrupt module. (4) Reset the I/O assignment in the parameter setting according to the actually loaded special function module by using a peripheral device.
SP. module ERROR	43	—	STOP (RUN)	(1) Access (execution of FROM/TO instruction) has been made to a location where there is no special function module.	(1) Read the error step by use of peripheral device, and check and correct the content of the FROM/TO instruction at that step by using a peripheral device.
		462		(1) The model name of the module specified in the CC-Link dedicated instruction is different from that specified by I/O allocation parameter. (2) The module specified by a CC-Link dedicated instruction is not a master module.	(1) Match the model name specified by I/O allocation parameter with that specified in the CC-Link dedicated instruction. (2) Read the error step with a peripheral device. Check and correct the CC-Link dedicated instruction in the step.
LINK PARA. ERROR	47	—	RUN	(1) The contents which have been written to the parameter area of the link by setting the link range in the parameter setting of peripheral device are different from the link parameter contents. (2) The setting for the total number of slave stations is 0	(1) Write the parameters again and check. (2) If this message is displayed again, there is a hardware fault. Therefore, consult your nearest Mitsubishi representative.
OPERATION ERROR	50	—	RUN (STOP)	(1) The result of BCD conversion has exceeded the specified range (9999 or 99999999). (2) A setting has been done which exceeds the specified device range and the operation cannot be done. (3) File registers are used in the program without performing the capacity setting of file registers.	(1) Use a peripheral device to read the error step and check and correct the program at that step. (Check device setting range, BCD conversion value, etc.)

Error message	Contents of special register D9008 (BIN value)	Deaile error code (D9092)	CPU status	Error and cause	Corrective action
OPERATION ERROR	50	503	RUN (STOP)	The storage data or constant for the specified device is out of range.	Read the error step by using a pheripheral device and correct the program at that step.
		504		The set number of data to be handled exceeds the usable range.	
		509		The number of CC-Link dedicated instructions for one scan exceeds 64.	Decrease the number of CC-Link dedicated instructions executed for one scan to 64 or less
				CC-Link dedicated instruction was executed to the CC-Link module in which parameters are not set.	Set the parameters.
BATTERY ERROR	70	—	RUN	(1) The battery voltage is below 24 V DC. (2) The battery lead is disconnected.	(1) Change the battery. (2) When RAM or power interruption compensation is used, connect the battery.

11.4 I/O Connection Troubleshooting

This section explains possible problems with I/O circuits.

11.4.1 Input circuit troubleshooting

This section describes possible problems with input circuits, and corrective action.

Table 11.2 Input circuit problems and corrective action

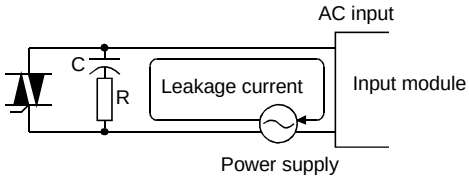
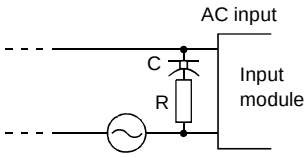
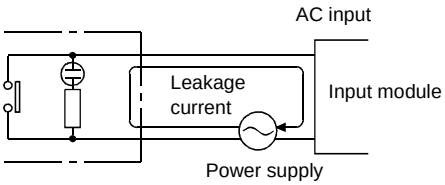
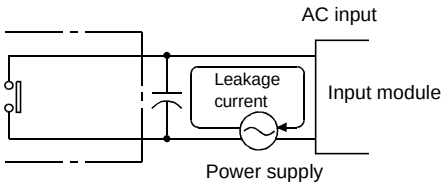
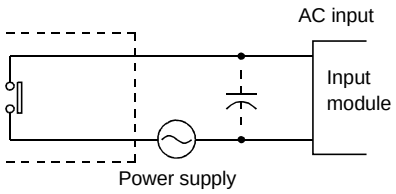
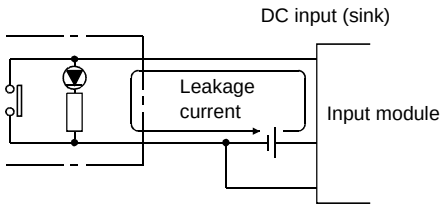
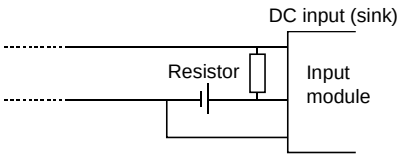
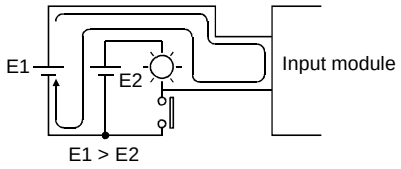
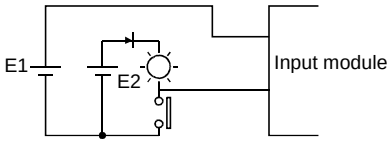
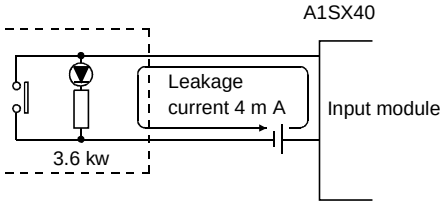
	Condition	Cause	Corrective action
Example 1	Input signal does not turn OFF	Leakage current of input switch (e.g. drive by non-contact switch). 	• Connect an appropriate resistor which will make the voltage across the terminals of the input module lower than the OFF voltage value.  It is recommended to use 0.1 to 0.47 μF + 47 to 120 Ω (1/2 W) for the CR constant.
Example 2	Input signal does not turn OFF	Drive by a limit switch with neon lamp. 	• Same as Example 1. • Or make up another independent display circuit.
Example 3	Input signal does not turn OFF	Leakage current due to line capacity of wiring cable. (Line capacity C of twisted pair wire is approx. 100 PF/m). 	• Same as Example 1. • However, leakage current is not generated when the power supply is located in the input equipment side as shown below. 
Example 4	Input signal does not turn OFF	Drive by switch with LED indicator. 	• Connect a register which will make the voltage between the input module terminal and common higher than the OFF voltage, as shown below.  * An example calculation of a value for a connected resistor is given on the following page.

Table 11.2 Input circuit problems and corrective action

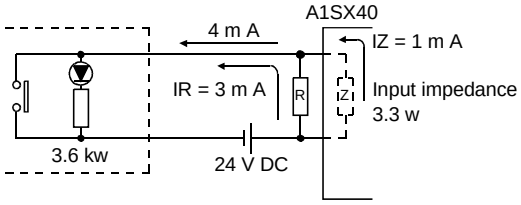
	Condition	Cause	Corrective action
Example 5	Input signal does not turn OFF	• Sneak path due to the use of two power supplies. 	• Use only one power supply. • Connect a sneak path prevention diode. (Figure below) 

<Example calculation for Example 4>

The switch with an LED indicator is connected to A1SX40, and there is a 4 m A leakage current.



(1) Since the leakage current does not reach the 1 m A OFF current of the A1SX40, the input signal does not go OFF. Connect a resistor as shown below :



(2) Calculate the value of the connected resistor R as follows :

To reach the 1 m A OFF current of the A1SX40, connect a resistor R through which a current of 3 m A or greater flows.

I.MDSD/R.MDNM/ : I.MDSD/Z.MDNM/ = Z (input impedance) : R

$$R \leq \frac{Iz}{IR} \times (\text{input impedance}) = \frac{1}{3} \times 3.3 = 1.1\ [k\ \Omega]$$

$R < 1.1\ k\ \Omega$

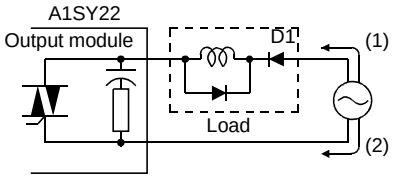
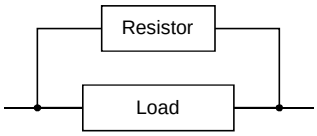
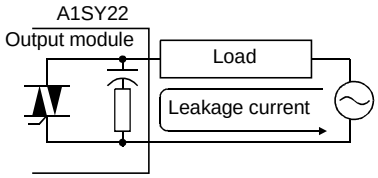
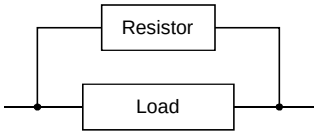
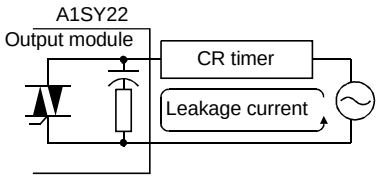
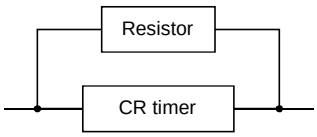
When R = 1 k Ω, the power capacity must be :

$W = (\text{applied voltage})^2 \div R = 26.4^2 \div 1000\ (\Omega) = 0.7\ (W)$

(3) The power capacity of the resistor should be three to five times as large as the actual power consumption. The problem can therefore be solved by connecting a 1 k Ω, 2 to 3 W resistor to the terminal in question.

11.4.2 Output circuit failures and corrective action

Table 11.3 Output circuit failures and corrective action

	Condition	Cause	Corrective action
Example 1	When the output is OFF, excessive voltage is applied to the load.	• Load is half-wave rectified inside (in some cases, this is true of a solenoid).  When the polarity of the power supply is as shown in [1], C is charged. When the polarity is as shown in [2], the voltage charged in C plus the line voltage are applied across D1. Max. voltage is approx. 2.2E.	• Connect a resistor of 10 to 99 k Ω. across the load. (If a resistor is used in this way, it does not pose a problem to the output element. But it may cause the diode, which is built into the load, to deteriorate, resulting in a fire, etc.) 
Example 2	The load does not turn OFF (triac output)	• Leakage current due to built-in noise suppression 	• Connect C and R across the load. (When the wiring distance from the output card to the load is long, there may be a leakage current due to the line capacity.) 
Example 3	When the load is a CR type timer, time constant fluctuates (triac output).		• Drive the relay using a contact and drive the CR type timer using the same contact. (Some timers have half-wave rectified internal circuits. Therefore, take the precautions indicated in the Example1.)  Calculate the CR constant depending on the load.

APPENDICES

Appendix 1 Instructions

Instructions used with the AnSHCPU are listed below.
See the following programming manuals for details of the instructions.

• ACPU Programming Manual (Fundamentals)	(IB-66249)
• ACPU Programming Manual (Common Instructions)	(IB-66250)
• AnSHCPU/AnACPU/AnVCPU Programming Manual (Dedicated Instructions)	(IB-66251)

(1) Sequence instructions

(a) Contact instruction

Contact	LD, LDI, AND, ANI, OR, ORI

(b) Connection instruction

Connection	ANB, ORB, MPS, MRD, MPP

(c) Output instruction

Output	OUT, SET, RST, PLS, PLF, CHK

(d) Shift instruction

Shift	SFT, SFTP

(e) Master control instruction

Master control	MC, MCR

(f) Termination instruction

Program end	FEND, END

(g) Other instructions

Stop	STOP
No operation	NOP
Page feed (page feed operation of printer output)	NOPLF

(2) Basic instructions

(a) Comparison instructions

=	16 bits	LD=, AND=, OR=
	32 bits	LDD=, ANDD=, ORD=
< >	16 bits	LD<>, AND<>, OR<>
	32 bits	LDD<>, ANDD<>, ORD<>
>	16 bits	LD>, AND>, OR>
	32 bits	LDD>, ANDD>, ORD>
<=	16 bits	LD<=, AND<=, OR<=
	32 bits	LDD<=, ANDD<=, ORD<=
<	16 bits	LD<, AND<, OR<
	32 bits	LDD<, ANDD<, ORD<
>=	16 bits	LD>=, AND>=, OR>=
	32 bits	LDD>=, ANDD>=, ORD>=

(b) BIN arithmetic operation instructions

+ Addition	16 bits	Two types each for + and +P
	32 bits	Two types each for D+ and D+P
- Subtraction	16 bits	Two types each for - and -P
	32 bits	Two types each for D- and D-P
* Multiplication	16 bits	*, *P
	32 bits	D*, D*P
/ Division	16 bits	/, /P
	32 bits	D/, D/P
+1 Addition	16 bits	INC, INCP
	32 bits	DINC, DINCP
-1 Subtraction	16 bits	DEC, DECP
	32 bits	DDEC, DDECP

(c) BCD arithmetic operation instructions

+ Addition	BCD 4 digits	Two types each for B+ and B+P
	BCD 8 digits	Two types each for DB+ and DB+P
- Subtraction	BCD 4 digits	Two types each for B- and B-P
	BCD 8 digits	Two types each for DB- and DB-P
* Multiplication	BCD 4 digits	B*, B*P
	BCD 8 digits	DB*, DB*P
/ Division	BCD 4 digits	B/, B/P
	BCD 8 digits	DB/, DB/P

(d) BCD - BIN conversion instructions

BIN → BCD	16 bits	BCD, BCDP
	32 bits	DBCD, DBCDP
BCD → BIN	16 bits	BIN, BINP
	32 bits	DBIN, DBINP

(e) Data transfer instructions

Transfer	16 bits	MOV, MOVP
	32 bits	DMOV, DMOVP
Change	16 bits	XCH, XCHP
	32 bits	DXCH, DXCHP
Undefined transfer	16 bits	CML, CMLP
	32 bits	DCML, DCMLP
Block transfer	16 bits	BMOV, BMOVP
Repeat data block transfer	16 bits	FMOV, FMOVP

(f) Program branch instructions

Jump	CJ, SCJ, JMP
Subroutine call	CALL, CALLP, RET
Interrupt program enable/disable	EI, DI, IRET
Microcomputer program call	SuB

(g) Refresh instructions

Link refresh	COM
Link refresh enable/disable	EI, DI
Partial refresh	SEG

(3) Application instructions

(a) Logical operation instructions

Logical product	16 bits	Two types each for WAND and WANDP
	32 bits	DAND, DANDP
Logical product	16 bits	Two types each for WOR and WORP
	32 bits	DOR, DORP
Exclusive logical sum	16 bits	Two types each for WXOR and WXORP
	32 bits	DXOR, DXORP
NOT exclusive logical sum	16 bits	Two types each for WXNR and WXNRP
	32 bits	DXNR, DXNRP
2's complement (reversed sign)	16 bits	NEG, NEGP

(b) Rotation instructions

Right ward rotation	16 bits	ROR, RORP, RCR, RCRP
	32 bits	DROR, DRORP, DRCR, DRCRP
Left ward rotation	16 bits	ROL, ROLP, RCL, RCLP
	32 bits	DROL, DROLP, DRCL, DRCLP

(c) Shift instructions

Right ward shift	16 bits	SFR, SFRP, BSFR, BSFRP
	Per device	DSFR, DSFRP
Left ward shift	16 bits	SFL, SFLP, BSFL, BSFLP
	Per device	DSFL, DSFLP

(d) Data processing instructions

Data search	16 bits	SER, SERP
Bit check	16 bits	SUM, SUMP
	32 bits	DSUM, DSUMP
Decode	2.MDSU/n. MDNM/ bits	DECO, DECOP
	16 bits	SEG
Encode	2.MDSU/n. MDNM/ bits	ENCO, ENCOP
Bit set	16 bits	BSET, BSETP
Bit reset	16 bits	BRST, BRSTP
Dissociation	16 bits	DIS, DISP
Association	16 bits	UNI, UNIP

(e) FIFO instructions

Write	16 bits	FIFW, FIFWP
Read	16 bits	FIFR, FIFRP

(f) ASCII instructions

ASCII conversion	ASC
ASCII print	Two types each for PR and PRC

(g) Buffer memory access instructions

Data read	1 word	FROM, FROMP
	2 words	DFRO, DFROP
Data write	1 word	TO, TOP
	2 words	DTO, DTOP

(h) FOR NEXT instruction

Repetition	FOR, NEXT

(i) Data link module instruction

Data read	1 word	LRDP, RFRP
Data write	1 word	LWTP, RTOP

(j) Display instruction

Display reset	LEDR

(k) Other instructions

WDT reset		WDT, WDTP
Fault check		CHK
Status latch		SLT, SLTR
Sampling trace		STRA, STRAR
Carry flag set/reset	1 bit	STC, CLC
Timing clock	1 bit	DUTY

(4) CC-Link dedicated instructions

Link parameter setting	RLPA
Refresh parameter setting	RRPA
Read master station buffer memory	RIFR
Write to master station buffer memory	RITO
Read buffer memory of intelligent remote station	RIRD
Write to buffer memory of intelligent remote station	RIWT
Write to buffer memory of intelligent remote station (with handshaking)	RISEND
Read buffer memory of intelligent remote station (with handshaking)	RIRCV
Read to the word station link register	RDGET
Write to the word station link register	RDPUT
Monitor the word station link register	RDMON

Appendix 1.1 CC-Link Dedicated Instructions

The instructions dedicated to CC-Link are designed to make automatic refresh setting for the AnSHCPU and master module/local module and to make data communication with a remote station connected to CC-Link.
There are 11 different CC-Link dedicated instructions as indicated in Table 1.

Table 1 CC-Link dedicated instruction list

Classification	Instruction name	Description	Instruction execution stations		Stations connected to CC-Link				Refer to
			M	L	M	L	ID	RD	
Network parameter setting	RLPA	Sets the network parameters to the master module of CC-Link.	ϒ	×	×	×	×	×	App 1.1.2
Automatic refresh parameter setting	RRPA	Sets the automatic refresh parameters to the master/local module of CC-Link.	ϒ	ϒ	×	×	×	×	App 1.1.3
Read from automatic updating buffer memory	RIFR	Reads the specified points of data from the automatic updating buffer memory of the master/local module.	ϒ	ϒ	×	×	×	×	App 1.1.4
Write to automatic updating buffer memory	RITO	Writes the specified points of data to the automatic updating buffer memory of the master/local module.	ϒ	ϒ	×	×	×	×	App 1.1.5
Read from remote device station buffer memory	RIRD	Reads the specified points of data from the specified buffer memory of the remote device station.	ϒ	ϒ	ϒ	ϒ	ϒ	×	App 1.1.6
Write to remote device station buffer memory	RIWT	Writes the specified points of date to the specified buffer memory of the remote device station.	ϒ	ϒ	ϒ	ϒ	ϒ	×	App 1.1.7
Read from intelligent device station buffer memory (with handshake)	RIRCV	Reads the specified points of data from the specified buffer memory of the intelligent device station. Handshake is performed using a handshake signal.	ϒ	×	×	×	ϒ	×	App 1.1.8
Write intelligent device station buffer memory (with handshake)	RISEND	Writes the specified points of data to the specified buffer memory of the intelligent device station. Handshake is performed using a handshake signal.	ϒ	×	×	×	ϒ	×	App 1.1.9
Read from remote device station	RDGET	Reads data from a remote device station.	ϒ	×	×	×	×	ϒ	App 1.1.10
Write to remote device station	RDPUT	Writes data to a remote device station.	ϒ	×	×	×	×	ϒ	App 1.1.11
Remote device station monitoring	RDMON	Monitors a remote device station.	ϒ	×	×	×	×	ϒ	App 1.1.12

REMARKS

1) "M", "L", "ID" and "RD" in Table 1. denote the following :
   - M : Master station
   - L : Local station
   - ID : Intelligent device station
   - RD : Remote device station

2) In the "Instruction Execution Stations" and "Object Stations" fields of Table 1, ϒ denotes that the corresponding station is available and × unavailable.
   However, since the availability of the dedicated instructions in Table 1 changes with the module of the station connected to CC-Link, refer to the manual of the module used to confirm the availability.

1.1.1 Instructions for use of the CC-Link dedicated instructions

(1) Different intelligent device stations have different buffer memory capacities.
Refer to the manual of the intelligent device station used.

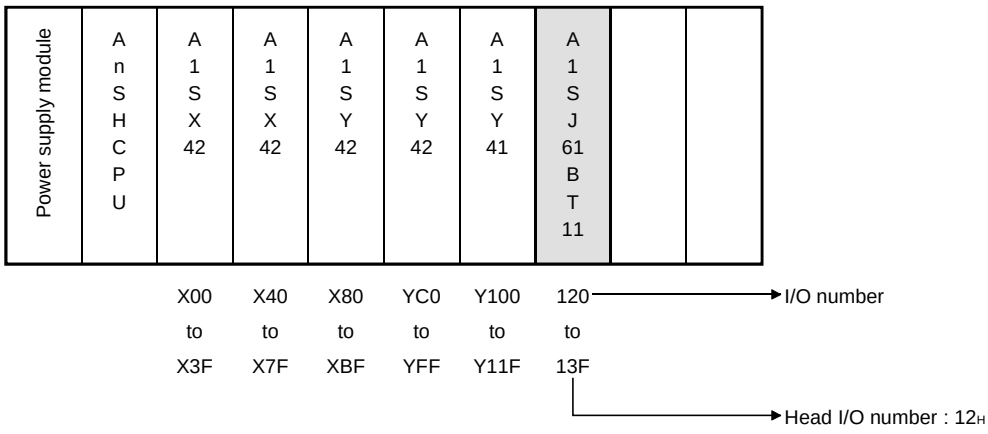
(2) Only one of the RIRD, RIWT, RISEND and RIRCV instructions may be executed for the same station.
If two or more of the RIRD, RIWT, RISEND and RIRCV instructions are executed, the second and subsequent instructions are ignored.

(3) RDGET, RDPUT and RDMON may be executed for the same station separately.
Any of these instructions cannot be executed in two or more locations for the same station.
If any of RDGET, RDPUT and RDMON instructions is used in two or more places, the second and subsequent instructions are ignored.

(4) RIRD, RIWT, RISEND, RIRCV, RDGET, RDPUT and RDMON may be executed for different stations at the same time.
Note that up to 64 instructions may be executed simultaneously.

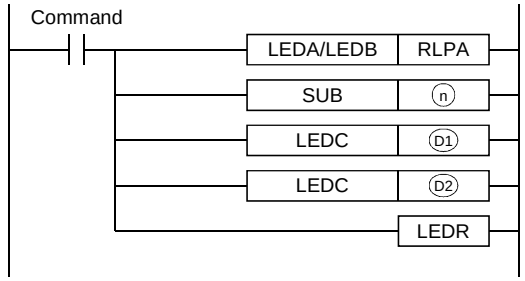
(5) The data of any devices used by the CC-Link dedicated instruction should not be changed until the completion of the instruction.
If the data of the device is changed during execution of the instruction, the CC-Link dedicated instruction cannot be completed properly.

(6) Specify the head I/O number of the master/local module in the CC-Link dedicated instruction.
This head I/O number of the master/local module is the value in the upper 2 digits of the master/local module's I/O number represented in 3 digits.
For example, when the master/local module's I/O number is X/Y120, the head I/O number is 12_H.



1.1.2 Network parameter setting .....RLPA

	Available device																				Digit designation	Number of steps	Subset	Index	Carry flag	Error flag
	Bit device							Word device									Constant		Pointer		Levle					
	X	Y	M	L	S	B	F	T	C	D	W	R	A0	A1	Z	V	K	H	P	I	N					M9012	M9011
(n)																	○	○									
(D1)								○	○	○	○	○											23				○
(D2)		○	○	○	○	○																					



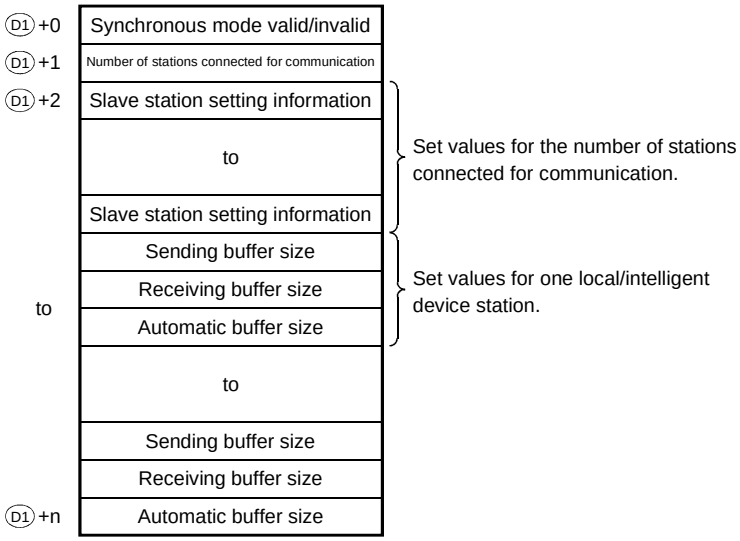
LEDA·····Executed while ON
LEDB·····Executed at leading edge
LEDC····· Device number designated
SUB·····Constant designated

Data to be set

(n)	Head I/O number of object master module
(D1)	Head number of devices which stores link parameters
(D2)	Host station's bit device number which is switched on on completion of execution

Network Parameter Data

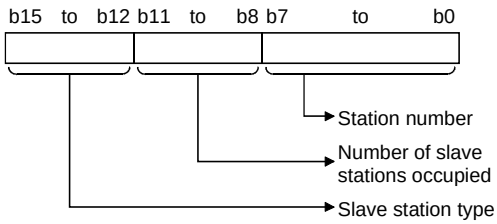
(1) Network parameter setting items



(2) Number of points required for the network parameter area
The following points are required for the network parameter setting :

- Synchronous mode.....1 point
  valid/invalid setting
- Communication station .....1 point
  count setting
- Slave station setting.....Number of points for the number of slave
  information stations connected for communication
- Sending buffer size.....Number of points for the number of local
  and intelligent device stations
- Receiving buffer size .....Number of points for the number of local
  and intelligent device stations
- Automatic update.....Number of points for the number of local
  buffer size and intelligent device stations

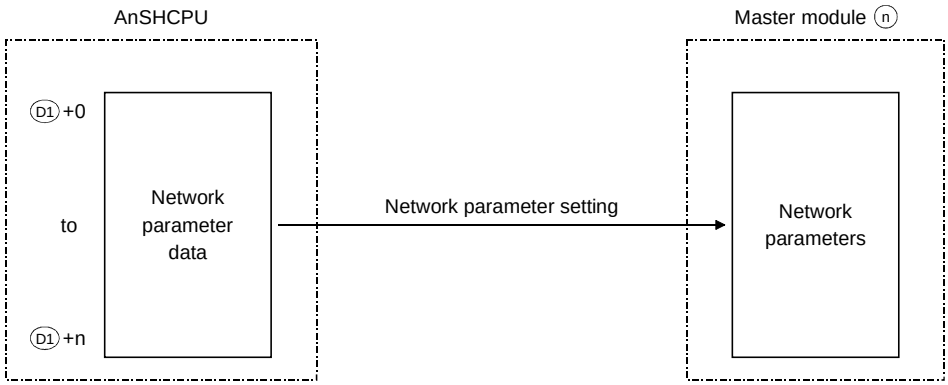
(3) Network parameter settings

<table>
<tr><th>Item</th><th>Set data</th><th>Setting range</th><th>Setting end</th></tr>
<tr><td>Synchronous mode valid/invalid</td><td>Set whether the synchronous mode is valid or invalid.
• When synchronous mode is valid : 0
• When synchronous mode is invalid : 1</td><td>0/1</td><td>User</td></tr>
<tr><td>Number of stations connected for communication</td><td>Set the number of slave stations connected to the master module of CC-Link.</td><td>1 to 64</td><td>User</td></tr>
<tr><td rowspan="4">Slave station setting information</td><td>Set the slave station type, number of slave stations occupied, and station number as indicated below :
 
</td><td>—</td><td rowspan="4">User</td></tr>
<tr><td>• Station number setting
1 to 64 (Setting with BIN)</td><td>b0 to b7
1 to 64
(1H to 40H)</td></tr>
<tr><td>• Set the number of slave stations occupied
<table><tr><th>Number of slave stations occupied</th><th>Setting</th></tr><tr><td>1 station</td><td>1</td></tr><tr><td>2 station</td><td>2</td></tr><tr><td>3 station</td><td>3</td></tr><tr><td>4 station</td><td>4</td></tr></table></td><td>b8 to b11
1 to 4</td></tr>
<tr><td>• Slave station type setting
<table><tr><th>Slave station type</th><th>Setting</th></tr><tr><td>Remote I/O station</td><td>0</td></tr><tr><td>Remote device station</td><td>1</td></tr><tr><td>Local station</td><td rowspan="2">2</td></tr><tr><td>Intelligent device station</td></tr></table></td><td>b12 to b15
0 to 2</td></tr>
<tr><td>Sending buffer size</td><td>Set the number of points transmitted from the master station to a local/intelligent device station.</td><td>*</td><td>User</td></tr>
<tr><td>Receiving buffer size</td><td>Set the number of points transmitted from a local/intelligent device station to the master station.</td><td>*</td><td>User</td></tr>
<tr><td>Automatic updating buffer size</td><td>Set the number of points of the automatic updating buffer used by the master station and local/intelligent device station.</td><td>*</td><td>User</td></tr>
</table>

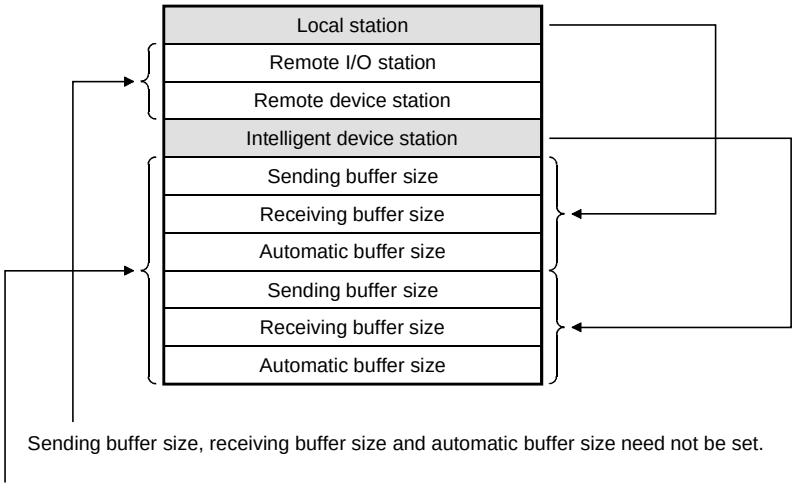
* : To be set in response to the module used.

Functions

(1) When the RLPA instruction is executed, the network parameter data set to the devices beginning with the one specified at D1 is set to the master module specified at n .



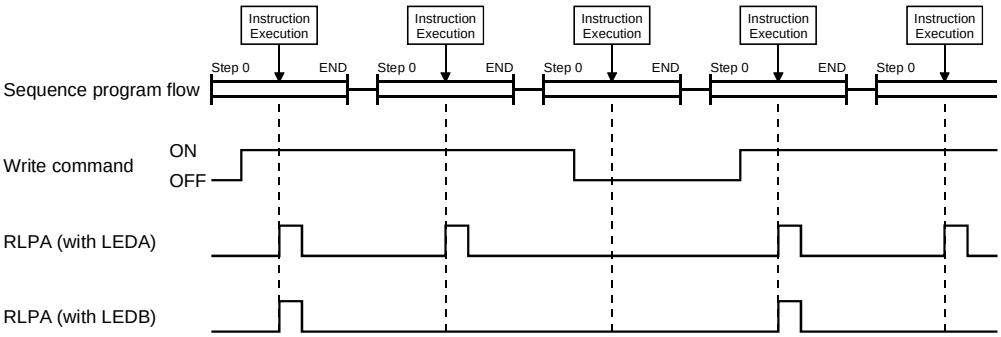
(2) When the slave station type specified is a local/intelligent device station, it is necessary to set the "sending buffer size", "receiving buffer size" and "automatic updating buffer size".
When the slave station type is a remote I/O station or a remote device station, it is not necessary to set the "sending buffer size", "receiving buffer size" and "automatic updating buffer size".



Set sizes for local and intelligent device stations successively.
For remote I/O and remote device stations, their buffer sizes are not set.
When setting for the other stations, therefore, start setting with the frontmost empty position.

(3) After setting of the network parameters, if the RLPA instruction is executed again during RUN to change the network parameters, new data is not used for communication with the slave stations.
When the AnSHCPU is switched to STOP/PAUSE, then to RUN, the new network parameters are used for communication with the slave stations.

Execution Conditions As shown below, when the LEDA instruction is used, the RLPA instruction is executed every scan while the write command is ON. When the LEDB instruction is used, the RLPA instruction is executed only one scan on the leading edge (OFF → ON) of the write command.

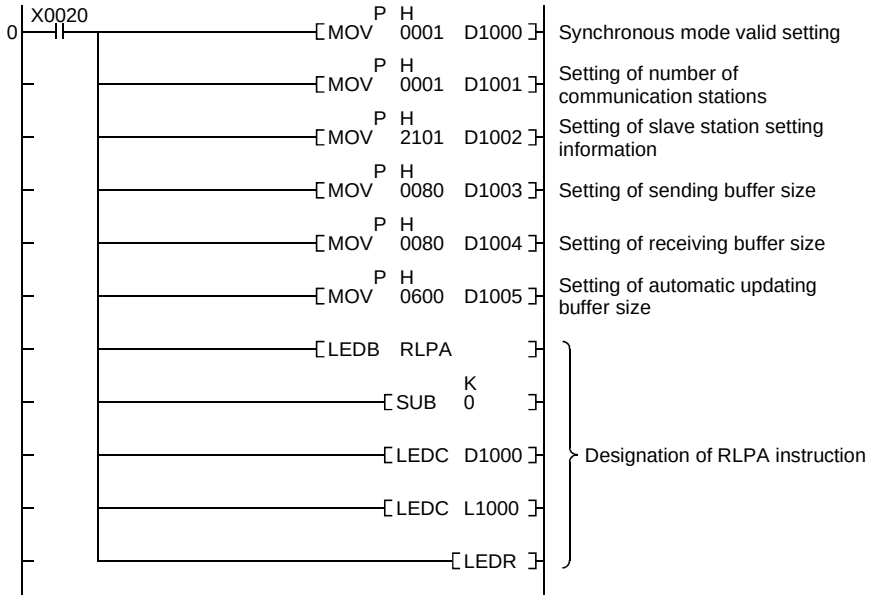


Program Example The following program sets the network parameters to the master module of CC-Link allocated to I/O numbers 000 to 01F.

(1) Network parameter settings

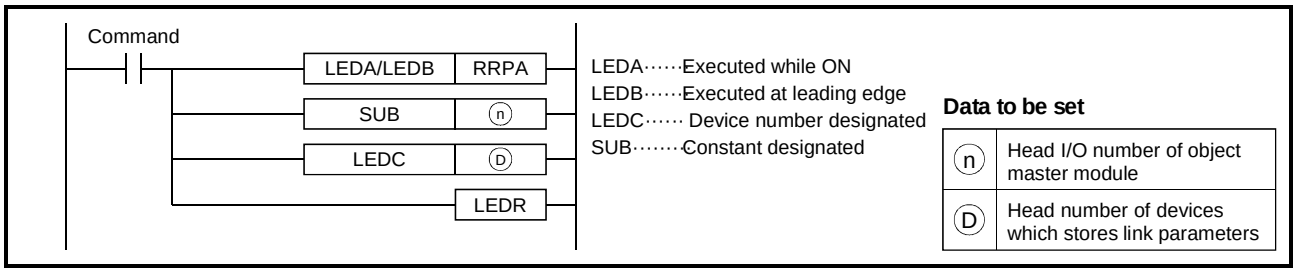
Set item		Set data		Device for storing data
Synchronous mode valid/invalid setting		Synchronous mode	1	D1000
Communication station count setting		1 module	1	D1001
Slave station setting information	Slave station type	Intelligent device station	2	D1002
	Number of slave stations occupied	1 station	1	
	Station number	1	1	
Sending buffer size		128 (80_H) words		D1003
Receiving buffer size		128 (80_H) words		D1004
Automatic buffer size		960 (600_H) words		D1005

2) Program



1.1.3 Automatic refresh parameter setting ..... RRPA

	Available device																				Digit designation	Number of steps	Subset	Index	Carry flag	Error flag
	Bit device							Word device									Constant		Pointer		Levle					
	X	Y	M	L	S	B	F	T	C	D	W	R	A0	A1	Z	V	K	H	P	I	N					M9012	M9011
(n)																	○	○					20				○
(D)								○	○	○	○	○															



Automatic Refresh Parameter Data

(1) Automatic refresh parameter setting items

(D)+ 0	RX's head number	RX refresh range setting
(D)+ 1	AnSHCPU side refreshed device code	
(D)+ 2	AnSHCPU side refreshed device's head number	
(D)+ 3	Number of refresh points	
(D)+ 4	RY's head number	RY refresh range setting
(D)+ 5	AnSHCPU side refreshed device code	
(D)+ 6	AnSHCPU side refreshed device's head number	
(D)+ 7	Number of refresh points	
(D)+ 8	RW's head number	RW refresh range setting
(D)+ 9	AnSHCPU side refreshed device code	
(D)+10	AnSHCPU side refreshed device's head number	
(D)+11	Number of refresh points	
(D)+12	SB's head number	SB refresh range setting
(D)+13	AnSHCPU side refreshed device code	
(D)+14	AnSHCPU side refreshed device's head number	
(D)+15	Number of refresh points	
(D)+16	SW's head number	SW refresh range setting
(D)+17	AnSHCPU side refreshed device code	
(D)+18	AnSHCPU side refreshed device's head number	
(D)+19	Number of refresh points	

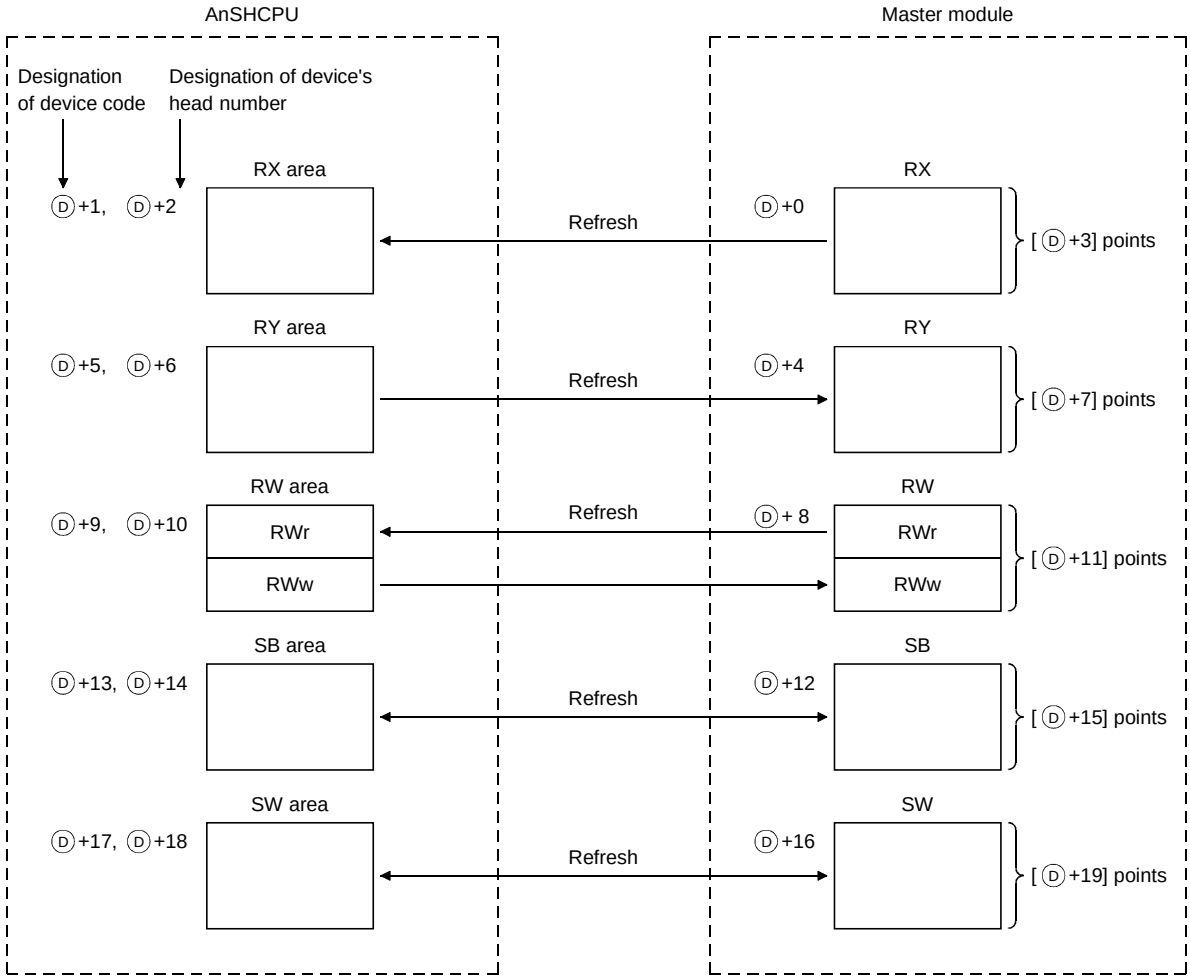
(2) Points for automatic refresh parameter area
Automatic refresh parameter data occupies 20 points from (D1) +0 to (D1) +19.
When there is a device on which automatic refresh will not be performed (RX, RY, RW, SB, SW), set "0" to its refreshed device code or number of refresh points.

(3) Automatic refresh parameter settings

<table>
<tr><th>Item</th><th>Set data</th><th>Setting end</th></tr>
<tr><td>RX's head number</td><td>Set the head number of RX on the master/local module side.</td><td>System</td></tr>
<tr><td>RY's head number</td><td>Set the head number of RY on the master/local module side.</td><td>User</td></tr>
<tr><td rowspan="2">RW's head number</td><td rowspan="2">Set the head number of RW on the master/local module side.</td><td>RWr : System</td></tr>
<tr><td>RWw : User</td></tr>
<tr><td>SB's head number</td><td>Set the head number of SB on the master/local module side.</td><td>System</td></tr>
<tr><td>SW's head number</td><td>Set the head number of SW on the master/local module side.</td><td>System</td></tr>
<tr><td>AnSHCPU side refreshed device code</td><td>Set the AnSHCPU side device with the following device code :
<table><tr><td>Device name</td><td>X</td><td>Y</td><td>M</td><td>B</td><td>T</td><td>C</td><td>D</td><td>W</td><td>R</td></tr><tr><td>Device code</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td><td>9</td></tr></table>0 : No automatic refresh setting</td><td>User</td></tr>
<tr><td>AnSHCPU side refreshed device's head number</td><td>Set the head device number on the AnSHCPU side.</td><td>User</td></tr>
<tr><td>Number of refresh points</td><td>Set the number of points on which automatic refresh will be performed.
0 : No automatic refresh setting</td><td>User</td></tr>
</table>

Functions

(1) Set the devices and numbers of points on which automatic refresh will be performed between the AnSHCPU and master/local module.
When the FROM/TO instruction is used to read/write data from/to the master/local module, the RRPA instruction need not be executed.



(2) When the RRPA instruction is executed, the automatic refresh settings are registered to the AnSHCPU and automatic refresh is performed between the AnSHCPU and master/local module.

(3) The following table indicates whether refreshed devices may be set or not.

Refreshed device	Device code	Setting				
		RX	RY	RW	SB	SW
X *1	1	ϒ	ϒ	ϒ	ϒ	ϒ
Y *1	2	ϒ	ϒ	ϒ	ϒ	ϒ
M (L, S)	3	ϒ	ϒ	ϒ	ϒ	ϒ
B *2	4	ϒ	ϒ	ϒ	ϒ	ϒ
T	5	ϒ	ϒ	ϒ	ϒ	ϒ
C	6	ϒ	ϒ	ϒ	ϒ	ϒ
D	7	ϒ	ϒ	ϒ	ϒ	ϒ
W *2	8	ϒ	ϒ	ϒ	ϒ	ϒ
R	9	ϒ	ϒ	ϒ	×	×

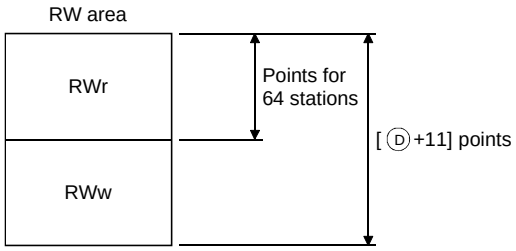
ϒ : May be set, × : Cannot be set

REMARKS

*1 : Set the range which is not being used by the main base, extension base and data link.
*2 : Set B and W in the range not used by data link.

(4) If the automatic refresh parameters are changed (RRPA instruction is executed) during RUN, new data is not used for control. When the AnSHCPU is switched to STOP/PAUSE, then to RUN, the new automatic refresh parameters are used for refreshing.

(5) Set RWr and RWw areas in the RW area.
Since the RWw area is set after the RWr area reserved for 64 stations, set RWw as shown below.



(6) Instructions for setting refreshed device in SB and SW

(a) In SB and SW, set refreshed devices within the specified number of points starting from the head number. SB0000 to SB003F are refreshed from the AnSHCPU to the master module, and SB0040 to SB00FF are refreshed from the master module to the AnSHCPU.

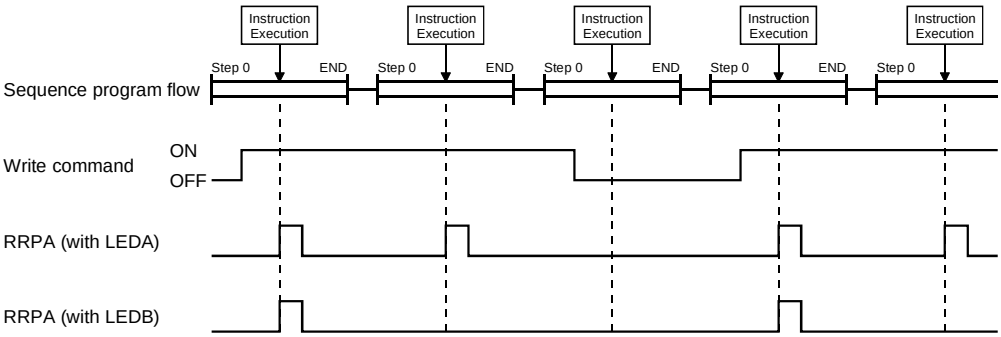
(b) File registers (R) cannot be specified as refreshed devices in SB and SW.
If file registers are set in SB or SW and written to the AnSHCPU, an instruction code error occurs and the AnSHCPU is inoperative.

(c) The device range set for refreshed devices in SB or SW should not be specified as a latch range.

(d) The SB and SW refresh ranges set with the RRPA instruction during power-on cannot be changed.

Execution Conditions

As shown below, when the LEDA instruction is used, the RRPA instruction is executed every scan while the write command is ON. When the LEDB instruction is used, the RRPA instruction is executed only one scan on the leading edge (OFF → ON) of the write command.



Operation Errors

Any of the following conditions will result in an operation error and the error flag (M9011) switch on.

Description	Error code	
	D9008	D9092
The device code specified is 0 or other than 1 to 9	50	503
The head number of a bit device is not a multiple of 16		
The number of refresh points is not a multiple of 16		

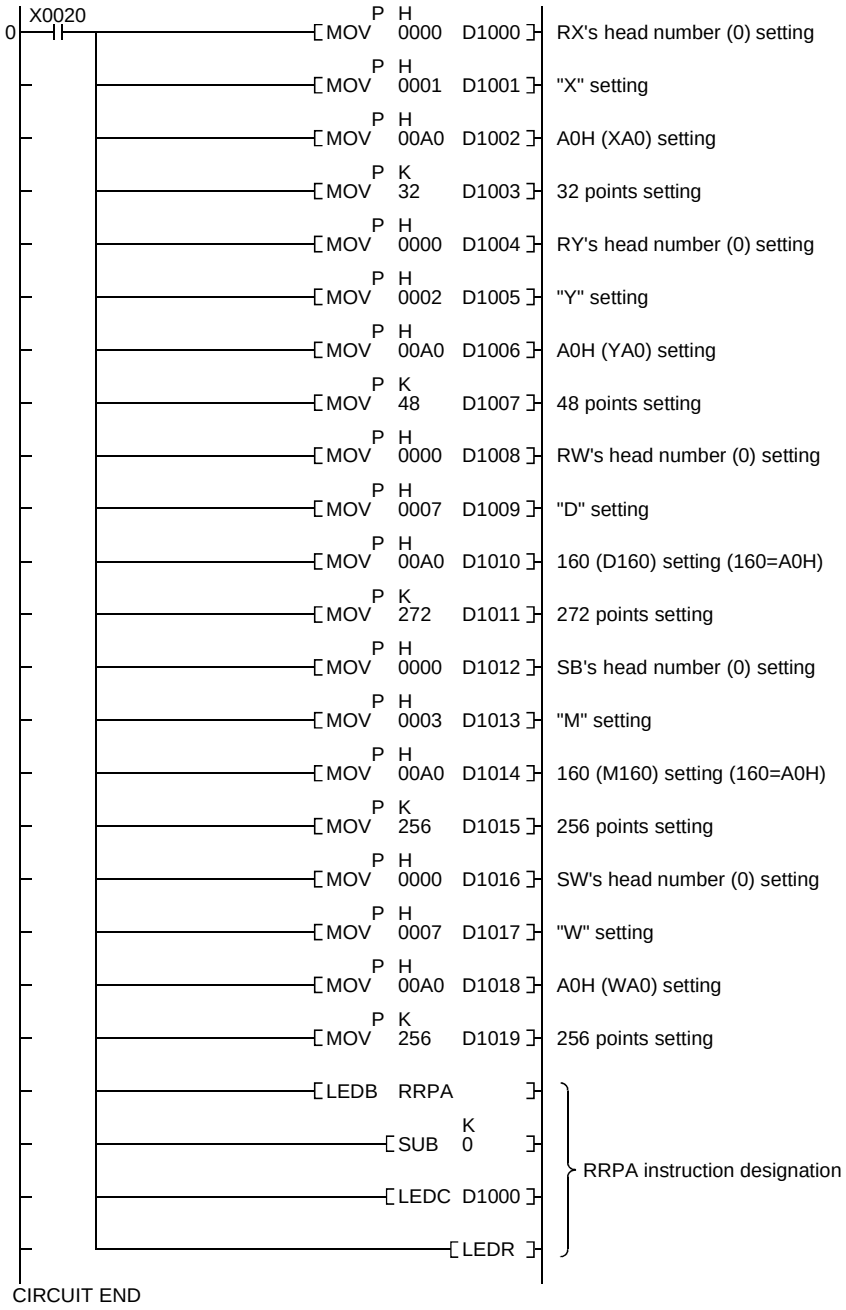
Program Example

The following program sets the automatic refresh parameters to the master module of CC-Link allocated to I/O numbers 000 to 01F.

(1) Automatic refresh parameter settings and data storage devices

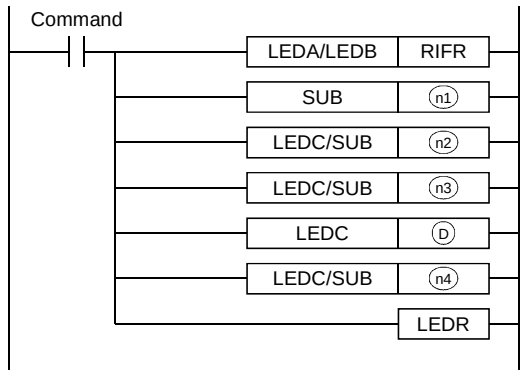
Setting item	Set data	Data storage device
RX's head number	0	D1000
AnSHCPU side refreshed device code	X (1)	D1001
AnSHCPU side refreshed device's head number	A0H	D1002
Number of refresh points	32	D1003
RY's head number	0	D1004
AnSHCPU side refreshed device code	Y (2)	D1005
AnSHCPU side refreshed device's head number	A0H	D1006
Number of refresh points	48	D1007
RW's head number	0	D1008
AnSHCPU side refreshed device code	D (7)	D1009
AnSHCPU side refreshed device's head number	160 (A0H)	D1010
Number of refresh points	272	D1011
SB's head number	0	D1012
AnSHCPU side refreshed device code	M (3)	D1013
AnSHCPU side refreshed device's head number	160 (A0H)	D1014
Number of refresh points	256	D1015
SW's head number	0	D1016
AnSHCPU side refreshed device code	W (8)	D1017
AnSHCPU side refreshed device's head number	A0H	D1018
Number of refresh points	256	D1019

(2) Program example



1.1.4 Read from automatic updating buffer memory ····· RIFR

	Available device																				Digit designation	Number of steps	Subset	Index	Carry flag	Error flag
	Bit device							Word device									Constant		Pointer		Levle					
	X	Y	M	L	S	B	F	T	C	D	W	R	A0	A1	Z	V	K	H	P	I	N					M9012	M9011
(n1)																	○	○								
(n2)								○	○	○	○	○					○	○								
(n3)								○	○	○	○	○					○	○				29				○
(D)								○	○	○	○	○														
(n4)								○	○	○	○	○					○	○								

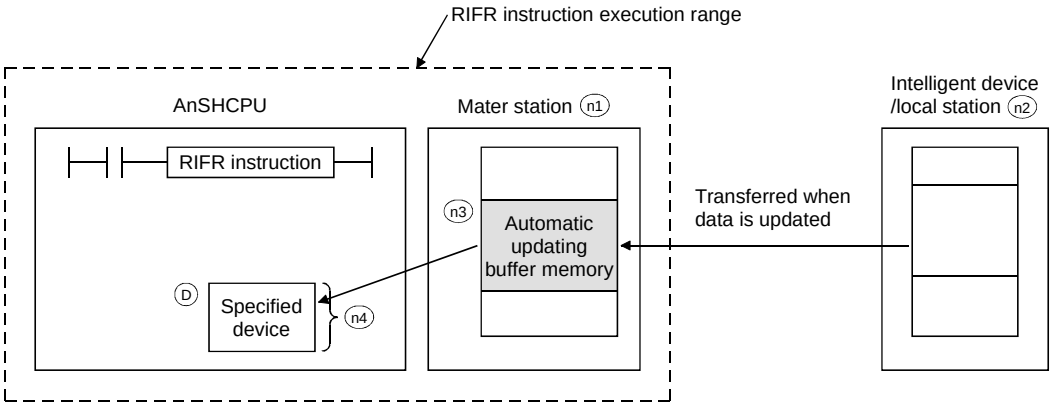


Data to be set

(n1)	Head I/O number of object master module
(n2)	Read destination designation • Intelligent device station : Station numbers 1 to64 (only when the host station is the master station) • Random access buffer : FFH
(n3)	Intelligent device station's sending/receiving buffer address specified in master station (Specify the offset address)
(D)	Device which will store the read data
(n4)	Number of points read : 1 to 8192

Functions

(1) Reads the points of data specified at (n4) from the automatic updating buffer memory address specified at (n3) for the station having the station number specified at (n2) in the master module specified at (n1) and stores that data into the devices starting from the one specified at (D).



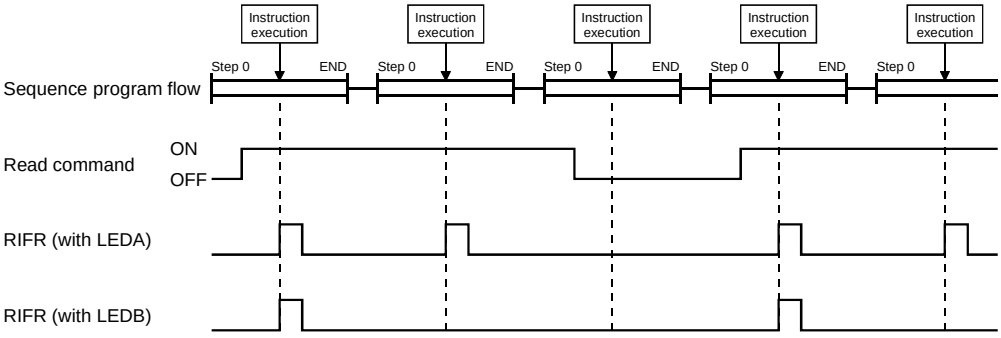
(2) When executed, the RIFR instruction reads data from the automatic updating buffer of the master module.

(3) Up to 8192 points may be read by the RIFR instruction.

(4) To set the number of automatic updating buffer memory points, make the automatic updating buffer size setting using the network parameter instruction (RLPA instruction).

Execution Conditions

As shown below, when the LEDA instruction is used, the RIFR instruction is executed every scan while the read command is ON. When the LEDB instruction is used, the RIFR instruction is executed only one scan on the leading edge (OFF → ON) of the read command.



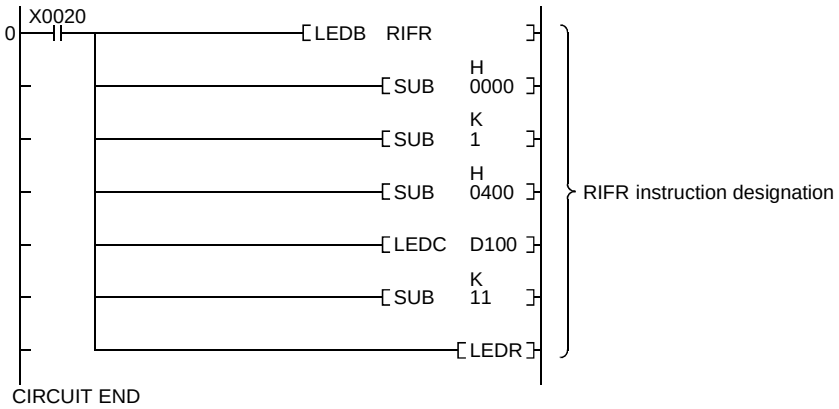
Operation Errors

Either of the following conditions will result in an operation error and the error flag (M9011) switch on.

Description	Error code	
	D9008	D9092
The buffer address specified is outside the range of automatic updating buffer memory designation range.	50	503
The number of refresh points is greater than 8192.		

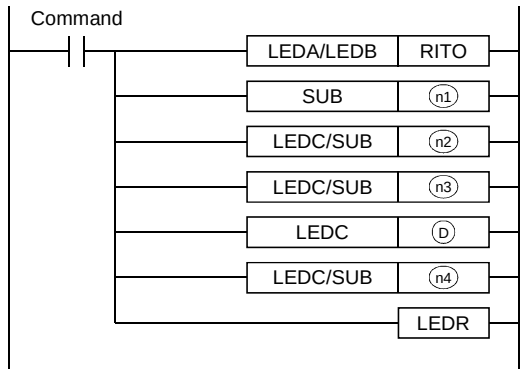
Program Examples

The following program reads 11 points of data to D100 and thereafter from 400H of the automatic updating buffer memory set to station number 1 in the master module of CC-Link allocated to I/O numbers 000 to 01F.



1.1.5 Write to automatic updating buffer memory .....RITO

	Available device																				Digit designation	Number of steps	Subset	Index	Carry flag	Error flag
	Bit device							Word device									Constant		Pointer		Levle					
	X	Y	M	L	S	B	F	T	C	D	W	R	A0	A1	Z	V	K	H	P	I	N					M9012	M9011
(n1)																	○	○								
(n2)								○	○	○	○	○					○	○								
(n3)								○	○	○	○	○					○	○				29				○
(D)								○	○	○	○	○														
(n4)								○	○	○	○	○					○	○								

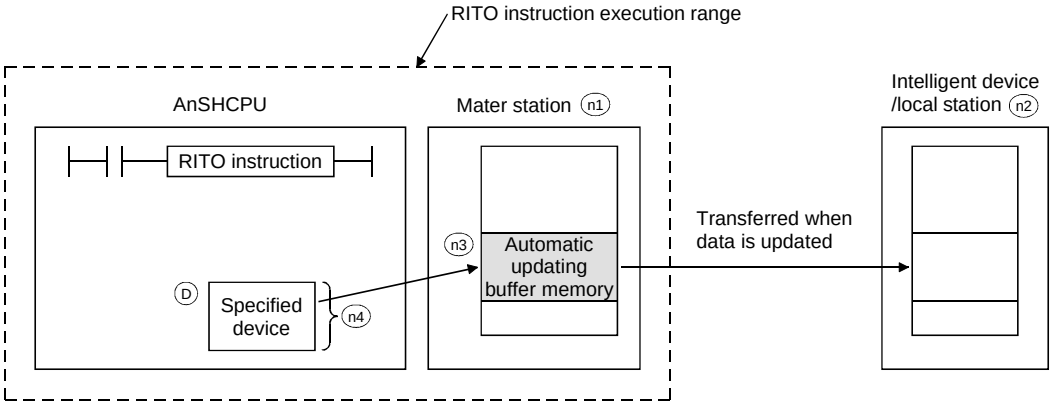


Data to be set

(n1)	Head I/O number of object master module
(n2)	Write destination designation • Intelligent device station : Station numbers 1 to 64 (only when the host station is the master station) • Random access buffer : FFH
(n3)	Intelligent device station's sending/receiving buffer address specified in master station (Specify the offset address)
(D)	Device which will store the written data
(n4)	Number of points written : 1 to 8192

Functions

(1) Writes the points of data specified at (n4) from the devices beginning with the one specified at D to the automatic updating buffer memory addresses beginning with the specified one at (n3) for the station having the station number specified at (n2) in the master module specified at (n1).



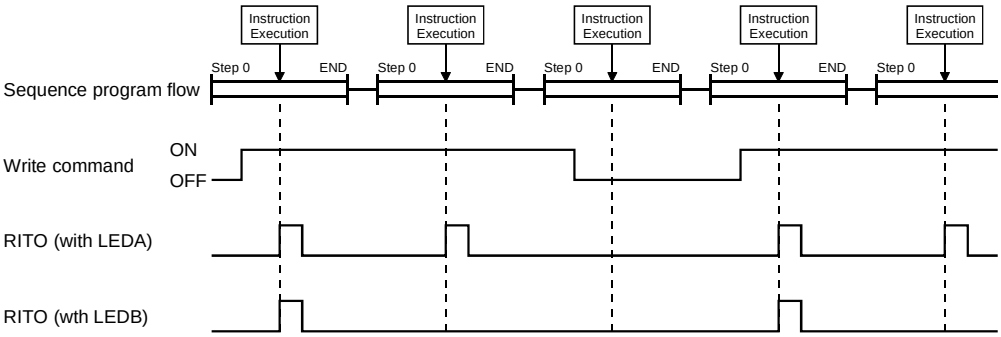
(2) When executed, the RITO instruction writes data.

(3) Up to 8192 points may be written by the RITO instruction.

(4) To set the number of automatic updating buffer memory points, make the automatic updating buffer size setting using the network parameter instruction (RLPA instruction).

Execution Conditions

As shown below, when the LEDA instruction is used, the RITO instruction is executed every scan while the write command is ON. When the LEDB instruction is used, the RITO instruction is executed only one scan on the leading edge (OFF → ON) of the write command.



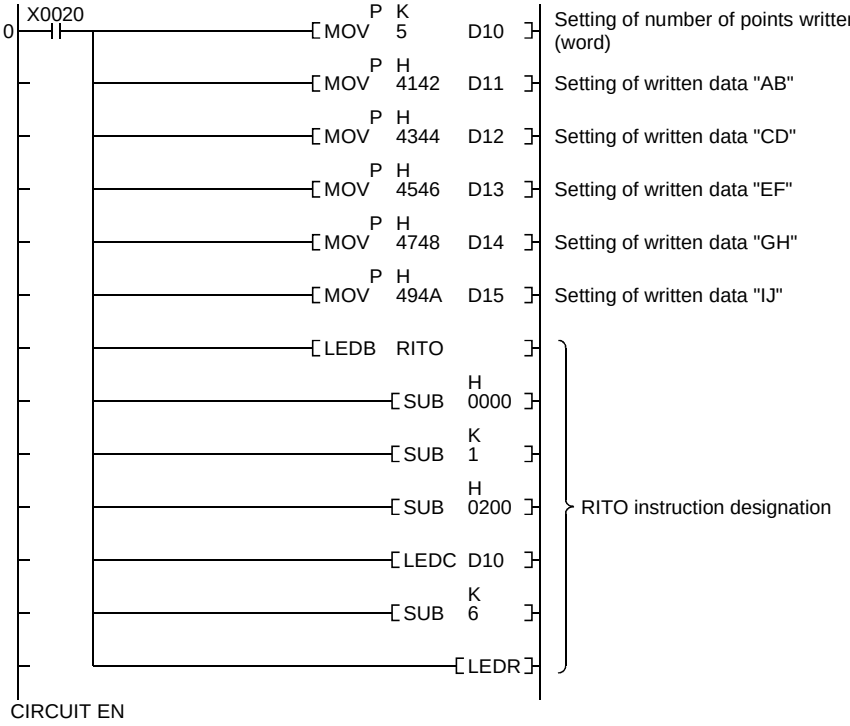
Operation Errors

Either of the following conditions will result in an operation error and the error flag (M9011) switch on.

Description	Error code	
	D9008	D9092
The buffer address specified is outside the range of automatic updating buffer memory designation range.	50	503
The number of refresh points is greater than 8192.		

Program Examples

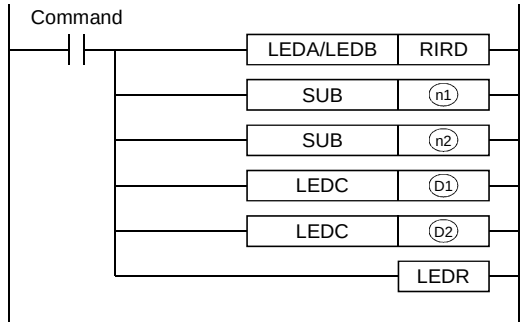
The following program writes "ABCDEFGHIJ" to 200H and subsequent addresses of the automatic updating buffer memory for the station set to station number 1 in the master module of CC-Link allocated to I/O numbers 000 to 01F.



MEMO

1.1.6 Read from remote station buffer memory .....RIRD

	Available device																				Digit designation	Number of steps	Subset	Index	Carry flag	Error flag
	Bit device							Word device									Constant		Pointer		Levle					
	X	Y	M	L	S	B	F	T	C	D	W	R	A0	A1	Z	V	K	H	P	I	N					M9012	M9011
n1																	○	○					26				○
n2																	○	○									
D1								○	○	○	○	○															
D2		○	○	○	○	○																					



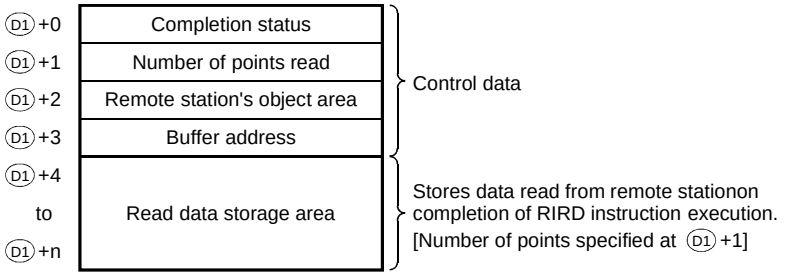
LEDA·····Executed while ON
LEDB·····Executed at leading edge
LEDC····· Device number designated
SUB·····Constant designated

Data to be set

n1	Head I/O number of object master/local module
n2	Remote station number • When the host station is the master station : 1 to 64 • Local station : 0 to 64
D1	Device for storing control data and read data
D2	Bit device number which is switched on on completion of execution

Control Data

(1) Control data setting items



(2) Number of control data area points
Data read from a remote station is stored into the area after the 4 points of control data [D1 +0 to D1 +3].
Reserve the control data area for 4 points + [number of points specified at D1 +1] successively.

REMARKS

1) A remote station is a generic term for an intelligent device station and a local station.

(3) Control data

Item	Set data	Setting range	Setting end
Completion status	Status on completion of instruction execution is stored. 0 : No error Other than 0 : Error code *1	—	System
Number of points read	Specify the number of data read (word basis).	1 to 480 *2	User
Remote station's object area	• Set "0004H" when accessing the buffer memory of an intelligent device station. • Set "2004H" when accessing the random access buffer memory of a local station.	0004H 2004H	User
Buffer memory address	Specify the head address of the buffer memory.	*3	User
Read data	—	—	System

REMARKS

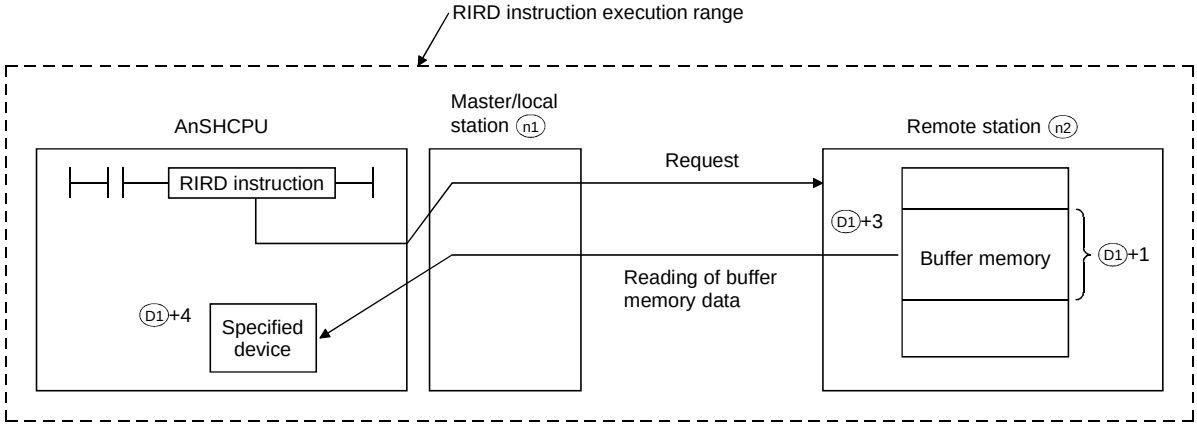
1) *1 : For error codes at error occurrence, refer to the following manual.
Control & Communication-Link System Master · Local Module type AJ65BT11/A1SJ61BT11 User's Manual

2) *2 : Indicates the maximum number of data read.
Set a value within the remote station buffer memory capacity and parameter-set receiving buffer area setting range.

3) *3 : Refer to the manual of the remote station from which data is read.
When specifying the random access buffer memory, set the address with the head of the random access buffer memory defined as 0.

Functions

(1) Reads the points of data specified at (D1) +1 from the buffer memory address specified at [D1 +3] in the remote station having the station number specified at (n2) and connected to the master/local module specified at (n1), and stores that data into the devices starting from the one specified at (D1) +4.
On completion of reading, the bit device specified at (D2) switches on only one scan.
On abnormal completion, the bit device at (D2) +1 switches on only one scan.



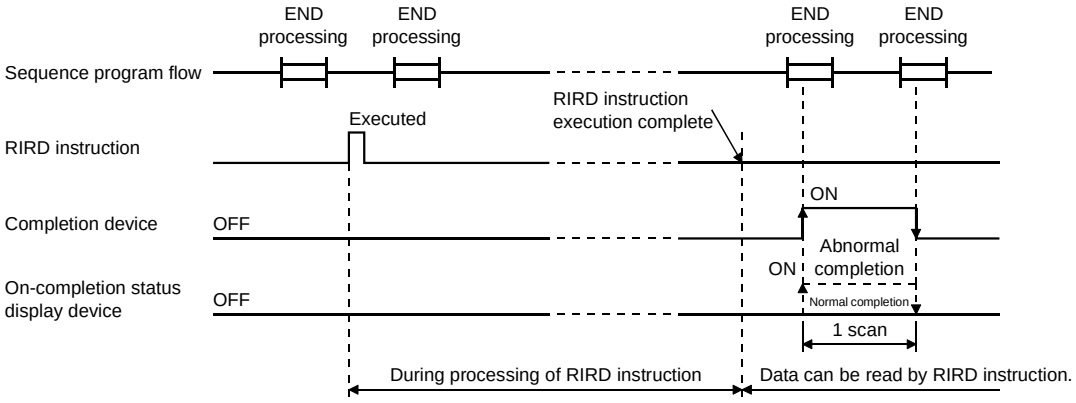
(2) The RIRD instruction may be executed for two or more remote stations at the same time.
However, this instruction cannot be executed for the same remote station in two or more locations at the same time.

(3) Before executing the RIRD instruction, set the network parameters using the RLPA instruction (network parameter setting).
If the RIRD instruction is executed without the network parameters set, abnormal completion will occur and "4B00H" will be stored into the completion status.

(4) No processing will be performed if the number of read points specified at (D1) +1 is "0".

Execution Conditions

When the LEDA instruction is used, the RIRD instruction is executed every scan while the read command is ON. When the LEDB instruction is used, the RIRD instruction is executed only one scan on the leading edge (OFF → ON) of the read command.
Note that several scans will be required until the completion of read processing by the RIRD instruction. Therefore, execute the next RIRD instruction after the completion device has switched on.
(The RIRD instruction executed before the completion of RIRD instruction execution is ignored.)



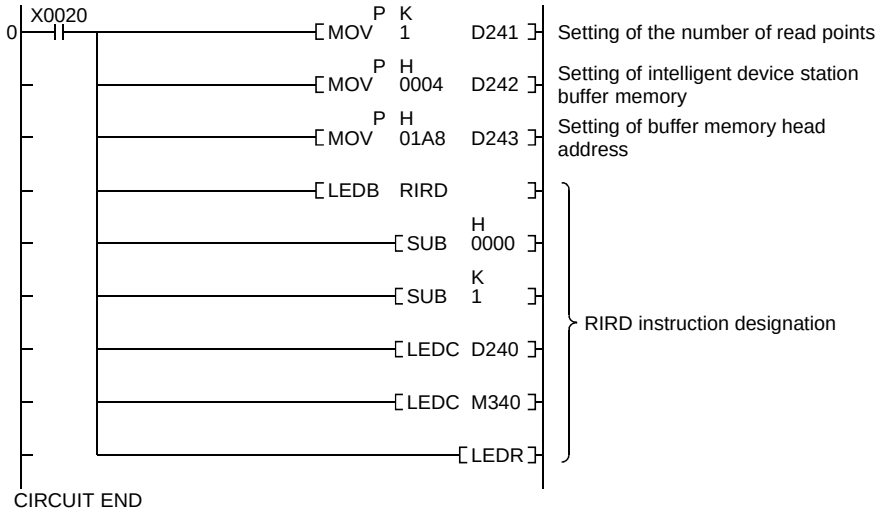
Operation Error

The following condition will result in an operation error and the error flag (M9011) switch on.

Description	Error code	
	D9008	D9092
The number of read points specified at (D1) +1 is outside the range 0 to 480.	50	503

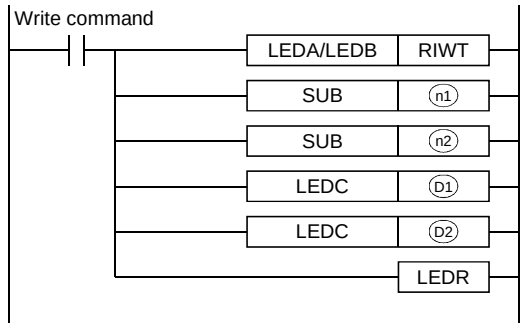
Program Example

The following program reads 1 point of data from 1A8H of the buffer memory of the intelligent device station having station number 1 and connected to the master module of CC-Link allocated to I/O numbers 000 to 01F.



1.1.7 Write to remote station buffer memory..... RIWT

	Available device																				Digit designation	Number of steps	Subset	Index	Carry flag	Error flag
	Bit device							Word device									Constant		Pointer		Levle					
	X	Y	M	L	S	B	F	T	C	D	W	R	A0	A1	Z	V	K	H	P	I	N					M9012	M9011
n1																	○	○								
n2																	○	○					26				○
D1								○	○	○	○	○														
D2		○	○	○	○	○																				

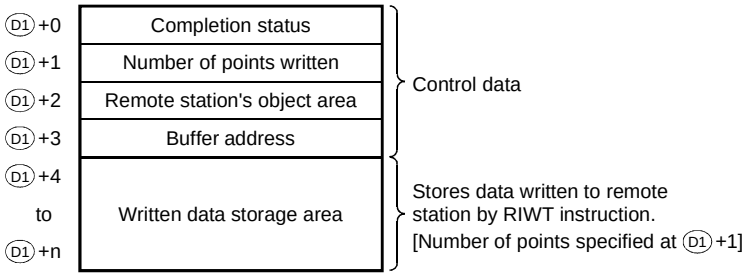


LEDA·····Executed while ON
LEDB·····Executed at leading edge
LEDC····· Device number designated
SUB·····Constant designated

Data to be set

n1	Head I/O number of object master/local module
n2	Remote station number • When the host station is the master station : 1 to 64 • Local station : 0 to 64
D1	Device for storing control data and written data
D2	Bit device number which is switched on on completion of execution

Control Data (1) Control data setting items



(2) Control data

Item	Set data	Setting range	Setting end
Completion status	Status on completion of instruction execution is stored. 0 : No error Other than 0 : Error code *1	—	System
Number of points written	Specify the number of data written (word basis).	1 to 480 *2	User
Remote station's object area	• Set "0004H" when accessing the buffer memory of an intelligent device station. • Set "2004H" when accessing the random access buffer memory of a local station.	0004H 2004H	User
Buffer memory address	Specify the head address of the buffer memory.	*3	User
Written data	——	—	User

REMARKS

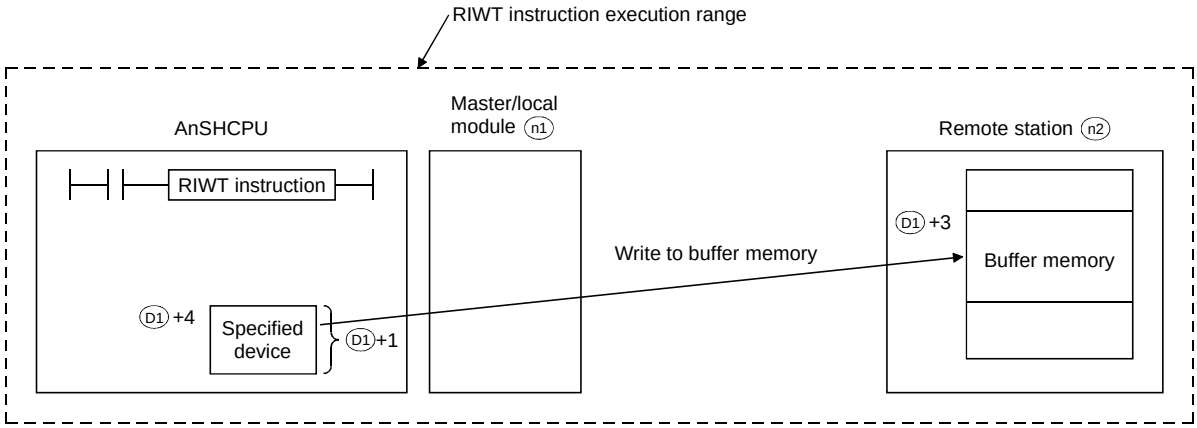
1) *1 : For error codes at error occurrence, refer to the following manual.
Control & Communication-Link System Master · Local Module type AJ65BT11/A1SJ61BT11 User's Manual

2) *2 : Indicates the maximum number of data written.
Set a value within the remote station buffer memory capacity and parameter-set receiving buffer area setting range.

3) *3 : Refer to the manual of the remote station to which data is written.
When specifying the random access buffer memory, set the address with the head of the random access buffer memory defined as 0.

Functions

(1) Writes the points of data specified at (D1) +1 from the devices beginning with the one specified at (D1) +4 to the buffer memory address specified at [(D1) +3] in the remote station having the station number specified at (n2) and connected to the master/local module specified at n1 , and stores that data into.
On completion of writing, the bit device specified at (D2) switches on only one scan.
On abnormal completion, the bit device at (D2) +1 switches on only one scan.



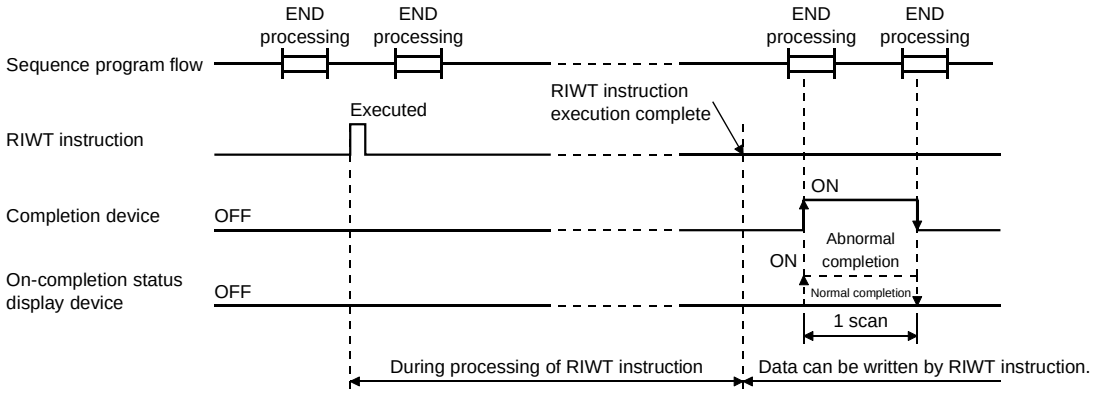
(2) The RIWT instruction may be executed for two or more remote stations at the same time.
However, this instruction cannot be executed for the same remote station in two or more locations at the same time.

(3) Before executing the RIWT instruction, set the network parameters using the RLPA instruction (network parameter setting).
If the RIWT instruction is executed without the network parameters set, abnormal completion will occur and "4B00H" will be stored into the completion status.

(4) No processing will be performed if the number of written points specified at (D1) +1 is "0".

Execution Conditions

When the LEDA instruction is used, the RIWT instruction is executed every scan while the write command is ON. When the LEDB instruction is used, the RIWT instruction is executed only one scan on the leading edge (OFF → ON) of the write command.
Note that several scans will be required until the completion of write processing by the RIWT instruction. Therefore, execute the next RIWT instruction after the completion device has switched on.
(The RIWT instruction executed before the completion of RIWT instruction execution is ignored.)



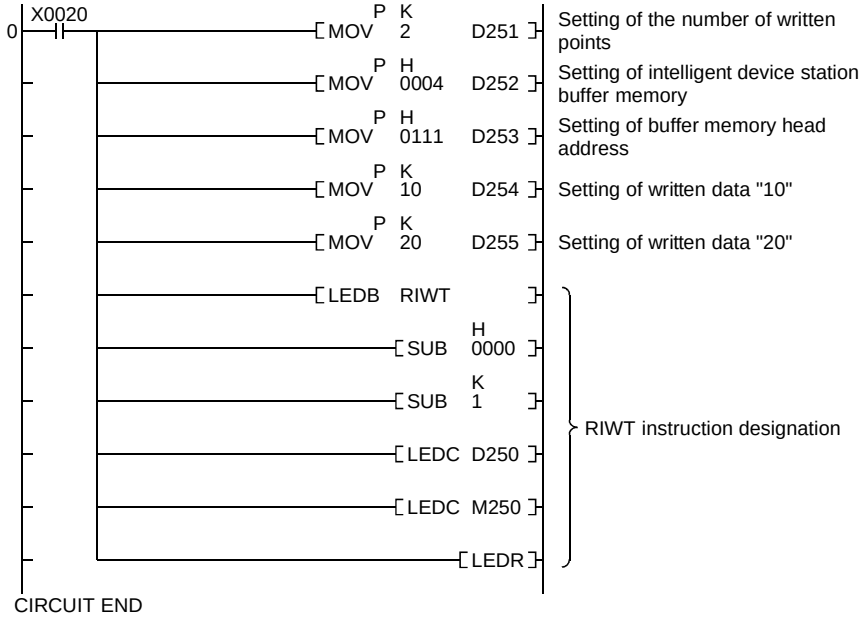
Operation Error

The following condition will result in an operation error and the error flag (M9011) switch on.

Description	Error code	
	D9008	D9092
The number of written points specified at (D1) +1 is outside the range 0 to 480.	50	503

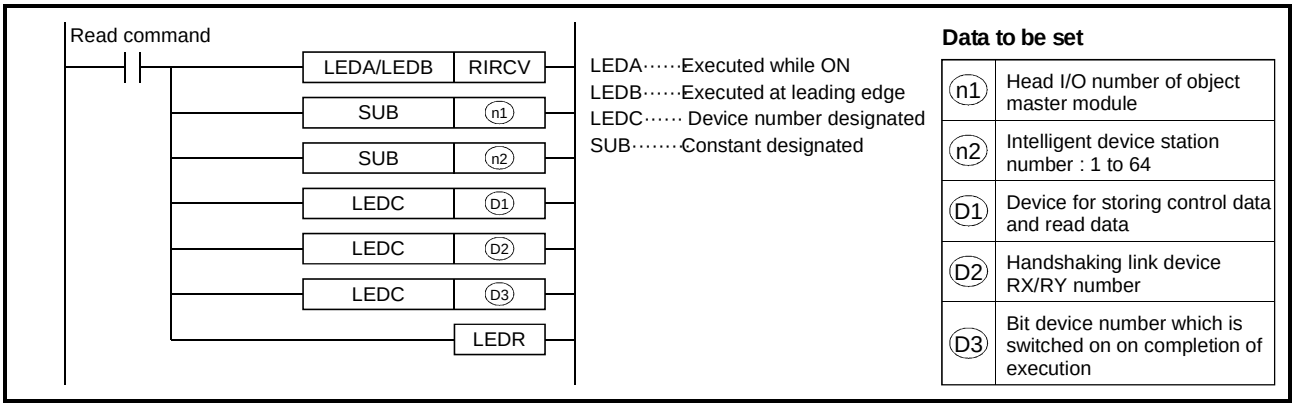
Program Example

The following program writes data 10 and 20 to 111H and 112H of the buffer memory of the intelligent device station having station number 1 and connected to the master module of CC-Link allocated to I/O numbers 000 to 01F.



1.1.8 Read from intelligent device station buffer memory (with handshake) RIRCV

	Available device																				Digit designation	Number of steps	Subset	Index	Carry flag	Error flag
	Bit device							Word device									Constant		Pointer		Levle						
	X	Y	M	L	S	B	F	T	C	D	W	R	A0	A1	Z	V	K	H	P	I	N					M9012	M9011
n1																	○	○					29				○
n2																	○	○									
D1								○	○	○	○	○															
D2								○	○	○	○	○															
D3		○	○	○	○	○																					

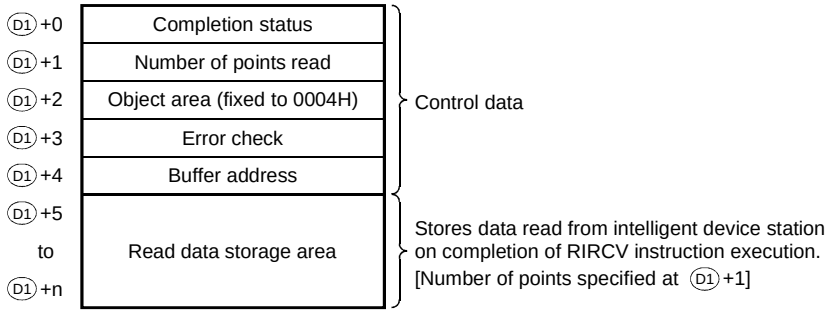


Data to be set

n1	Head I/O number of object master module
n2	Intelligent device station number : 1 to 64
D1	Device for storing control data and read data
D2	Handshaking link device RX/RY number
D3	Bit device number which is switched on on completion of execution

Control Data

(1) Control data setting items



(2) Number of control data area points
Data read from an intelligent device station is stored into the area after the 5 points of control data [D1 +0 to D1 +4].
Reserve the control data area for 5 points + [number of points specified at D1 +1] successively.

(3) Control data

Item	Set data	Setting range	Setting end
Completion status	Status on completion of instruction execution is stored. 0 : No error Other than 0 : Error code *1	—	System
Number of points read	Specify the number of data read (word basis).	1 to 480 *2	User
Object area	Set "0004_H" when accessing the buffer memory of an intelligent device station.	0004_H	User
Error check	Specify the error check device. 0 : Completion status is used for error check. Other than 0 : RX_{+1} is used for error check.	0, 1	User
Buffer memory address	Specify the head address of the buffer memory.	*3	User
Read data	——	—	System

REMARKS

1) *1 : For error codes at error occurrence, refer to the following manual.
Control & Communication-Link System Master. Local Module type AJ65BT11/A1SJ61BT11 User's Manual

2) *2 : Indicates the maximum number of data read.
Set a value within the intelligent device station buffer memory capacity and parameter-set receiving buffer area setting range.

3) *3 : Refer to the manual of the intelligent device station from which data is read.

Handshaking Link Devices

(1) Handshaking link device setting items

(D2)+0	RX	RY
(D2)+1	RWr	

(2) Setting of handshaking link devices

Item	Set data	Setting range	Setting end
RX	Specify the handshaking RX number of the intelligent device station.	0 to 127	User *2
RY	Specify the handshaking RY number of the intelligent device station.	0 to 127	User *2
RWr	Specify the handshaking RWr number of the intelligent device station.	0 to 15 FF *1	User *2

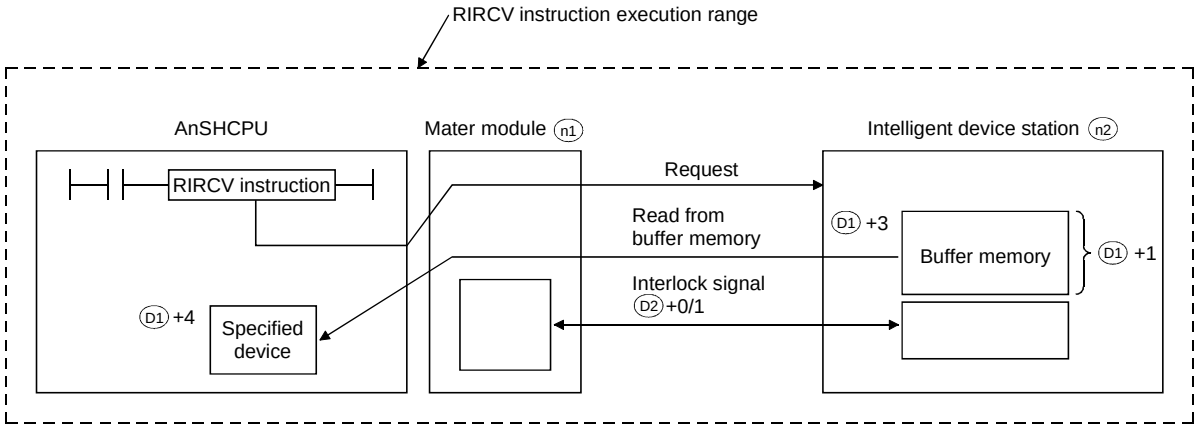
POINTS

(1) *1 : When FF_H is set, no number is specified.

(2) *2 : The RX, RY and RW numbers used are set by the user.
Note that RX and RY ON/OFF control and RW data setting are performed by the system and cannot be changed by the user.
If RX, RY and RW are changed by the user, the RIRVC instruction will not be completed properly.

Functions

(1) Reads the points of data specified at (D1) +1 from the buffer memory address specified at [D1 +3] in the intelligent device station having the station number specified at n2 and connected to the master module specified at n1 , and stores that data into the devices starting from the one specified at D1 +4.
On completion of reading, the bit device specified at (D2) switches on only one scan.
On abnormal completion, the bit device at (D2) +1 switches on only one scan.



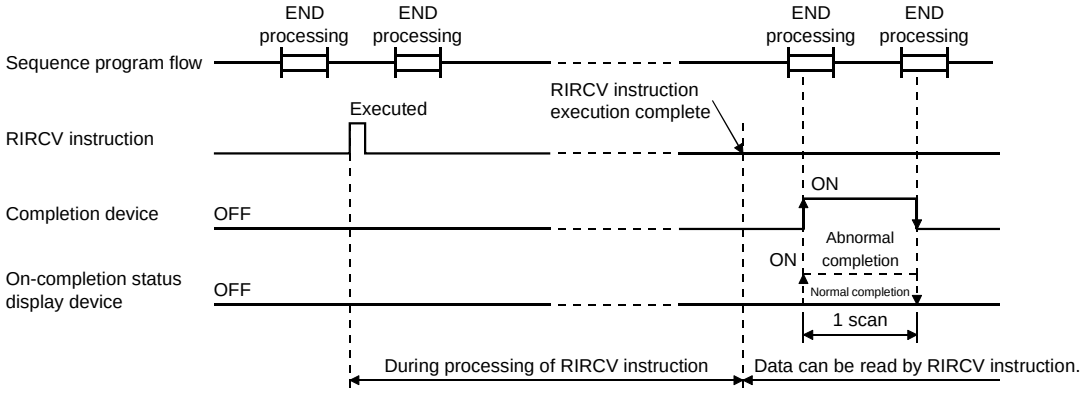
(2) The RIRCV instruction may be executed for two or more intelligent device stations at the same time.
However, this instruction cannot be executed for the same intelligent device station in two or more locations at the same time.

(3) Before executing the RIRCV instruction, set the network parameters using the RLPA instruction (network parameter setting).
If the RIRCV instruction is executed without the network parameters set, abnormal completion will occur and "4B00H" will be stored into the completion status.

(4) No processing will be performed if the number of read points specified at (D1) +1 is "0".

Execution Conditions

When the LEDA instruction is used, the RIRCV instruction is executed every scan while the read command is ON. When the LEDB instruction is used, the RIRCV instruction is executed only one scan on the leading edge (OFF → ON) of the read command.
Note that several scans will be required until the completion of read processing by the RIRCV instruction. Therefore, execute the next RIRCV instruction after the completion device has switched on.
(The RIRCV instruction executed before the completion of RIRCV instruction execution is ignored.)



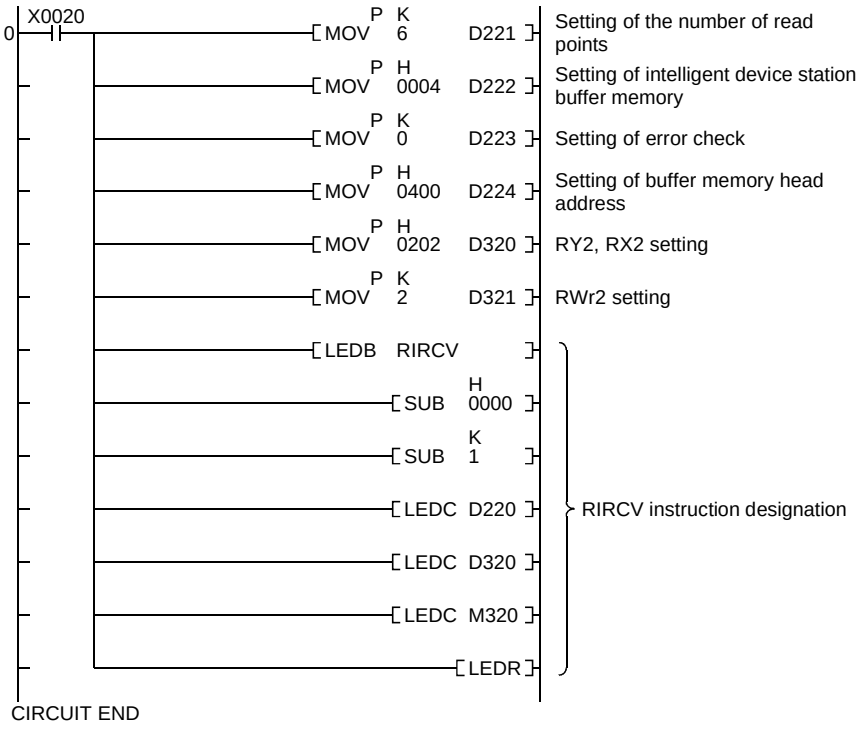
Operation Error

The following condition will result in an operation error and the error flag (M9011) switch on.

Description	Error code	
	D9008	D9092
The number of read points specified at (D1) +1 is outside the range 0 to 480.	50	503

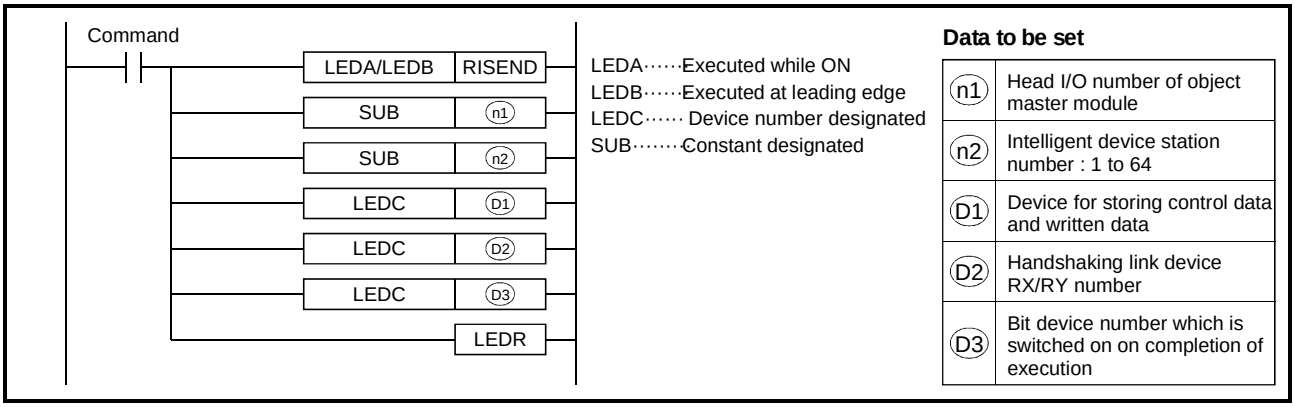
Program Example

The following program reads data from 400H-405H of the buffer memory of the intelligent device station having station number 1 and connected to the master module of CC-Link allocated to I/O numbers 000 to 01F.
The completion status is used for error check.
Also RX2, RY2 and RWr2 are used as handshaking link devices.



1.1.9 Write to intelligent device station buffer memory (with handshake) .....RISEND

	Available device																				Digit designation	Number of steps	Subset	Index	Carry flag	Error flag
	Bit device							Word device									Constant		Pointer		Levle					
	X	Y	M	L	S	B	F	T	C	D	W	R	A0	A1	Z	V	K	H	P	I	N					M9012	M9011
n1																	○	○					29				○
n2																	○	○									
D1								○	○	○	○	○															
D2								○	○	○	○	○															
D3		○	○	○	○	○																					

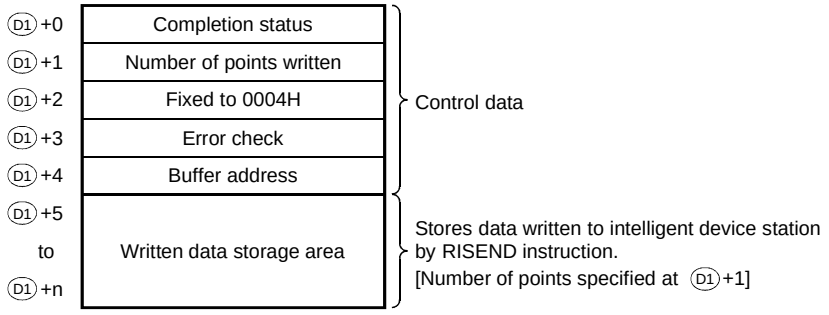


Data to be set

n1	Head I/O number of object master module
n2	Intelligent device station number : 1 to 64
D1	Device for storing control data and written data
D2	Handshaking link device RX/RY number
D3	Bit device number which is switched on on completion of execution

Control Data

(1) Control data setting items



(2) Control data

Item	Set data	Setting range	Setting end
Completion status	Status on completion of instruction execution is stored. 0 : No error Other than 0 : Error code *1	—	System
Number of points written	Specify the number of data written (word basis).	1 to 480 *2	User
Object area	Set "0004H" when accessing the buffer memory of an intelligent device station.	0004H	User
Error check	Specify the error check device. 0 : Completion status is used for error check. Other than 0 : RX+1 is used for error check.	0, 1	User
Buffer memory address	Specify the head address of the buffer memory.	*3	User
Written data storage area	——	—	User

REMARKS

1) *1 : For error codes at error occurrence, refer to the following manual.
Control & Communication-Link System Master · Local Module
type AJ65BT11/A1SJ61BT11 User's Manual

2) *2 : Indicates the maximum number of data written.
Set a value within the intelligent device station buffer memory capacity and parameter-set receiving buffer area setting range.

3) *3 : Refer to the manual of the intelligent device station from which data is read.

Handshaking Link Devices

(1) Handshaking link device setting items

(D2)+0	RX	RY
(D2)+1	RWr	

(2) Setting of handshaking link devices

Item	Set data	Setting range	Setting end
RX	Specify the handshaking RX number of the intelligent device station.	0 to 127	User *2
RY	Specify the handshaking RY number of the intelligent device station.	0 to 127	User *2
RWr	Specify the handshaking RWr number of the intelligent device station.	0 to 15 FF *1	User *2

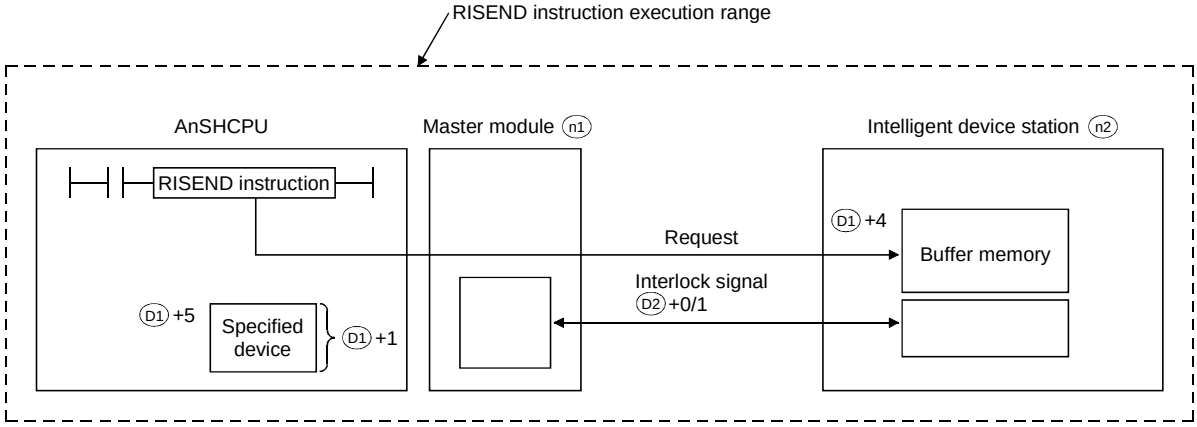
POINTS

(1) *1 : When FFH is set, no number is specified.

(2) *2 : The RX, RY and RW numbers used are set by the user.
Note that RX and RY ON/OFF control and RWr data setting are performed by the system and cannot be changed by the user.
If RX, RY and RW are changed by the user, the RISEND instruction will not be completed properly.

Functions

(1) Writes the points of data specified at (D1)+1 from the devices beginning with the one specified at (D1)+5 to the buffer memory address specified at [(D1)+4] in the intelligent device station having the station number specified at n2 and connected to the master module specified at n1.
On completion of writing, the bit device specified at (D3) switches on only one scan.
On abnormal completion, the bit device at (D2)+1 switches on only one scan.

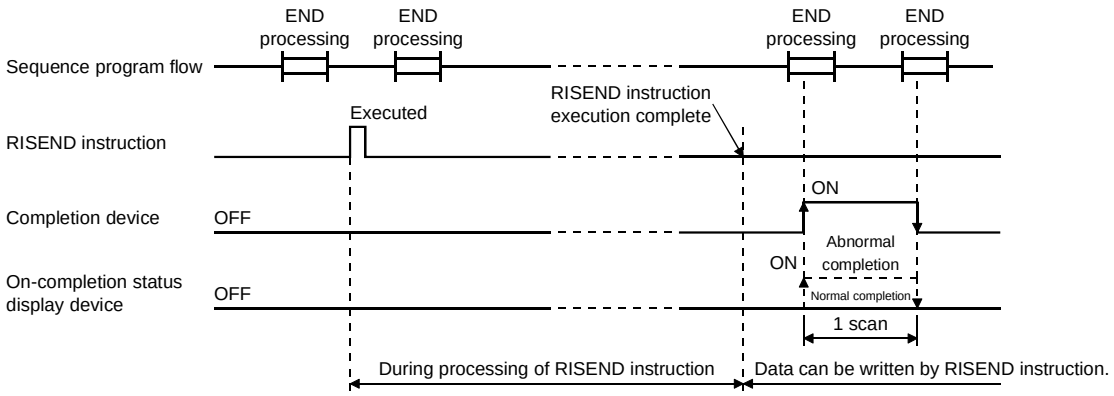


(2) The RISEND instruction may be executed for two or more intelligent device stations at the same time.
However, this instruction cannot be executed for the same intelligent device station in two or more locations at the same time.

(3) Before executing the RISEND instruction, set the network parameters using the RLPA instruction (network parameter setting).
If the RISEND instruction is executed without the network parameters set, abnormal completion will occur and "4B00H" will be stored into the completion status.

(4) No processing will be performed if the number of written points specified at (D1) +1 is "0".

Execution Conditions When the LEDA instruction is used, the RISEND instruction is executed every scan while the write command is ON. When the LEDB instruction is used, the RISEND instruction is executed only one scan on the leading edge (OFF → ON) of the write command.
Note that several scans will be required until the completion of write processing by the RISEND instruction. Therefore, execute the next RISEND instruction after the completion device has switched on.
(The RISEND instruction executed before the completion of RISEND instruction execution is ignored.)



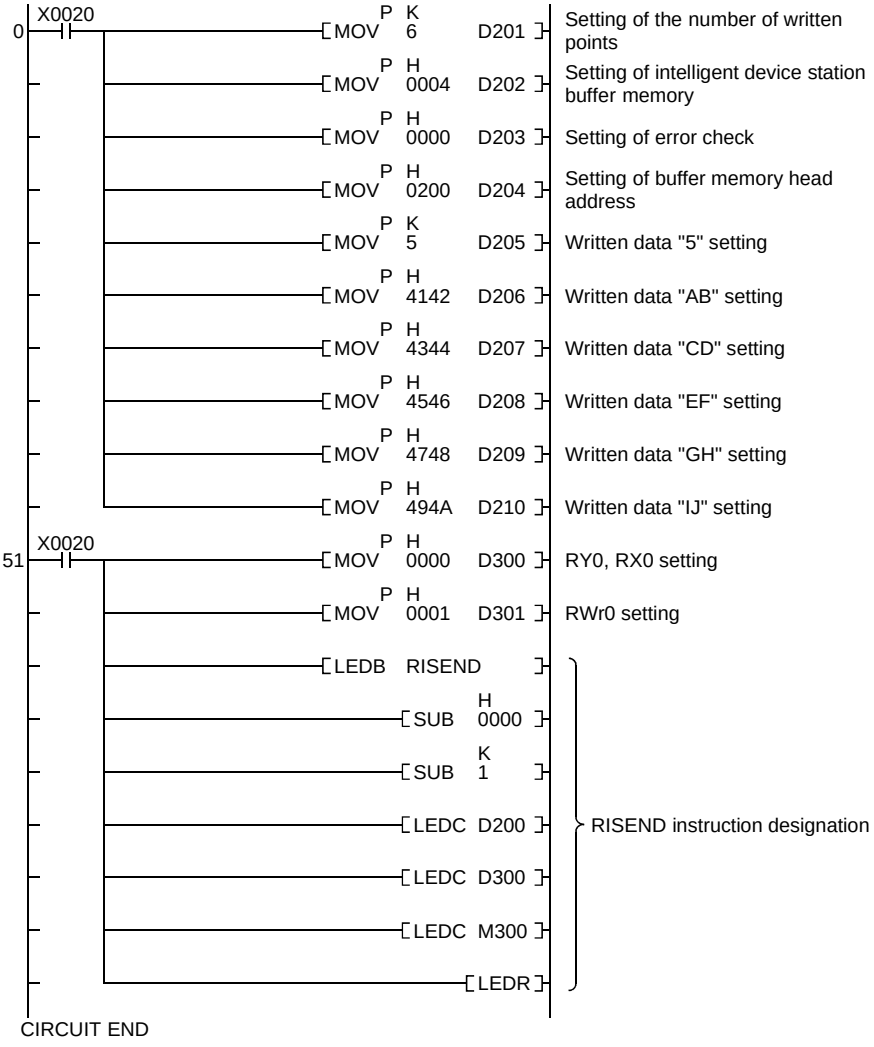
Operation Error

The following condition will result in an operation error and the error flag (M9011) switch on.

Description	Error code	
	D9008	D9092
The number of written points specified at (D1) +1 is outside the range 0 to 480.	50	503

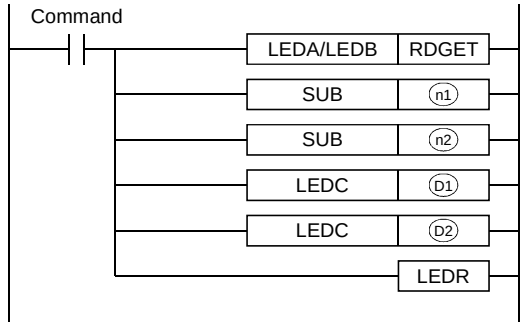
Program Example

The following program writes the number of data written and data "ABCDEFGHIJ" to 200H-205H of the buffer memory of the intelligent device station having station number 1 and connected to the master module of CC-Link allocated to I/O numbers 000 to 01F.
The completion status is used for error check.
Also RX0, RY0 and RWr0 are used as handshaking link devices.



1.1.10 Read from remote device station..... RDGET

	Available device																			Digit designation	Number of steps	Subset	Index	Carry flag	Error flag
	Bit device							Word device									Constant		Pointer		Levle					
	X	Y	M	L	S	B	F	T	C	D	W	R	A0	A1	Z	V	K	H	P	I	N					M9012	M9011
(n1)																	○	○					26				○
(n2)																	○	○									
(D1)								○	○	○	○	○															
(D2)								○	○	○	○	○															



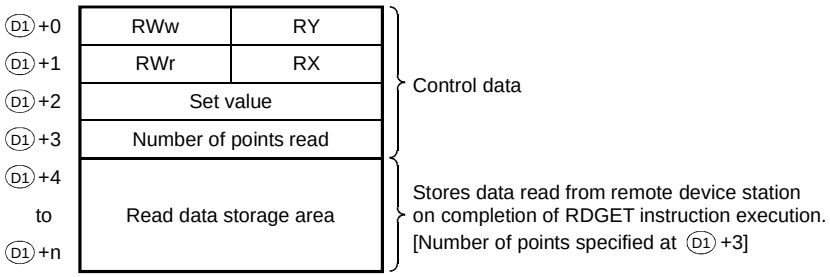
LEDA·····Executed while ON
LEDB·····Executed at leading edge
LEDC····· Device number designated
SUB·····Constant designated

Data to be set

(n1)	Head I/O number of object master module
(n2)	Remote device station number : 1 to 64
(D1)	Device for storing control data and read data
(D2)	Bit device number which is switched on on completion of execution

Control Data

(1) Control data setting items



(2) Number of control data area points
Data read from a remote device station is stored into the area after the 4 points of control data [(D1) +0 to (D1) +3].
Reserve the control data area for 4 points + [number of points specified at (D1) +3] successively.

(3) Control data settings

Item	Set data	Setting range	Setting end
RY	Read request	0 to 127	User *2
RWw	Read request	0 to 15	User *2
RX	Read completion	0 to 127	User *2
RWr	Read completion	0 to 15	User *2
Set value	Specify the reading set value allocated to the remote device station	*1	User
Number of points read	Specify the number of data read (word basis).	1 to 16	User

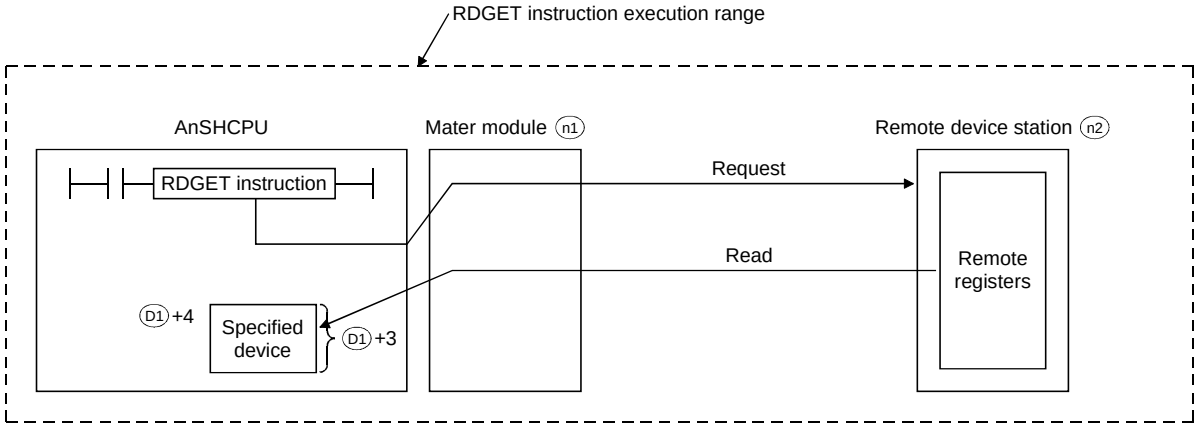
POINTS

(1) *1 : Refer to the manual of the remote device station from which data is read.

(2) *2 : The RY, RWw, RX and RWr numbers used are set by the user.
Note that RY and RX ON/OFF control and RWw and RWr data setting are performed by the system.
The user cannot perform RY and RX ON/OFF control and RWw and RWr data setting.

Functions

(1) Reads the points of data specified at (D1)+3 from the link registers in the remote device station having the station number specified at (n2) and connected to the master module specified at (n1), and stores that data into the devices starting from the one specified at (D1)+4.
On completion of reading, the bit device specified at (D2) switches on only one scan.
On abnormal completion, the bit device at (D2)+1 switches on only one scan.

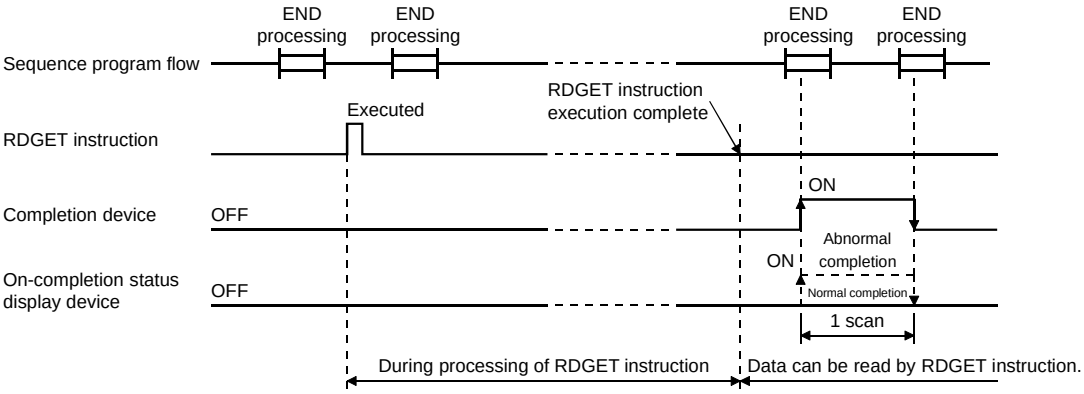


(2) The RDGET instruction may be executed for two or more intelligent device stations at the same time.
However, this instruction cannot be executed for the same intelligent device station in two or more locations at the same time.

(3) As control data, specify the values given in the manual of the remote device station.
If wrong setting is made, the instruction will not be completed.

Execution Conditions

When the LEDA instruction is used, the RDGET instruction is executed every scan while the read command is ON. When the LEDB instruction is used, the RDGET instruction is executed only one scan on the leading edge (OFF → ON) of the read command.
Note that several scans will be required until the completion of read processing by the RDGET instruction. Therefore, execute the next RDGET instruction after the completion device has switched on.
(The RDGET instruction executed before the completion of RDGET instruction execution is ignored.)



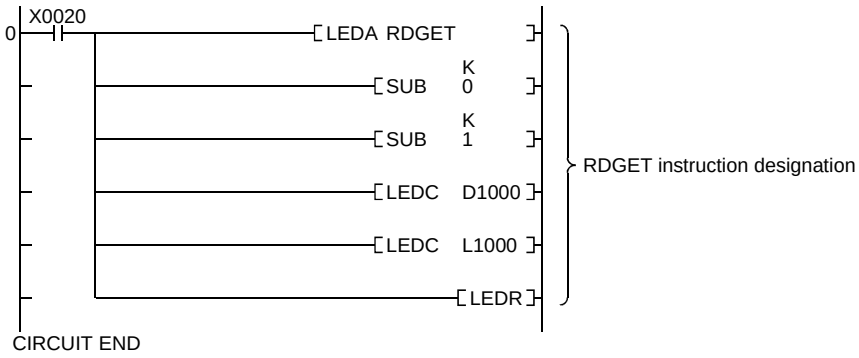
Operation Error

The following condition will result in an operation error and the error flag (M9011) switch on.

Description	Error code	
	D9008	D9092
The number of read points specified at (D1) +3 is outside the range 0 to 480.	50	503

Program Example

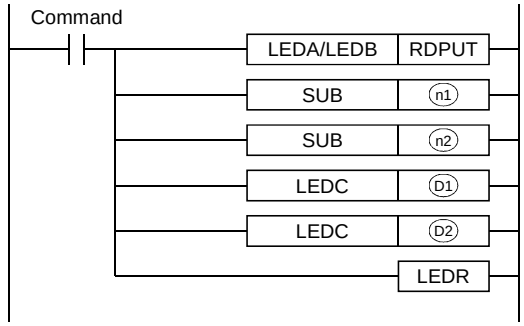
The following program reads 1 point of data from the remote device station having station number 1 and connected to the master module of CC-Link allocated to I/O numbers 000 to 01F.
This program assumes that control data are stored in D1000-D1003.



MEMO

1.1.11 Write to remote device station ..... RDPUT

	Available device																				Digit designation	Number of steps	Subset	Index	Carry flag	Error flag
	Bit device							Word device									Constant		Pointer		Levle						
	X	Y	M	L	S	B	F	T	C	D	W	R	A0	A1	Z	V	K	H	P	I	N					M9012	M9011
n1																	○	○									
n2																	○	○									
D1								○	○	○	○	○										26				○
D2		○	○	○	○	○																				



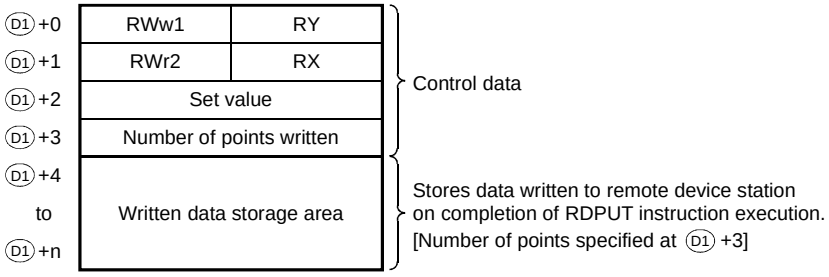
LEDA·····Executed while ON
LEDB·····Executed at leading edge
LEDC····· Device number designated
SUB·····Constant designated

Data to be set

n1	Head I/O number of object master module
n2	Remote device station number : 1 to 64
D1	Device for storing control data and written data
D2	Bit device number which is switched on on completion of execution

Control Data

(1) Control data setting items



(2) Control data settings

Item	Set data	Setting range	Setting end
RY	Write request	0 to 127	User *2
RWw	Write request	0 to 15	User *2
RX	Write completion	0 to 127	User *2
RWr	Write completion	0 to 15	User *2
Set value	Specify the writing set value allocated to the remote device station	*1	User
Number of points written	Specify the number of data written (word basis).	1 to 16	User

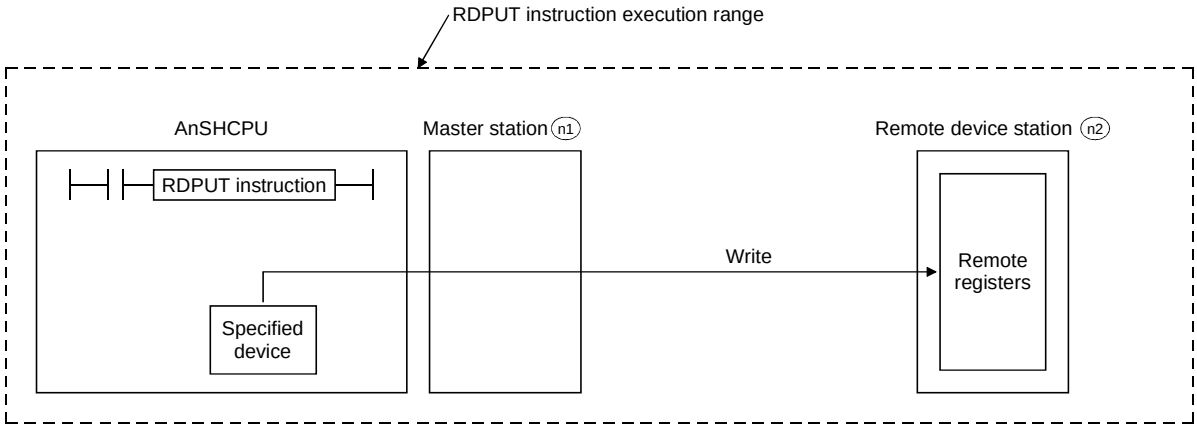
POINTS

(1) *1 : Refer to the manual of the remote device station to which data is written.

(2) *2 : The RY, RWw, RX and RWr numbers used are set by the user.
Note that RY and RX ON/OFF control and RWw and RWr data setting are performed by the system.
The user cannot perform RY and RX ON/OFF control and RWw and RWr data setting.

Functions

(1) Writes the points of data specified at (D1) +3 stored from the devices beginning with the one specified at (D1) +4 using RX and RY specified at (D1) +0-1 to the link registers in the remote device station having the station number specified at (n2) and connected to the master module specified at (n1) .
On completion of writing, the bit device specified at (D2) switches on only one scan.
On abnormal completion, the bit device at (D2) +1 switches on only one scan.

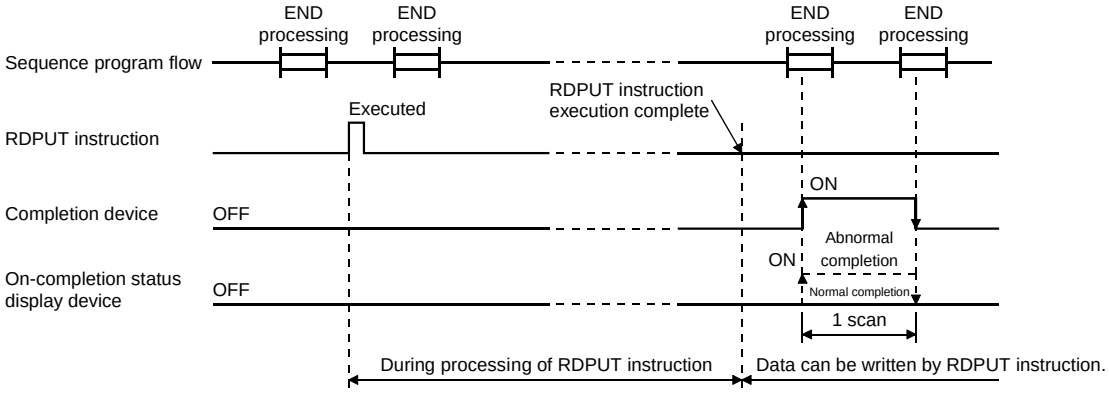


(2) The RDPUT instruction may be executed for two or more remote device stations at the same time.
However, this instruction cannot be executed for the same remote device station in two or more locations at the same time.

(3) As control data, specify the values given in the manual of the remote device station.
If wrong setting is made, the instruction will not be completed.

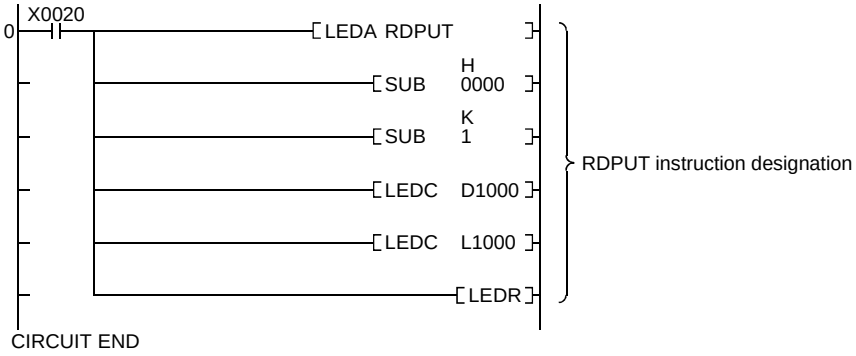
Execution Conditions

When the LEDA instruction is used, the RDPUT instruction is executed every scan while the write command is ON. When the LEDB instruction is used, the RDPUT instruction is executed only one scan on the leading edge (OFF → ON) of the write command.
Note that several scans will be required until the completion of write processing by the RDPUT instruction. Therefore, execute the next RDPUT instruction after the completion device has switched on.
(The RDPUT instruction executed before the completion of RDPUT instruction execution is ignored.)



Program Example

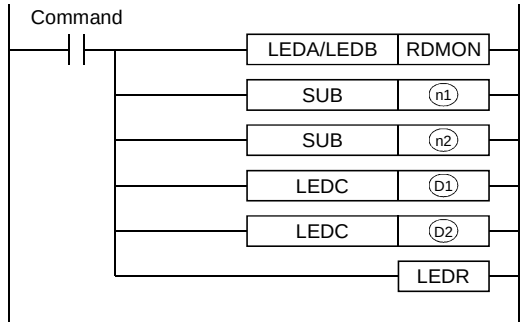
The following program writes 1 point of data to the remote device station having station number 1 and connected to the master module of CC-Link allocated to I/O numbers 000 to 01F.
This program assumes that control data and written data are stored in D1000-D1004.



MEMO

1.1.12 Monitoring of remote device station .....RDMON

	Available device																				Digit designation	Number of steps	Subset	Index	Carry flag	Error flag
	Bit device							Word device									Constant		Pointer		Levle					
	X	Y	M	L	S	B	F	T	C	D	W	R	A0	A1	Z	V	K	H	P	I	N					M9012	M9011
n1																	○	○								
n2																	○	○								
D1								○	○	○	○	○										26				○
D2		○	○	○	○	○																				



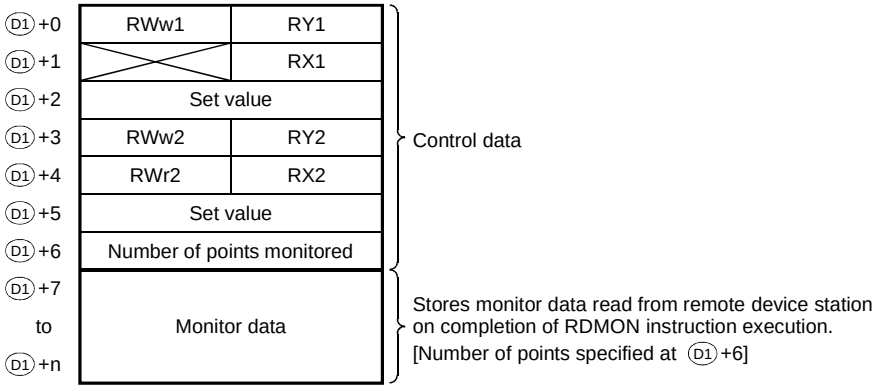
LEDA·····Executed while ON
LEDB·····Executed at leading edge
LEDC····· Device number designated
SUB·····Constant designated

Data to be set

n1	Head I/O number of object master/local module
n2	Remote device station number : 1 to 64
D1	Device for storing control data and read data
D2	Bit device number which is switched on on completion of execution

Control Data

(1) Control data setting items



(2) Number of control data area points

Monitor data read from a remote device station is stored into the area after the 7 points of control data [D1 +0 to D1 +6].
Reserve the control data area for 7 points + [number of points specified at D1 +6] successively.

3) Control data settings

Item	Set data	Setting range	Setting end
RY1	Monitoring registration request	0 to 127 *1	User *2
RWw1	Monitoring registration request	0 to 15 *1	User *2
RX1	Monitoring registration completion	0 to 127 *1	User *2
RY2	Monitoring execution request	0 to 127 *1	User *2
RWw2	Monitoring execution request	0 to 15 *1	User *2
RX2	Monitoring completion	0 to 127 *1	User *2
RWr2	Monitoring completion	0 to 15 *1	User *2
Set value	Specify the monitoring set value allocated to the remote device station.	*1	User
Number of points monitored	Specify the number of data monitored (word basis).	1 to 16	User

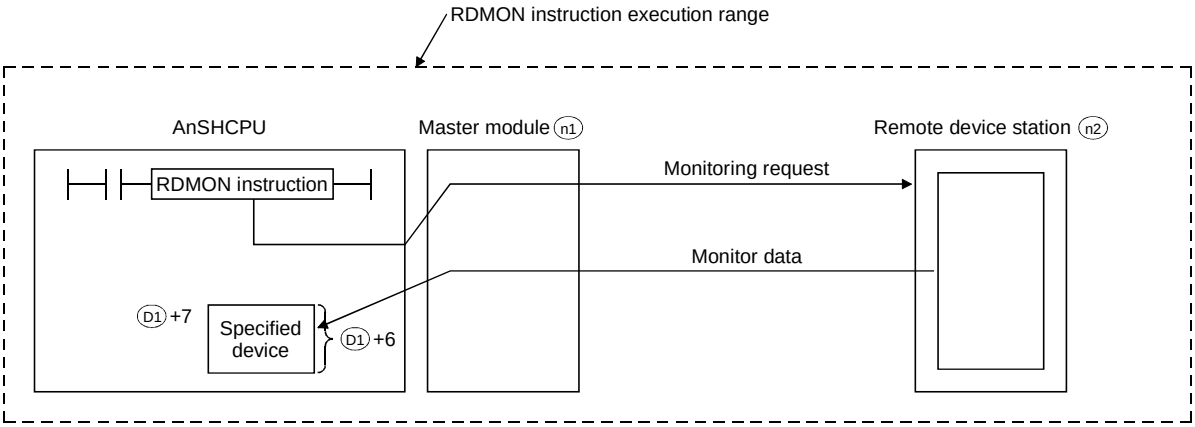
POINTS

(1) *1 : Refer to the manual of the remote device station from which data is monitored.

(2) *2 : The RY1/2, RWw1/2, RX1/2 and RWr2 numbers used are set by the user.
Note that RY1/2 and RX1/2 ON/OFF control and RWw1/2 and RWr2 data setting are performed by the system.
If the user performs RY1/2 and RX1/2 ON/OFF control and RWw1/2 and RWr2 data setting, the RDMON instruction will not be completed properly.

Functions

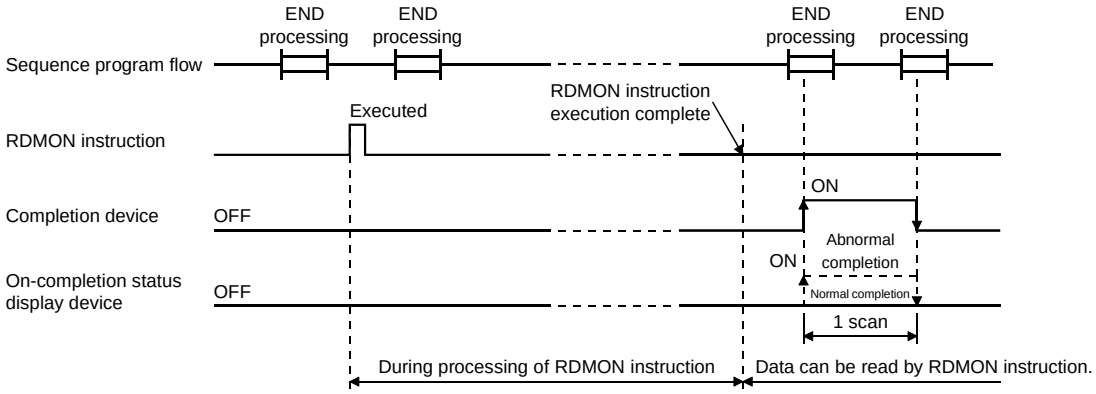
(1) Registers monitoring of the remote device station having the station number specified at (n2) and connected to the master module specified at (n1), and stores the points of monitor data specified at (D1)+6 into the devices starting from the one specified at (D1)+7.
On completion of monitor data reading, the bit device specified at (D2) switches on only one scan.
On abnormal completion, the bit device at (D2)+1 switches on only one scan.



(2) The RDMON instruction may be executed for two or more remote device stations at the same time.
However, this instruction cannot be executed for the same remote device station in two or more locations at the same time.

Execution Conditions

When the LEDA instruction is used, the RDMON instruction is executed every scan while the read command is ON. When the LEDB instruction is used, the RDMON instruction is executed only one scan on the leading edge (OFF → ON) of the read command.
Note that several scans will be required until the completion of read processing by the RDMON instruction. Therefore, execute the next RDMON instruction after the completion device has switched on.
(The RDMON instruction executed before the completion of RDMON instruction execution is ignored.)



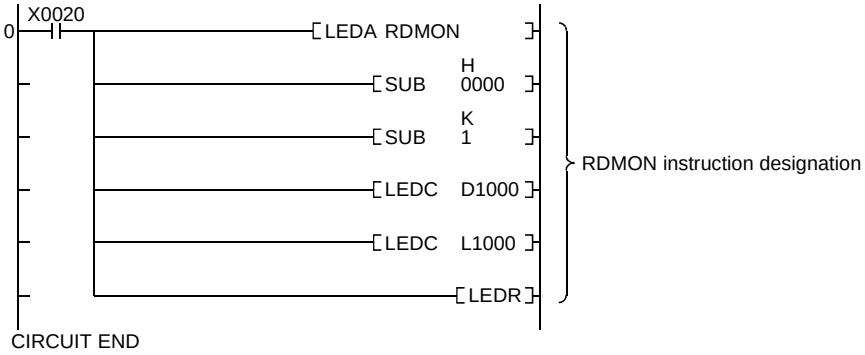
Operation Error

The following condition will result in an operation error and the error flag (M9011) switches on.

Description	Error code	
	D9008	D9092
The number of read points specified at (D1) +3 is outside the range 0 to 480.	50	503

Program Example

The following program monitors 1 point from the remote device station having station number 1 and connected to the master module of CC-Link allocated to I/O numbers 000 to 01F.
This program assumes that control data are stored in D1000-D1006.



Appendix 1.2 Caution when Performing a Write while Running Dedicated Instruction

Description of write performed when running.	For LEDA	For LEDB
Normal configuration is written when running.	After write, the previous contact turns on and the instruction is executed.	After write, the instruction is executed when the previous contact is turned from OFF to ON.
LEDA/LEDB was added by mistake.	Error 104 occurs (incorrect configuration).	If the previous contact stays after write, the instruction is not executed, so no process is performed. When the previous contact is turned from OFF to ON, error 104 results.
LEDA/LEDB was deleted by mistake.	The LEDC/SUB/LEDR is processed as a regular instruction.	Same as stated on left.
LEDC/SUB was added by mistake.	Error 104 occurs (incorrect configuration).	If the previous contact stays after write, the instruction is not executed, so no process is performed. When the previous contact is turned from OFF to ON, error 104 results.
LEDC/SUB was deleted by mistake.	Error 104 occurs (incorrect configuration).	If the previous contact stays after write, the instruction is not executed, so no process is performed. When the previous contact is turned from OFF to ON, error 104 results.
LEDR was added by mistake.	The latter LEDR is processed as a regular instruction.	The latter LEDR is processed as a regular instruction.
LEDR was deleted by mistake.	Error 104 occurs if LEDR does not exist directly after the deleted LEDR.	Error 104 occurs if LEDR does not exist directly after the deleted LEDR. If LEDR exists, all instructions in between are not executed.

Appendix 2 Special Relay, Special Register List

Appendix 2.1 Special Relay List

(1) Special relay list

Special relays are internal relays whose uses are determined inside the PC. Therefore, they cannot be turned ON/OFF as coils is a program. (Except for *1 and *2 in the table)

Table 2.1 Special relay list

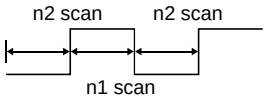
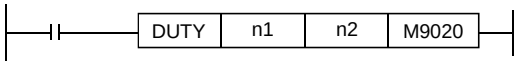
Number	Name	Description	Details
*1 M9000	Fuse blown	OFF : Normal ON : Presence of fuse blow module	• Turned on when there is one or more output modules whose fuse has blown. Remains on if normal status is restored.
*1 M9002	I/O module verify error	OFF : Normal ON : Error	• Turned on if the status of I/O module is different from entered status when power is turned on. Remains on if normal status is restored.
*1 M9005	AC DOWN detection	OFF : AC is good ON : AC is down	• Turned on if power interruption no longer than 20msec occurs. Reset when POWER switch is moved from OFF to ON position.
M9006	Battery low	OFF : Normal ON : Battery low	• Turned on when battery voltage falls to less than specified voltage. Turned off when battery voltage becomes normal.
*1 M9007	Battery low latch	OFF : Normal ON : Battery low	• Turned on when battery voltage falls to less than specified voltage. Remains on if battery voltage becomes normal.
*1 M9008	Self-diagnostic error	OFF : Normal ON : Error	• Turned on when error is found as a result of self-diagnosis.
M9009	Annunciator detection	OFF : Normal ON : Error	• Turned on when OUT F or SET F instruction is executed. Switched off when D9124 value is set to 0.
M9010	Operation error flag	OFF : Normal ON : Error	• Turned on when an operation error occurs during execution of an application instruction. Turned off when the error is eliminated.
*1 M9011	Operation error flag	OFF : Normal ON : Error	• Turned on when an operation error occurs during execution of an application instruction. Remains on when normal status is restored.
M9012	Carry flag	OFF : Carry off ON : Carry on	• Carry flag used in application instruction.
M9016	Data memory clear flag	OFF : No processing ON : Output clear	• Clears all data memory (except special relays and special registers) in remote run mode from a computer, for example, when M9016 is 1.
M9017	Data memory clear flag	OFF : No processing ON : Output clear	• Clears all unlatched data memory (except special relays and special registers) in remote run mode from a computer, for example, when M9017 is 1.
M9020 M9021 M9022 M9023 M9024	User timing clock No.0 User timing clock No.1 User timing clock No.2 User timing clock No.3 User timing clock No.4		• Relay which repeats on/off at intervals of the predetermined scan. • When the power is turned on or reset is performed, the clock starts with off. • Set the intervals of on/off [DUTY] instruction. 
*2 M9025	Clock data set request	OFF : No processing ON : Data set request	• Writes clock data from D9025-D9028 to the clock devices after the END instruction is executed in the scan in which M9025 is switched on.

Table 2.1 Special Relay List (Continued)

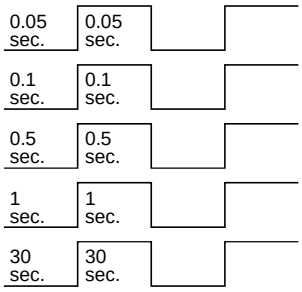
Number	Name	Description	Details
M9026	Clock data error	OFF : Normal ON : Error	• Switched on when a clock data (D9025 to D9028) error occurs.
*2 M9028	Clock data read request	OFF : No processing ON : Read request	• Reads clock data in BCD to D9025-D9028 when M9028 is switched on.
M9030	0.1 second clock		• 0.1 second, 0.2 second, 1 second, 2 second, and 1 minute clocks are generated. • Not turned on and off in synchrony with the scan cycle but even during a scan if the corresponding time has elapsed. • Starts when power is turned on or reset is performed.
M9031	0.2 second clock		
M9032	1 second clock		
M9033	2 second clock		
M9034	1 minute clock		
M9036	Normally ON	ON OFF	• Used as dummy contacts for initialization and application instructions in sequence program. • M9036 and M9037 are switched on/off independently of the CPU RUN/STOP switch position. M9038 and M9039 are switched on/off in accordance with the RUN/STOP switch position, i.e. switched off when the switch is set to STOP. When the switch is set to a position other than STOP, M9038 is only switched on during 1 scan and M9039 is only switched off during 1 scan.
M9037	Normally OFF	ON OFF	
M9038	On only for 1 scan after run	ON OFF 1 scan	
M9039	RUN flag (off only for 1 scan after run)	ON OFF 1 scan	
M9040	PAUSE enable coil	OFF : PAUSE disabled ON : PAUSE enabled	• When RUN key switch is at PAUSE position or remote pause contact has turned on and if M9040 is on, PAUSE mode is set and M9041 is turned on.
M9041	PAUSE status contact	OFF : During pause ON : Not during pause	
M9042	Stop status contact	OFF : During stop ON : Not during stop	• Switched on when the RUN/STOP switch is set to STOP.
M9043	Sampling trace completion	OFF : During sampling trace ON : Sampling trace completion	• Turned on upon completion of sampling trace performed the number of times preset by parameter after STRA instruction is executed. Reset when STRAR instruction is executed.
M9046	Sampling trace	OFF : Except during trace ON : During trace	• On during sampling trace.
M9047	Sampling trace preparation	OFF : Sampling trace stop ON : Sampling trace start	• Sampling trace is not executed until M9047 is turned on. By turning off M9047, sampling trace is stopped.
M9049	Number of characters output switching	OFF : Characters up to NULL code output ON : 16 characters output	• When M9049 is off, characters up to NULL (00H) code are output. • When M9049 is on, ASCII codes for 16 characters are output.
*2 M9052	SEG instruction switching	OFF : 7SEG display ON : I/O partial refresh	• Serves as an I/O partial refresh instruction when M9052 is on. • Serves as a 7SEG display instruction when M9052 is off.
*2 M9053	EI/DI instruction switching	OFF : Sequence interrupt control ON : Link interrupt control	• Switch on to execute the link refresh enable, disable (EI, DI) instructions.
M9054	STEP RUN flag	OFF : Not during step run ON : During step run	• Switched on when the RUN/STOP switch is in the STEP RUN position.
M9055	Status latch completion flag	OFF : Uncompleted ON : Completed	• Turned on when status latch is completed. Turned off by reset instruction.

Table 2.1 Special relay list (Continued)

Number	Name	Description	Details
*2 M9084	Error check setting	OFF : Error checked ON : Error unchecked	• Used to set whether or not the following error checks are made on execution of the END instruction. (To shorten the END instruction processing time.) • Fuse blown, I/O module verify error, battery error

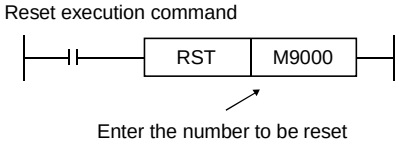
POINTS

(1) All special relays are switched off by the power-off, latch clear and reset operations. The special relays remain unchanged when the RUN/STOP switch is set to STOP.

(2) The above relays with numbers marked *1 remain "on" if normal status is restored. To turn them "off", use the following method:

1) Method using a user program

Insert the circuit shown at right into the program and turn on the reset execution command contact to clear the special relay M.



2) Method using a peripheral device.

Cause forced reset by the test function of peripheral equipment. For the operating procedure, refer to the manual for each peripheral device.

3) By moving the RESET key switch at the CPU front to the RESET position, the special relay is turned "off".

(3) Special relays marked *2 are switched on/off in the sequence program.

Appendix 2.2 Special Registers D

The special registers are data registers used for specific purposes. Therefore, do not write data to the special registers in the program (except the ones with numbers marked *2 in the table).

Table 2.2 Special registers list

Number	Name	Stored data	Explanation
D9000	Fuse blown	Number of module with blown fuse	• When modules with blown fuses are detected, the lowest module number among the detected modules is stored in hexadecimal. (Example : When the fuses of Y50 to 6F output modules have blown, "50" is stored in hexadecimal) The module number monitored by the peripheral is hexadecimal. (Cleared when all contents of D9100 are reset to 0.)
D9002	I/O module verify error	I/O module verify error module number	• If I/O modules whose data is different from data entered are detected when the power is turned on, the first I/O number of the lowest module number among the detected modules is stored in hexadecimal. (Storing method is the same as that of D9000.) The module number monitored by the peripheral is hexadecimal. (Cleared when all contents of D9116 of D9123 are reset to 0.)
*1 D9005	AC DOWN counter	AC DOWN time count	• 1 is added each time the input voltage becomes 80 % or less of the rating while the CPU module is performing an operation, and the value is stored in BIN code.
*1 D9008	Self-diagnostic error	Self-diagnostic error number	• When error is found as a result of self-diagnosis, the error number is stored in BIN code.
D9009	Annunciator detection	F number at which external failure has occurred	• When one of F0 to F255 is turned on by [OUT F] or [SET F], the F number, detected earliest among the F numbers which have turned on is stored in BIN code. • D9009 can be cleared by the [RST F] or [LEDR] instruction. If another F number has been detected, the clearing of D9009 causes the next number to be stored in D9009.
D9010	Error step	Step number at which operation error has occurred	• When an operation error has occurred during execution of an application instruction, the step number at which the error has occurred is stored in BIN code. Thereafter, each time an operation error occurs, the contents of D9010 are renewed.
D9011	Error step	Step number at which operation error has occurred	• When an operation error has occurred during execution of an application instruction, the step number at which the error has occurred is stored in BIN code. Since storage into D9011 is executed when M9011 changes from off to on, the contents of D9010 cannot be renewed unless M9011 is cleared by the user program.
D9014	I/O control mode	I/O control mode number	• The set mode is represented as follows : 0 = I/O in direct mode 3 = I/O in refresh mode

Table 2.2 Special registers list

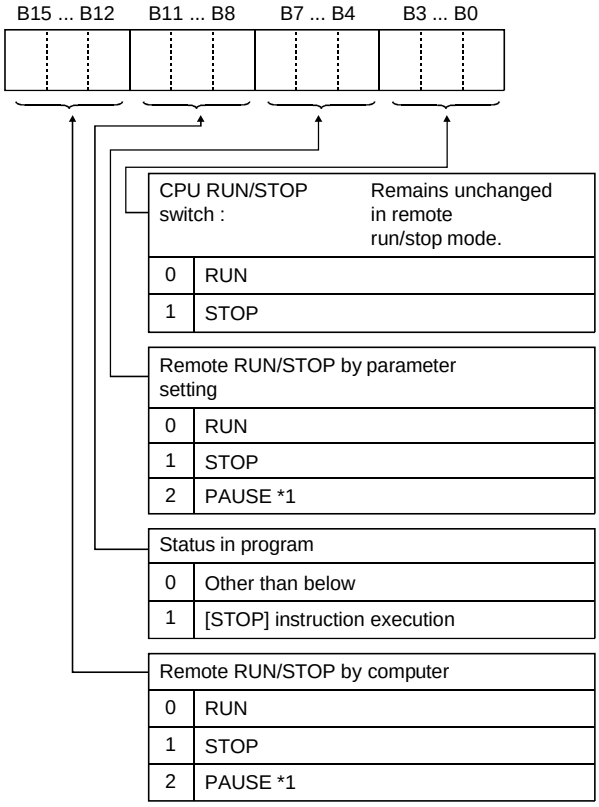
Number	Name	Stored data	Explanation
D9015	CPU operating states	Operating states of CPU	The operating states of CPU as shown below are stored in D9015.  *1 When the CPU is in RUN mode and M9040 is off, the CPU remains in RUN mode if changed to PAUSE mode.
D9016	ROM/RAM setting	0 : ROM 1 : RAM 2 : E.MDSU/2.MDNM/P ROM	• Indicates the setting of memory select chip. One value among 0 to 2 is stored in BIN code.
D9017	Scan time	Minimum scan time (per 10msec)	• If the scan time is shorter than the contents of D9017, the value is newly stored at each END. Namely, the minimum value for scan time is stored in D9017 in BIN code.
D9018	Scan time	Scan time (per 10msec)	• The scan time is stored in BIN code at each END and always rewritten.
D9019	Scan time	Maximum scan time (per 10msec)	• If the scan time is longer than the contents of D9019, the value is newly stored at each END. This means that the maximum value of the scan time is stored in D9019 in BIN code.

Table 2.2 Special registers list (Continued)

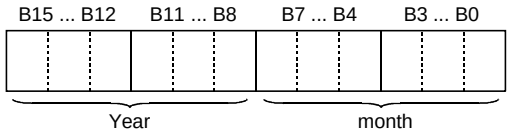
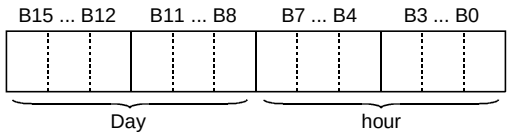
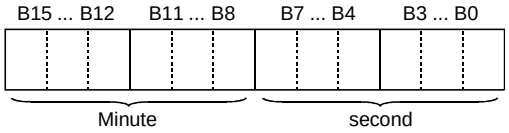
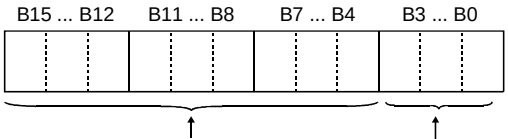
Number	Name	Stored data	Explanation
*2 D9020	Constant scan	Constant scan time (User specified in 10msec increments)	• Sets user program execution intervals in 10msec increments. 0 : Constant scan function not used 1 to 200 : Constant scan function used,, program executed at intervals of (set value) 10msec.
*2 D9025	Clock data	Clock data (Year, month)	• Stores the year (least significant digits) and month in BCD.  Example : 1987, July H8707
*2 D9026	Clock data	Clock data (Day, hour)	• Stores the day and hour in BCD.  Example : 31st, 10 O,clock, H3110
*2 D9027	Clock data	Clock data (Minute, second)	• Stores the minute and second in BCD.  Example : 35 minutes, 48 seconds, H3548
*2 D9028	Clock data	Clock data (0, day of the week)	• Stores the day of the week in BCD.  Day of the week 0 Sunday 1 Monday 2 Tuesday 3 Wednesday 4 Thursday 5 Friday 6 Saturday

Table 2.2 Special registers list (Continued)

<table>
<tr><th>Number</th><th>Name</th><th>Stored data</th><th>Explanation</th></tr>
<tr><td>*2 D9038

*2 D9039</td><td>LED display priority</td><td>Priority 1 to 4

Priority 5 to 7</td><td>• Set the error item numbers in the ERROR LED display (flashing) priority setting registers (1 to 4 at D9038 and 5 to 7 at D9039).
<table><tr><td>B15 ... B12</td><td>B11 ... B8</td><td>B7 ... B4</td><td>B3 ... B0</td></tr><tr><td>—</td><td>—</td><td>—</td><td>5</td></tr></table>
<table><tr><td>B15 ... B12</td><td>B11 ... B8</td><td>B7 ... B4</td><td>B3 ... B0</td></tr><tr><td>4</td><td>3</td><td>2</td><td>1</td></tr></table>
• Even when "0" is set, the ERROR LED display is given for those errors which stop CPU operation (parameter setting errors are also included).

Default :
D9038 = H4321
D9039 = H0006
Priority
<table><tr><th>Error item No.</th><th>Content</th></tr>
<tr><td>0.</td><td>No display is given.</td></tr>
<tr><td>1.</td><td>I/O verify and fuse break errors</td></tr>
<tr><td>2.</td><td>Special function module, link parameterk, SFC parameter, and SFC operation errors</td></tr>
<tr><td>3.</td><td>CHK instruction error</td></tr>
<tr><td>4.</td><td>Annunciator (F)</td></tr>
<tr><td>6.</td><td>Battery error</td></tr></table></td></tr>
<tr><td>*1 D9100
D9101</td><td>Fuse blown module</td><td>Bit pattern in units of 16 points, indicating the modules whose fuses have blown.</td><td>• The numbers of output modules whose fuses have blown or whose external power supply is OFF are input as a bit pattern (in modules of 16 points). (If the module numbers are set by parameter, the output is in the form of the parameter-set numbers.)
<table><tr><th></th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>D9100</td><td>0</td><td>0</td><td>0</td><td>1 YC0</td><td>0</td><td>0</td><td>0</td><td>1 Y80</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>D9101</td><td>1 Y1F0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1 Y1A0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>
Indicates "fuse blown"

(The pattern is not cleared even if the module recovers. Therefore, it must be cleared using a program.)</td></tr>
<tr><td>*1 D9116
D9117</td><td>Input/Output module verification error</td><td>Bit pattern in units of 16 points, indicating the modules with verification errors.</td><td>• The module numbers of the I/O modules whose information differs from the I/O module information registered when the power was turned ON are set (in modules of 16 points). (If the I/O module numbers are set by parameter, the output is in the form of the parameter-set numbers.)
<table><tr><th></th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>D9116</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1 X/Y 0</td></tr>
<tr><td>D9117</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1 X/Y 190</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>
Indicates "I/O module verification error"

(The pattern is not cleared even if the module recovers. Therefore, it must be cleared using a program.)</td></tr>
</table>

Table 2.2 Special registers list (Continued)

Number	Name	Stored data	Explanation
D9124	Anunciator detection quantity	Annunciator detection quantity	• When one of F0 to 255 is turned on by [OUT F] or [SET F], 1 is added to the contents of D9124. When the [RST F] or [LED R] instruction is executed, 1 is subtracted from the contents of D9124. The quantity which has been turned on by [OUT F] or [SET F] is stored into D9124 in BIN code. The maximum value of D9124 is 8.
D9125 D9126 D9127 D9128 D9129 D9130 D9131 D9132	Annunciator detection number	Annunciator detection number	• When one of F0 to 255 is turned on by [OUT F] or [SET F], the F number which has turned on is entered into D9125 to D9132 in due order in BIN code. The F number which has been turned off by [RST F] is erased from D9125 to D9132, and the contents of data registers succeeding the data register, where the erased F number was stored, are shifted to the preceding data registers. When the [LED R] instruction is executed, the contents of D9125 to D9132 are shifted upward by one. When there are 8 annunciator detections, a 9th one is not stored in D9125 to 9132 even if detected.

	SET F50	SET F25	SET F19	SET F25	SET F15	SET F70	SET F65	SET F38	SET F110	SET F151	SET F210	LED R
D9009	0	50	50	50	50	50	50	50	50	50	50	99
D9124	0	1	2	3	2	3	4	5	6	7	8	8
D9125	0	50	50	50	50	50	50	50	50	50	50	99
D9126	0	0	25	25	99	99	99	99	99	99	99	15
D9127	0	0	0	99	0	15	15	15	15	15	15	70
D9128	0	0	0	0	0	0	70	70	70	70	70	65
D9129	0	0	0	0	0	0	0	65	65	65	65	38
D9130	0	0	0	0	0	0	0	0	38	38	38	110
D9131	0	0	0	0	0	0	0	0	0	110	110	151
D9132	0	0	0	0	0	0	0	0	0	0	151	210

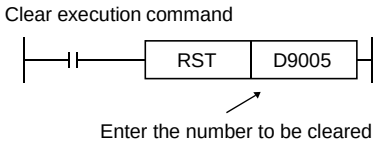
POINTS

(1) All special register data is cleared by the power-off, latch clear and reset operations. The data is retained when the RUN/STOP switch is set to STOP.

(2) For the above special registers with numbers marked *1, the contents of the register are not cleared if the normal status is restored. To clear the contents, use the following method:

1) Method using a user program.

Insert the circuit shown at right into the program and turn on the clear execution command contact to clear the contents of the register.



2) Method using peripheral equipment.

Set the register to "0" by changing the present value using the test function of a peripheral device or set it to "0" using forced reset. For the operation procedure, refer to the manual for each peripheral device.

3) By moving the RESET key switch at the CPU front to the RESET position, the special register is set to "0".

(3) Data is written to the special registers marked *2 by the sequence program.

Appendix 3 Precautions when Switching from AnSCPU to AnSHCPU

Appendix 3.1 Dissimilarities between A1SHCPU and A1SCPU

The dissimilarities between the A1SHCPU and A1SCPU are as follows :

	Item	A1SHCPU	A1SCPU
1	CPU processing speed *1	0.33 μs	1 μs
2	I/O points	2048 points *2	256 points
3	File register capacity (R)	Max. 8192 points (R0 to 8191)	Max. 4096 points (R0 to 4095)
4	Memory capacity	64 k bytes	32 k bytes
5	Comment points	Max. 3648 points	Max. 1600 points *3
6	CC-Link dedicated instruction	11	None
7	Startup model	A3	A1S
8	Memory write protect range	First half, 32 k bytes	First half, 20 k bytes
9	Microcomputer program	There are some restrictions.	There is no restrictions.
10	Conventional memory cassette A1SMCA-2KE/8KE/8KP	×	ϒ
	New-type memory cassette A1SMCA-2KE/8KE/8KP	ϒ	ϒ
11	Clock precision	Year, month, day, hour, minute, day of week (Automatic leap year calculation)	
		Precision -3.1 to +5.3 s(TYP. +1.7 s)/d at 0 °C -1.6 to +5.3 s(TYP. +2.4 s)/d at 25 °C -9.6 to +3.6 s(TYP. -2.1 s)/d at 55 °C	Precision -2.3 to +4.4 s(TYP. +1.8 s)/d at 0 °C -1.1 to +4.4 s(TYP. +2.2 s)/d at 25 °C -9.6 to +2.7 s(TYP. -2.4 s)/d at 55 °C

*1 : I/O processing: during refresh and LD instruction execution

*2 : Actual I/O points are the same as the AnS series, but this model has 2048 points of I/O device for each CPU (X/Y0 to 7FF). The added I/O device can be used for MELSECNET (/B), MELSECNET/MINI, or CC-Link.

*3 : The comment points for comments that can be stored in the CPU is 1600 points, while up to 3648 points of comment can be created using the GPP function.

Appendix 3.2 Dissimilarities between A2SHCPU(-S1) and A2SCPU

The dissimilarities between the A2SHCPU(-S1) and A2SCPU are as follows :

	Item	A2SHCPU(-S1)	A2SCPU
1	CPU processing speed *1	0.25 μs	1 μs
2	I/O points	2048 points *2	512 points
3	File register capacity (R)	Max. 8192 points (R0 to 8191)	Max. 4096 points (R0 to 4095)
4	CC-Link dedicated instruction	11	None
5	Startup model	A3	A2
6	Microcomputer program	There are some restrictions.	There is no restrictions.
7	Conventional memory cassette A2SMCA-14KE/14KP	×	ϒ
	New-type memory cassette A2SNMCA-30KE	ϒ	ϒ
8	Clock precision	Year, month, day, hour, minute, day of week (Automatic leap year calculation)	
		Precision -3.1 to +5.3 s(TYP. +1.7 s)/d at 0 °C -1.6 to +5.3 s(TYP. +2.4 s)/d at 25 °C -9.6 to +3.6 s(TYP. -2.1 s)/d at 55 °C	Precision -2.3 to +4.4 s(TYP. +1.8 s)/d at 0 °C -1.1 to +4.4 s(TYP. +2.2 s)/d at 25 °C -9.6 to +2.7 s(TYP. -2.4 s)/d at 55 °C

*1 : I/O processing : during refresh and LD instruction execution

*2 : Actual I/O points are the same as the AnS series, but this model has 2048 points of I/O device for each CPU (X/Y0 to 7FF). The added I/O device can be used for MELSECNET (/B), MELSECNET/MINI, or CC-Link.

Appendix 3.3 Precautions when Switching the Model

Appendix 3.3.1 PC type setting

The PC type becomes "A3" to enable the use of 2048 input device points X/Y, file register R8192 points and LEAD/LEDB instructions.

Appendix 3.3.2 The precaution when performing the ROM cutoff

When performing the ROM cutoff of A1SJHCPU and A1SHCPU with SW4GP-GPPA, the startup model must be changed as following.

	Startup model
Before software version Q	A0J2H
Aafter software version R	A1S

Appendix 3.3.3 The precaution when utilizing the sequence program

In case of utilizing the sequence program, the parameter must be set again as the parameter goes back to the initial setting when performing the change of the PC type.

Appendix 3.3.4 System comfirmation by high-speed instruction processing

Comfirm effects on the user system by the instruction processing speed and the reduction of the scan time.

Appendix 3.3.5 Handling conventional memory cassettes

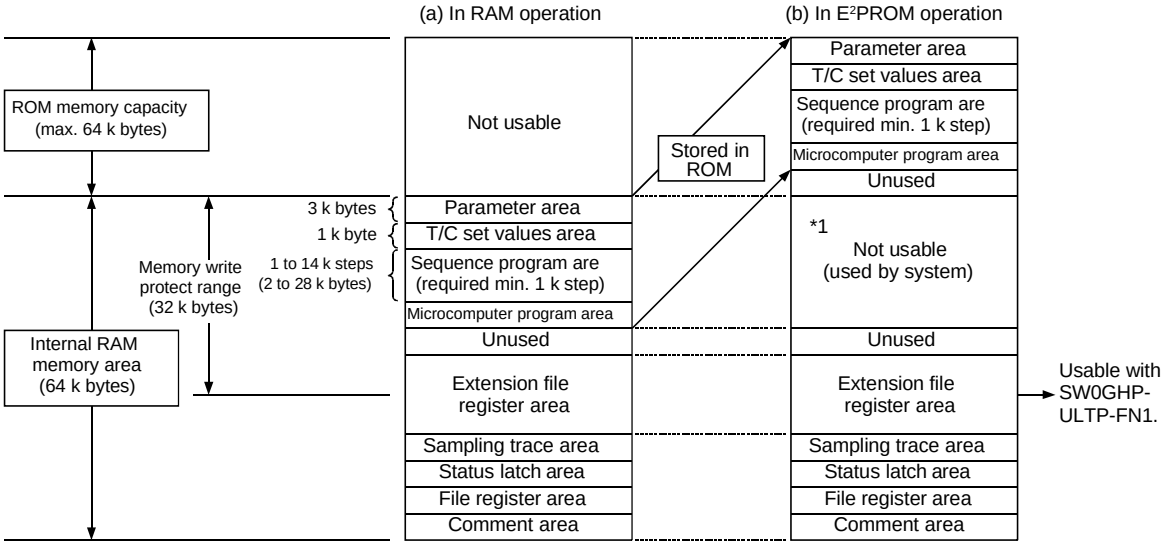
Conventional memory cassettes A1SMCA-2KE/8KE/8KP (for A1SCPU) and A2SMCA-14KE (for A2SCPU) cannot be used for A1SHCPU and A2SHCPU. (Used only for A1SJHCPU)

The new type memory cassettes A1SNMCA-2KE/8KE/8KP (for A1SJHCPU/A1SHCPU) and A2SNMCA-3KE (for A2SHCPU) should be used.

Appendix 3.3.6 Switching from the A2SMCA-14KP (when A2SCPU + A2SMCA-14KP has been used)

When A2SHCPU + A2SNMCA-30KE was switched, *1 area cannot be used as the extension file register.

When *1 area has been used as the extension file register, the system of A2USCPU(-S1) + A2SMCA-14KP should be used.



Appendix 3.3.7 Restrictions in microcomputer programs

When a customer used the microcomputer mode, the following changes are made in the microcomputer instructions.

Change points by switching to AnSHCPU from AnSCPU	Corrective action method
When REP LODSW and REP LODSB instructions are used AnSCPUThe ..... contents of a memory shown by the S1 register for the number of times specified in CX register,, are transfered to the register of AL (8 bits operation) or AX (16 bits operation). Aafter the instructions have been executed, the CX register value becomes 0. AnSHCPU ..... The contents of a memory shown only once by the S1 register regardless of the value of the CX register,, are transfered to the register of AL (8 bits operation) or AX (16 bits operation). After the instructions have been executed, the CX register value does not change.	The following example for the program should be revered. Program example STD MOV CX.3 **REP LODSB** → **A : LODSB Loop A** STD MOV CX.3

Appendix 4 CE Marking Compatible Module for Compact PC

Function		Specification
CPU module	A1SHCPU	See the performance specification in Section 4.4.1. Number of I/O points : 256,, memory capacity : 64 k bytes
	A1SJHCPU	See the performance specification in Section 4.4.1. Number of I/O points: 256,, memory capacity : 64 k bytes
	A2SHCPU	See the performance specification in Section 4.4.1. Number of I/O points : 512,, memory capacity : 64 k bytes
	A2SHCPU-S1	See the performance specification in Section 4.4.1. Number of I/O points : 1024,, memory capacity : 192 k bytes
Power supply module	A1S61PEU	200 to 240 V AC input, 5 V DC 5 A output
	A1S62PEU	200 to 240 V AC input,, 5 V DC 3 A 24 V DC 0.6 A output
	A1S61PN	100 to 240 V AC input,, 5 V DC 5 A output
	A1S62PN	100 to 240 V AC input,, 5 V DC 3 A 24 V DC 0.6 A output
Input module	A1SX10EU	16 points,, 100 to 120 V AC input
	A1SX20EU	16 points,, 200 to 240 V AC input
Output module	A1SY10EU	16 points, 120 V AC output (relay)
	A1SY14EU	16 points, 240 V AC output (relay)
	A1SY18AEU	8 points, 240 V AC output,, independent common (relay)
	A1SY28EU	8 points, 100 to 240 V AC output (triac)

Appendix 5 Instruction Processing Time

Instruction	Condition (device)					processing time (μs)			
						A1SHCPU		A2SHCPU	
						Refresh method	Direct method	Refresh method	Direct method
LD LDI AND	X					0.33	2.1	0.25	1.9
ANI OR ORI	Y, M, L, S, B, F, T, C					0.33	0.33	0.25	0.25
ANB	—								
ORB	—					0.33	0.33	0.25	0.25
OUT	Y		When not changed (OFF→OFF, ON→ON)			0.33	2.2	0.25	1.9
			When changed (OFF→OFF, ON→ON)			0.33	2.2	0.25	1.9
	M (excluding special M L, S, B)		When not changed (OFF→OFF, ON→ON)			0.33	0.33	0.25	0.25
			When changed (OFF→OFF, ON→ON)			0.33	0.33	0.25	0.25
	Special M					9.6	9.5	7.2	7.2
	F	Not in execution				16.5	16.7	12.3	12.3
		During execution				69.5	84.4	52.2	52.2
	T	Instruction execution time				0.33	0.33	0.25	0.25
		Processing time at END	Non-execution time			0	0	0	0
			During execution	After time is up		7.2	9.6	20.0	18.0
				When counting	K	12.0	12.8	22.0	22.0
					D	21.6	24.0	24.0	23.6
	C	Instruction execution time				0.33	0.33	0.25	0.25
		Processing time at END	Non-execution time			0	0	0	0
			During execution	When not counted		0	0	0	0
				After count is up		0	0	0	0
				When counting	K	0.8	0.8	12.0	12.8
					D	7.2	10.4	15.2	12.0

Instruction	Condition (device)			processing time (μs)					
				A1SHCPU		A2SHCPU			
				Refresh method	Direct method	Refresh method		Direct method	
SET	Y	Not in execution		0.33	2.1	0.25		1.9	
		During execution	When not changed (ON→ON)	0.33	2.1	0.25		1.9	
			When changed (OFF→ON)	0.33	2.1	0.25		1.9	
	M, L S, B	Not in execution		0.33	0.33	0.25		0.25	
		During execution	When not changed (ON→ON)	0.33	0.33	0.25		0.25	
			When changed (OFF→ON)	0.33	0.33	0.25		0.25	
	Special M B	Not in execution		0.9	1.0	1.0		1.0	
		During execution		7.9	8.3	6.2		6.2	
	F	Not in execution		0.9	1.4	1.0		1.0	
		During execution		62.0	61.5	46.1		46.1	
RST	Y	Not in execution		0.33	0.33	0.32		1.9	
		During execution	When not changed (OFF→OFF)	0.33	2.0	0.32		1.9	
			When changed (ON→OFF)	0.33	2.0	0.32		1.9	
	M, L S, B	Not in execution		0.33	0.33	0.32		0.25	
		During execution	When not changed (OFF→OFF)	0.33	0.33	0.32		0.25	
			When changed (ON→OFF)	0.33	0.33	0.32		0.25	
	Special M B	Not in execution		1.4	1.4	1.0		1.0	
		During execution		8.4	8.4	6.2		6.2	
	F	Not in execution		1.4	1.4	1.0		1.0	
		During execution		73.2	75.3	OFF →OFF 8.5	ON →OFF 57.1	OFF →OFF 8.4	ON →OFF 57.1
	T,C	Not in execution		1.4	1.4	1.0		1.0	
		During execution		11.0	11.0	OFF →OFF 8.3	ON →OFF 9.0	OFF →OFF 8.3	ON →OFF 9.0
	D, W A0, A1 V, Z	Not in execution		1.4	1.4	1.0		1.0	
		During execution		7.0	7.0	5.2		5.3	
	R	Not in execution		1.4	1.6	1.0		1.0	
		During execution		36.4	36.2	6.7		6.7	
NOP	—			0.33	0.33	0.25		0.25	

Instruction	Condition (device)			processing time (μs)					
				A1SHCPU		A2SHCPU			
				Refresh method	Direct method	Refresh method		Direct method	
FEND	M9084 OFF			663.2	628.0	Y0 ON 466.6	OFF 432.6	Y0 ON 451.7	OFF 412.3
END	M9084 ON			636.0	602.4	Y0 ON 451.3	OFF 415.3	Y0 ON 436.1	OFF 403.9
MC	Y	Not n execution		15.0	13.0	8.8		10.5	
		During execution		14.0	11.9	8.0		9.7	
	M, L, S B, F	Not in execution		13.4	11.4	8.8		8.5	
		During execution		12.2	10.3	8.0		7.7	
MCR	—			5.4	7.3	5.2		6.8	
PLS PLF	Y	Not in execution		16.8	16.8	11.7		13.7	
		During execution	When ON	17.2	17.2	11.6		13.7	
			When OFF	17.2	17.2	11.7		13.7	
	M, L B, F	Not in execution		15.2	15.2	11.7		11.7	
		During execution	When ON	15.6	15.6	11.6		11.6	
			When OFF	15.6	15.6	11.7		11.6	
SFT SFTP	Y	Not in execution		1.4	1.4	1.0		1.0	
		During execution		12.4	12.4	8.1		10.1	
	M, L B, F	Not in execution		1.4	1.4	1.0		1.0	
		During execution		10.8	10.8	8.1		8.1	
MPS	—			0.33	0.33	0.25		0.25	
MRD	—			0.33	0.33	0.25		0.25	
MPP	—			0.33	0.33	0.25		0.25	
CJ	No index modification			10.2	10.2	7.6		10.0	
	Index modification			12.6	12.6	9.5		11.9	
SCJ	No index modification			17.8	17.7	13.3		13.3	
	Index modification			20.2	20.5	15.1		15.1	
JMP				10.2	10.3	7.6		7.6	
CALL	No index modification			17.8	17.9	13.3		13.3	
	Index modification			20.2	20.3	15.1		15.1	
CALLP	No index modification			17.8	17.9	13.2		13.2	
	Index modification			20.2	20.3	15.1		15.1	
RET				10.4	10.3	9.3		9.6	
EI				9.6	9.2	7.1		7.1	
DI				6.8	7.0	6.5		6.5	
IRET				58.4	57.6	43.2		45.1	

Instruction	Condition (device)	processing time (μs)			
		A1SHCPU		A2SHCPU	
		Refresh method	Direct method	Refresh method	Direct method
SUB	No index modification	39.8	17.6	19.0	13.0
	Index modification	41.4	19.2	20.0	15.0
SUBP	No index modification	39.8	17.6	19.0	13.0
	Index modification	41.4	19.2	20.0	15.0
FOR		11.4	11.6	10.1	10.1
NEXT		8.0	8.1	7.5	8.2

Instruction	Condition	S		D		Processing time (μs)			
						A1SHCPU		A2SHCPU	
		(S1)	(S2)	(D1)	(D2)	Refresh method	Direct method	Refresh method	Direct method
LD=		D0		D1		19.2	19.6	14.7	14.6
AND=		D0		D1		17.0	17.0	12.9	12.8
OR=		D1		D0		18.0	18.2	13.7	13.6
LDD=		D0		D2		36.4	37.1	27.5	27.5
ANDD=		D0		D2		33.6	34.3	25.3	25.5
ORD=		D0		D2		36.2	36.9	27.3	27.5
LD<>		D0		D1		19.4	19.2	14.5	14.5
AND<		D0		D1		16.2	16.2	12.3	12.3
OR<>		D0		D1		17.4	17.6	13.1	13.0
LD<=		D0		D1		19.8	19.6	14.9	14.7
AND<		D0		D1		17.9	16.7	12.3	12.3
OR<=		D0		D1		18.6	18.9	13.9	13.9
LDD<=		D0		D2		37.8	37.8	28.5	28.3
ANDD<=		D0		D2		34.8	34.8	26.3	26.1
ORD<=		D0		D2		37.4	37.6	28.3	28.1
LD<		D0		D1		19.4	19.4	14.7	14.5
AND<		D0		D1		16.6	16.4	12.5	12.3
OR<		D0		D1		17.2	17.2	13.1	13.0
LDD<>		D0		D2		35.6	35.6	26.9	26.7
ANDD<>		D0		D2		35.2	35.4	26.7	26.7
ORD<>		D0		D2		34.4	34.6	25.9	25.9
LD>		D0		D1		18.8	19.0	14.3	14.3
AND>		D0		D1		17.0	17.4	12.7	12.9
OR>		D0		D1		17.2	17.6	12.9	12.9
LDD>		D0		D2		36.4	36.2	27.5	27.3
ANDD>		D0		D2		38.5	36.4	27.1	27.1
ORD>		D0		D2		35.2	35.2	26.5	26.5
LDD<		D0		D2		36.2	36.6	27.3	27.5
ANDD<		D0		D2		36.0	36.4	27.1	27.1
ORD<		D0		D2		35.4	35.4	26.5	26.4
LD>=		D0		D1		19.6	19.6	14.9	14.8
AND>		D0		D1		16.6	16.8	12.5	12.4
OR>=		D0		D1		18.6	19.0	14.1	13.8
LDD>=		D0		D2		37.8	38.0	28.3	28.2

Instruction	Condition	S		D		Processing time (μs)			
						A1SHCPU		A2SHCPU	
		(S1)	(S2)	(D1)	(D2)	Refresh method	Direct method	Refresh method	Direct method
ANDD>=		D0		D2		35.0	35.0	26.1	26.1
ORD>=		D0		D2		37.6	37.8	28.3	28.0
+		D0		D1		11.6	11.9	8.7	8.6
+P		D0		D1		11.4	12.1	8.6	8.6
D+		D0		D2		18.2	18.5	13.7	13.6
D+P		D0		D2		18.0	18.3	13.6	13.2
+		D0	D1	D2		20.2	20.7	15.3	15.2
+P		D0	D1	D2		20.2	20.5	15.2	14.8
D+		D0	D1	D4		25.6	25.9	19.3	19.2
D+P		D0	D1	D4		25.8	26.3	19.4	19.2
-		D0		D1		11.6	12.1	8.7	8.6
-P		D0		D1		11.8	12.1	8.6	8.6
D-		D0		D2		18.0	18.5	13.7	13.6
D-P		D0		D2		18.0	18.7	13.6	13.2
-		D0	D1	D2		20.8	21.3	15.7	15.6
-P		D0	D2	D2		20.8	21.3	15.8	15.6
D-		D0	D2	D4		27.0	25.7	20.3	20.4
D-P		D0	D2	D4		26.8	27.3	20.4	20.2
*		D0	D1	D2		22.0	22.7	16.5	16.4
*P		D0	D1	D2		21.8	22.7	16.6	16.6
D*		D0	D2	D4		98.2	98.3	73.7	73.6
D*P		D0	D2	D4		98.2	98.5	73.6	73.8
/		D0	K1	D2		23.2	23.9	17.7	17.4
/P		D0	K1	D2		23.2	23.9	17.4	17.4
D/		D0	K1	D4		106.8	107.5	80.1	80.2
D/P		D0	K1	D4		106.6	107.3	80.2	80.2
INC				D0		7.2	7.5	5.7	5.4
INCP				D1		7.4	7.7	5.4	5.4
DINC				D0		10.6	11.3	8.1	8.0
DINCP				D0		10.6	11.1	7.9	7.8
DEC				D0		7.8	8.5	6.1	5.8
DECP				D0		7.8	8.3	5.9	5.8
DDEC				D0		10.6	11.1	8.1	8.0
DDECP				D0		2.7	1.9	8.1	7.8

Instruction	Condition	S		D		Processing time (μs)			
						A1SHCPU		A2SHCPU	
		(S1)	(S2)	(D1)	(D2)	Refresh method	Direct method	Refresh method	Direct method
B+		D0		D1		33.6	34.1	25.3	25.2
B+P		D1		D1		34.0	34.3	25.2	25.0
DB+		D0		D2		47.0	47.5	35.2	35.2
DB+P		D0		D2		46.8	47.7	35.4	35.0
B+		D0	D1	D2		35.2	35.7	26.5	26.4
B+P		D0	D1	D2		35.2	35.5	26.6	26.2
DB+		D0	D2	D4		50.2	50.9	37.7	37.8
DB+P		D0	D2	D4		50.2	50.5	37.5	37.8
B-		D0		D1		33.2	33.7	24.9	24.8
B-P		D0		D1		33.0	33.7	24.9	24.6
DB-		D0		D2		46.8	47.3	35.3	35.0
DB-P		D0		D2		46.8	47.3	35.1	35.0
B-		D0	D1	D2		36.2	36.9	27.3	27.0
B-P		D0	D1	D2		36.2	36.7	27.1	27.0
DB-		D0	D2	D4		50.4	50.6	38.1	37.8
DB-P		D0	D2	D4		50.4	51.1	37.9	37.4
B*		D0	D1	D2		79.8	80.1	60.1	59.4
B*P		D0	D1	D2		80.0	80.1	59.7	59.8
DB*		D0	D2	D4		245.6	246.3	184.3	184.2
DB*P		D0	D2	D4		246.8	246.1	184.3	184.2
B/		D0	K1	D1		61.4	61.7	46.2	46.6
B/P		D0	K1	D2		61.2	61.7	46.1	46.6
DB/		D0	K1	D2		246.4	246.9	185.1	184.8
DB/P		D0	K1	D4		246.0	186.5	184.5	184.8
BCD		D0		D1		22.0	22.3	16.3	16.5
BCDP		D0		D1		22.0	22.5	16.7	16.6
DBCD		D0		D2		59.2	59.7	44.3	44.4
DBCDP		D0		D2		59.2	59.7	44.5	44.8
BIN		D0		D1		20.8	21.5	15.7	16.0
BINP		D0		D1		20.8	21.3	15.7	15.8
DBIN		D0		D2		58.2	58.9	43.9	43.8
DBINP		D0		D2		58.2	58.9	43.7	43.8
MOV		D0		D2		11.8	12.3	9.1	9.0
MOVP		D0		D2		11.8	12.5	8.9	9.0

Instruction	Condition	S		D		Processing time (μs)			
						A1SHCPU		A2SHCPU	
		(S1)	(S2)	(D1)	(D2)	Refresh method	Direct method	Refresh method	Direct method
DMOV		D0		D2		17.2	17.7	13.1	13.0
DMOVP		D0		D2		17.2	17.9	13.1	13.0
XCH				D0	D1	15.8	16.3	11.9	11.8
XCHP				D0	D1	15.8	16.3	11.9	11.8
DXCH				D0	D2	28.8	29.5	21.7	21.6
DXCHP				D0	D2	28.8	29.1	21.7	21.8
CML		D0		D1		10.8	11.5	8.3	8.4
CMLP		D0		D1		10.8	11.5	8.3	8.2
DCML		D0		D2		20.2	20.9	15.1	15.2
DCMLP		D0		D2		20.2	20.7	15.3	15.0
BMOV		D0		D1	K5	59.2	59.5	44.4	44.4
BMOVP		D0		D1	K5	59.1	59.5	44.5	44.3
FMOV		D0		D1	K5	33.8	34.5	25.4	25.4
FMOVP		D0		D1	K5	33.8	34.3	25.5	25.4
WAND Ⓢ Ⓓ		D0		C0		15.4	15.7	11.5	11.4
WANDP Ⓢ Ⓓ		D0		C0		15.4	15.7	11.5	11.6
DAND Ⓢ Ⓓ		D0		C0		36.2	36.5	27.1	27.2
DANDP Ⓢ Ⓓ		D0		C0		36.2	36.5	27.1	27.2
WAND Ⓢ1 Ⓢ2 Ⓓ		C0	D0	D100		25.8	26.1	19.3	19.2
WANDP Ⓢ1 Ⓢ2 Ⓓ		C0	D0	D100		25.8	26.1	19.3	19.2
WOR Ⓢ Ⓓ		C0		D0		15.0	15.5	11.1	11.2
WORP Ⓢ Ⓓ		C0		D0		15.0	15.5	11.1	11.2
DOR Ⓢ Ⓓ		C0		D0		36.4	36.7	27.3	27.2
DORP Ⓢ Ⓓ		C0		D0		36.4	36.9	27.3	27.2
WOR Ⓢ1 Ⓢ2 Ⓓ		C0	D0	D100		25.8	26.1	19.3	19.2
WORP Ⓢ1 Ⓢ2 Ⓓ		C0	D0	D100		25.8	26.3	19.3	19.2
WXOR Ⓢ Ⓓ		C0		D0		15.4	15.5	11.5	11.4
WXORP Ⓢ Ⓓ		C0		D0		15.4	15.5	11.5	11.6
DXOR Ⓢ Ⓓ		C0		D0		36.2	36.7	27.1	27.2
DXORP Ⓢ Ⓓ		C0		D0		36.4	36.5	27.3	27.2
WXOR Ⓢ1 Ⓢ2 Ⓓ		C0	D0	D10		25.6	25.9	19.3	19.2
WXORP Ⓢ1 Ⓢ2 Ⓓ		C0	D0	D10		25.6	26.1	19.3	19.2
WXNR Ⓢ Ⓓ		C0		D0		15.6	16.1	11.7	11.6
WXNRP Ⓢ Ⓓ		C0		D0		15.6	15.9	11.7	11.8

Instruction	Condition	S		D		Processing time (μs)			
						A1SHCPU		A2SHCPU	
		(S1)	(S2)	(D1)	(D2)	Refresh method	Direct method	Refresh method	Direct method
DXNR Ⓢ Ⓓ		C0		D0		36.6	37.1	27.5	27.4
DXNRP Ⓢ Ⓓ		C0		D0		36.6	36.9	27.5	27.6
WXNR Ⓢ1 Ⓢ2 Ⓓ		C0	D0	D10		25.6	26.1	19.3	19.4
WXNRP Ⓢ1 Ⓢ2 Ⓓ		C0	D0	D10		26.0	26.3	19.5	19.4
NEG Ⓓ				D0		12.6	13.1	9.5	9.5
NEGP Ⓓ				D0		12.6	13.3	9.5	9.5
ROR n	n=3					12.6	13.1	9.5	9.5
RORP n	n=3					12.6	12.9	9.5	9.5
RCR n	n=3					14.6	15.1	10.9	11.1
RCRP n	n=3					14.6	14.9	10.9	11.0
ROL n	n=3					13.2	13.7	9.9	10.0
ROLP n	n=3					13.4	13.7	9.9	10.1
RCL n	n=3					15.2	15.7	11.3	11.4
RCLP n	n=3					15.2	15.5	11.5	11.4
DROR n	n=3					18.4	18.7	13.7	13.7
DRORP n	n=3					18.4	18.7	13.7	13.7
DRCR n	n=3					18.0	18.3	13.5	13.5
DRCRP n	n=3					18.0	18.5	13.5	13.4
DROL n	n=3					18.4	18.7	13.7	13.8
DROLP n	n=3					18.2	18.9	13.1	13.7
DRCL n	n=3					18.8	19.1	14.1	14.1
DRCLP n	n=3					18.8	18.9	14.1	14.0
SFR Ⓓ n	n=5			D0		18.4	17.5	13.7	13.8
SFRP Ⓓ n	n=5			D0		18.4	18.9	13.7	13.8
BSFR Ⓓ n	n=5			M0		31.6	31.7	23.7	23.8
BSFR Ⓓ n	n=15			M0		33.6	33.9	25.1	25.2
BSFRP Ⓓ n	n=5			M0		31.6	31.9	23.5	23.5
BSFRP Ⓓ n	n=15			M0		33.6	33.9	25.3	25.0
DSFR Ⓓ n	n=5			C0		30.2	30.5	22.5	22.6
DSFRP Ⓓ n	n=5			C0		30.2	30.5	22.7	22.8
SFL Ⓓ n	n=5			C0		19.2	19.5	14.3	14.4
SFLP Ⓓ n	n=5			C0		19.2	19.7	14.3	14.6
BSFL Ⓓ n	n=5			M64		34.4	34.7	25.7	25.8
BSFL Ⓓ n	n=15			M64		36.0	36.5	26.9	27.2

Instruction	Condition	S		D		Processing time (μs)			
						A1SHCPU		A2SHCPU	
		(S1)	(S2)	(D1)	(D2)	Refresh method	Direct method	Refresh method	Direct method
BSFLP Ⓓ n	n=5			M64		34.4	34.9	25.9	25.8
BSFLP Ⓓ n				M64		36.0	36.5	27.1	27.0
DSFL Ⓓ n	n=5			C0		30.4	30.9	22.7	22.8
DSFLP Ⓓ n	n=5			C0		30.4	30.9	22.9	22.8
BSET Ⓓ n	n=5			C0		23.6	24.1	17.5	18.0
BRST Ⓓ n	n=5			D0		25.0	25.5	18.7	18.8
BRSTP Ⓓ n	n=5			D0		25.0	25.5	18.7	18.8
SEG Ⓢ Ⓓ								19.8	19.7
UNI Ⓢ Ⓓ n	n=1	C0		D0		28.8	29.1	21.5	21.6
UNIP Ⓢ Ⓓ n	n=1	C0		D0		28.8	29.1	21.5	21.6
DIS Ⓢ Ⓓ n	n=1	C0		D0		37.6	38.1	28.1	28.4
DISP Ⓢ Ⓓ n	n=1	C0		D0		37.6	37.9	28.1	28.4
FIFW Ⓢ Ⓓ		D0		C0		69.0	69.3	55.3	55.2
FIFWP Ⓢ Ⓓ		C0		D0		27.2	43.3	20.5	20.4
FIFR Ⓓ1 Ⓓ2				C0	D0	53.8	54.3	40.3	40.3
FIFRP Ⓓ1 Ⓓ2				C0	D0	82.2	54.3	40.3	40.2
SER Ⓢ1 Ⓢ2 n	n=5	D0	C0			49.8	50.1	37.3	37.2
SERP Ⓢ1 Ⓢ2 n	n=5	D0	C0			49.8	50.3	37.5	37.4
SUM Ⓢ		D0				30.8	31.1	23.1	23.2
SUMP Ⓢ		D0				30.8	31.3	23.3	23.2
DSUM Ⓢ		D0				53.8	54.3	40.3	40.4
DSUMP Ⓢ		D0				53.8	54.3	40.5	40.4
DECO Ⓢ Ⓓ n	n=2	C0		D0		43.2	43.7	32.3	32.4
DECOP Ⓢ Ⓓ n	n=2	C0		D0		43.2	43.9	32.5	32.4
ENCO Ⓢ Ⓓ n	n=2	C0		D0		92.6	93.1	69.5	69.4
ENCOP Ⓢ Ⓓ n	n=2	C0		D0		92.6	93.1	69.4	69.4
BSET Ⓓ n	n=5			C0		23.6	23.9	17.7	18.0
ASC						30.7	30.7	23.1	23.0
ASC	Z					34.8	34.9	26.3	26.1
LRDP	n=1					48.4	48.3	36.4	36.6
LRDP	n=32					48.4	48.3	36.4	36.6
LWTP	n=1					51.2	51.2	38.8	38.6
LWTP	n=32					115.2	115.6	86.6	86.6
RFRP	n=1					43.4	53.2	32.8	45.0

Instruction	Condition	S		D		Processing time (μs)			
						A1SHCPU		A2SHCPU	
		(S1)	(S2)	(D1)	(D2)	Refresh method	Direct method	Refresh method	Direct method
RFRP	n=16					43.4	53.4	32.8	45.0
RTOP	n=1					44.0	54.0	33.4	45.4
RTOP	n=16					44.4	54.0	33.6	45.6
WDT						16.2	16.3	12.2	12.2
WDTP						16.2	16.3	12.2	12.2
CHK	1 contact						97.0		77.0
CHK	50 contacts						118.2		92.8
CHK	100 contacts						140.0		109.0
CHK	150 contacts						160.8		125.4
SLT	Device memory only					1088.5	1561.5	878.7	1381.3
SLT	Device memory + R					3314.5	3787.5	2480.7	3035.3
SLTR						7.6	7.7	5.8	5.8
STRA						7.5	7.5	5.7	5.6
STRAR						7.1	7.2	5.4	5.4
STC						7.1	7.2	5.4	5.4
CLC						7.4	7.5	5.7	5.6
DUTY						17.3	17.4	13.1	13.0
PR						68.7	70.4	52.5	54.4
PRC						41.9	41.9	31.5	31.4
CHK	Bit invert					30.7		23.2	
LEDR						75.9	75.9	56.9	57.0
FROM	n=1					150.6	146.9	131.7	130.4
FROM	n=1000					3880.5	3873.5	4576.7	4579.3
FROMP	n=1					150.7	146.9	131.8	130.4
FROMP	n=1000					3926.5	3873.5	4624.7	4635.3
DFRO	n=1					161.9	158.3	141.8	140.6
DFRO	n=500					3888.5	3897.5	4584.7	4582.3
DFROP	n=1					161.9	158.3	141.8	140.6
DFROP	n=500					4012.5	3887.5	4632.7	4582.3
TO	n=1					152.4	151.1	135.0	133.6
TO	n=1000					3882.5	3881.5	4568.7	4579.3
TOP	n=1					152.4	151.3	135.0	133.6
TOP	n=1000					3946.5	3881.5	4688.7	4635.3

Instruction	Condition	S		D		Processing time (μs)			
						A1SHCPU		A2SHCPU	
		(S1)	(S2)	(D1)	(D2)	Refresh method	Direct method	Refresh method	Direct method
DTO	n=1					157.2	155.9	138.2	138.8
DTO	n=500					3882.5	3881.5	4584.7	4582.3
DTOP	n=1					157.2	155.9	138.2	138.8
DTOP	n=500					3930.5	3881.5	4688.7	4582.3
RRPA						275.2	292.5	206.0	220.2
RLPA						308.1	324.0	240.9	255.6
RIFR						340.5	348.2	284.1	293.5
RITO						349.0	356.7	290.6	299.8
RIRD						198.9	201.6	148.7	152.9
RIWT						192.8	195.5	144.1	148.3
RISEND						230.7	231.8	172.7	174.6
RIRCV						230.9	232.0	172.8	174.8
RDGET						202.5	205.2	151.4	155.6
RDPUT						204.3	207.1	152.8	156.9
RDMON						196.9	199.7	147.2	151.4

* The instruction processing time is measures while performing the subset processing.

Subset processing processes basic and applied instructions speedily with the following conditions when a bit device is specified.

- Conditions of subset processing
  Subset processing is possible when one of the following is satisfied without using the index modification.

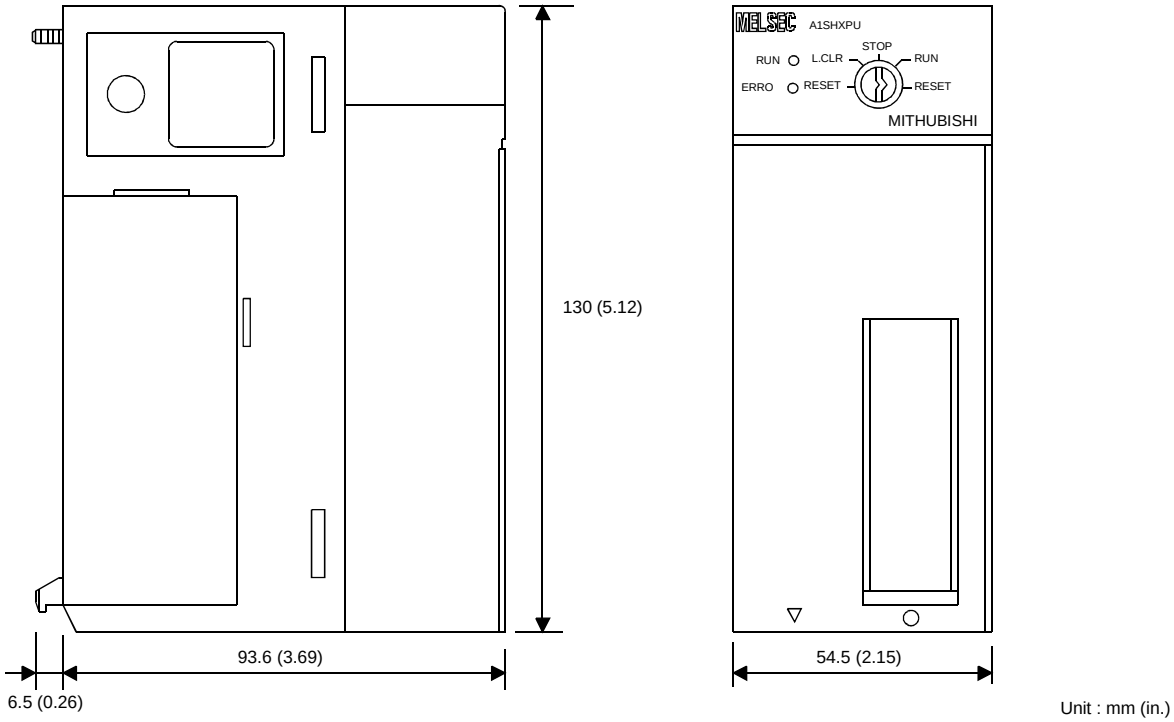
  (1) Bit device digit specification is K4 (for 16-bit processing) or K8 (for 32-bit processing).

  (2) The device No. is a multiple of 8.

Appendix 6 Outside Dimensions

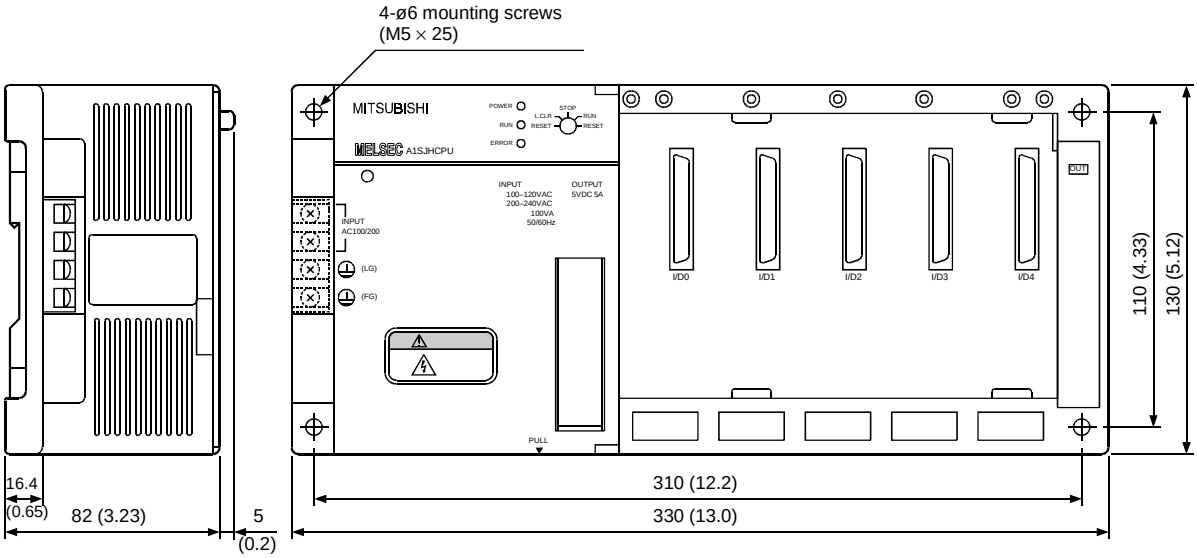
Appendix 6.1 CPU Module

Appendix 6.1.1 A1SHCPU/A2SHCPU(S1) module



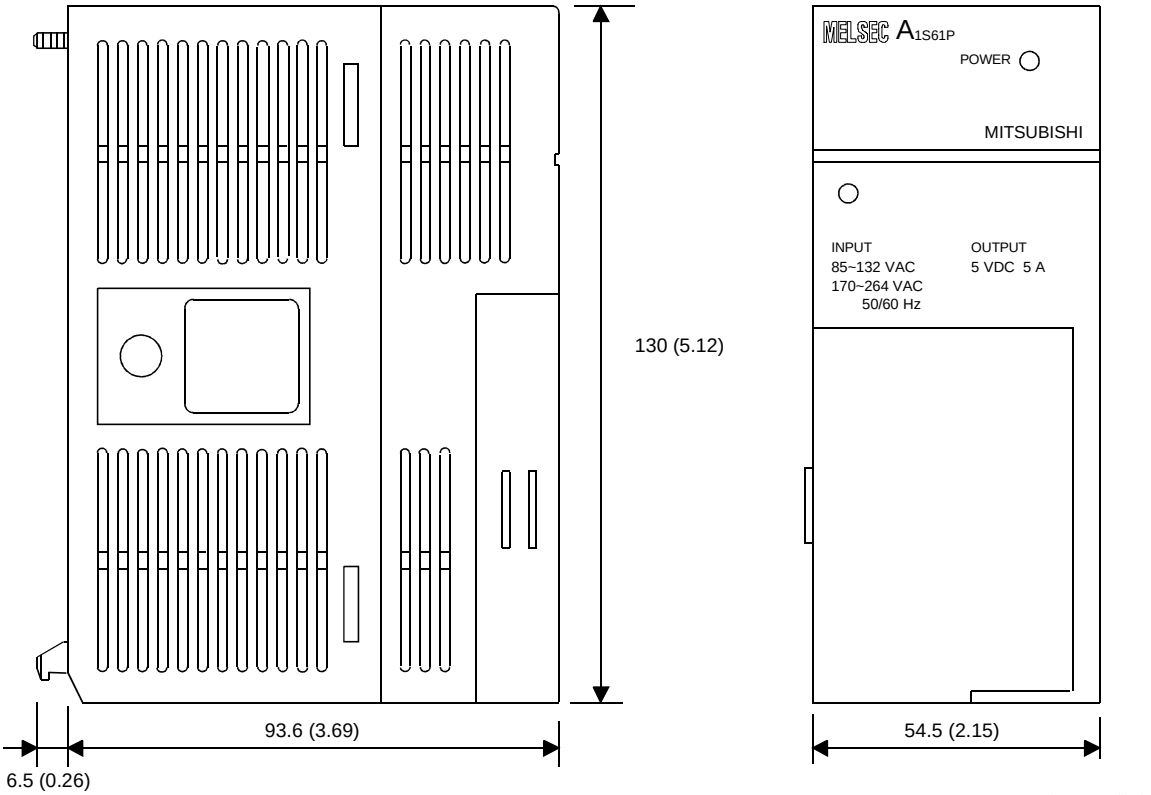
Unit : mm (in.)

Appendix 6.1.2 A1SJHCPU module



Unit : mm (in.)

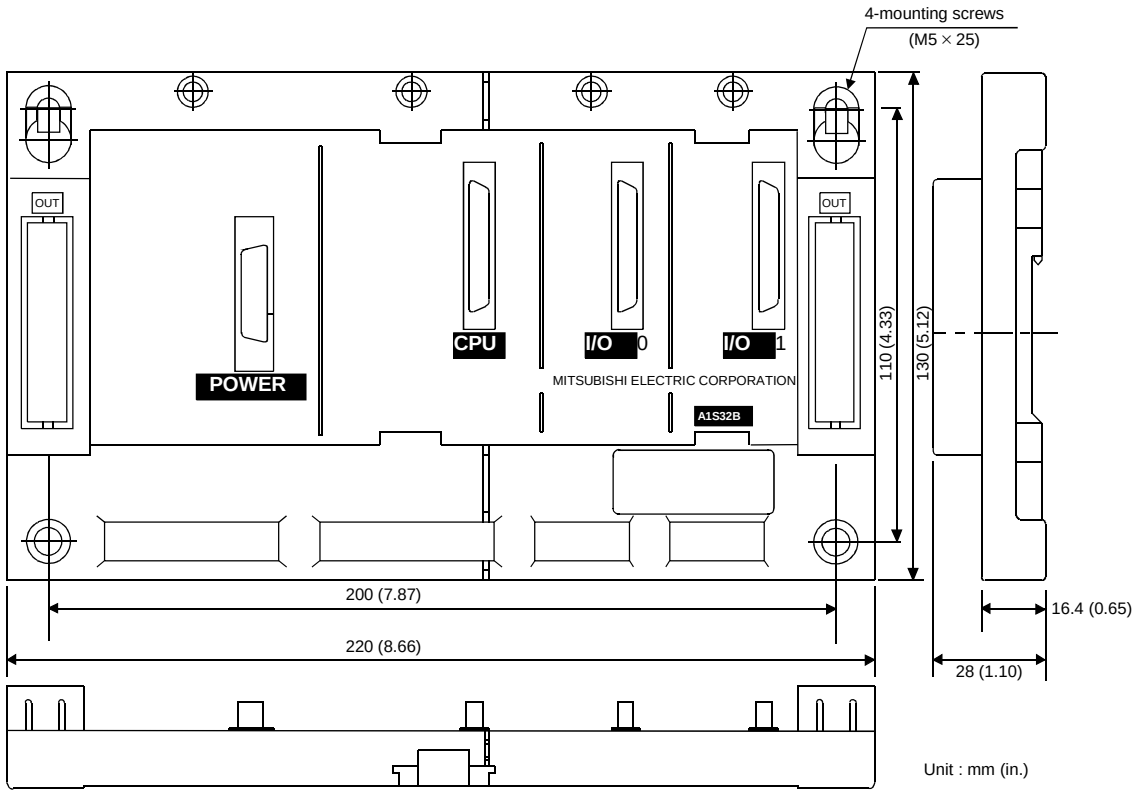
Appendix 6.2 A1S61P/A1S62P/A1S63P/A1S61PEU/A1S62PEU/A1S61PN/A1S62PN Power Supply Module



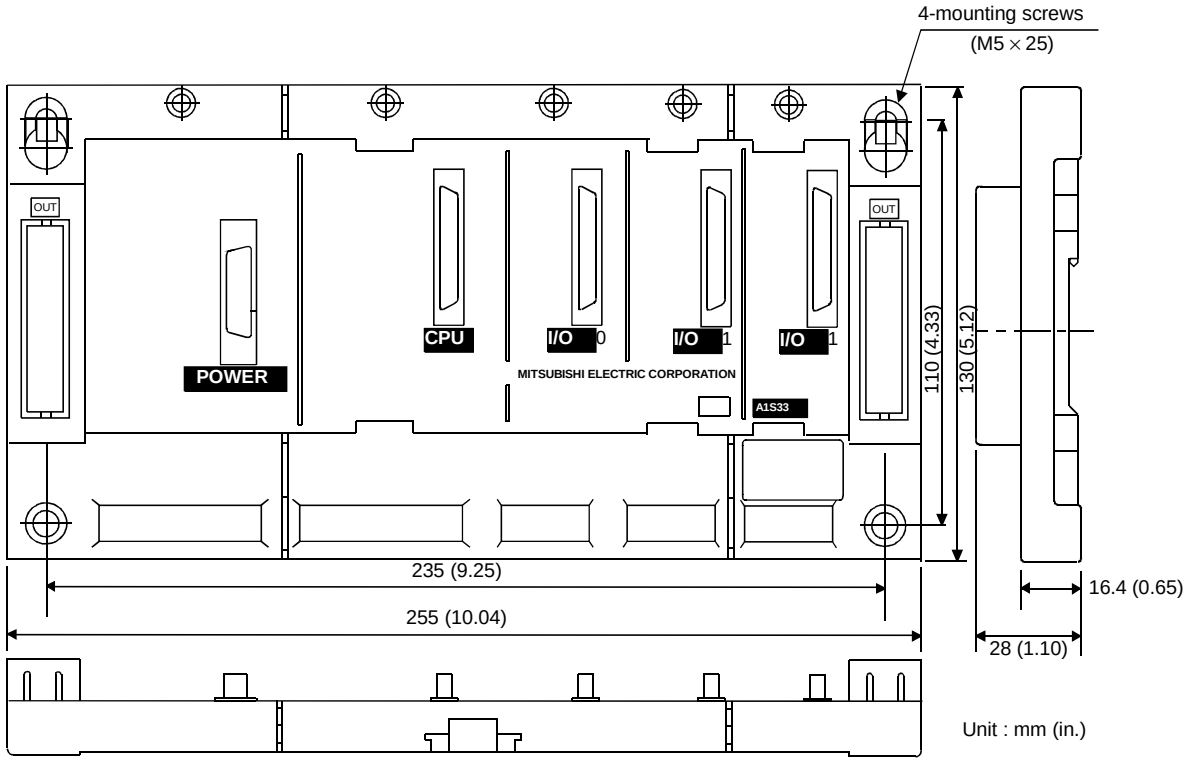
Unit : mm (in.)

Appendix 6.3 Main Base Units

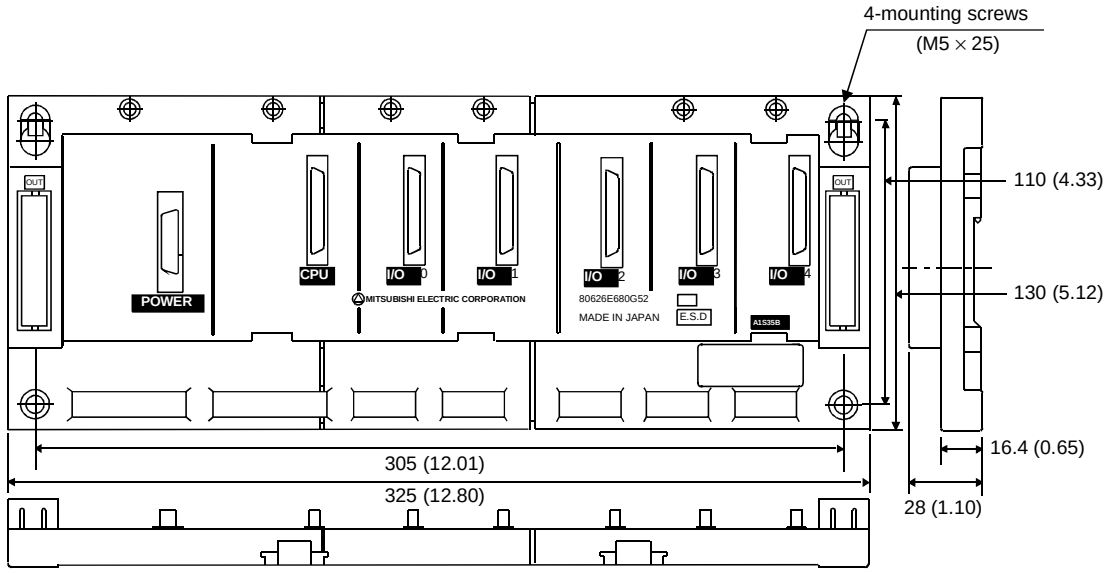
Appendix 6.3.1 A1S32B main base unit



Appendix 6.3.2 A1S33B main base unit

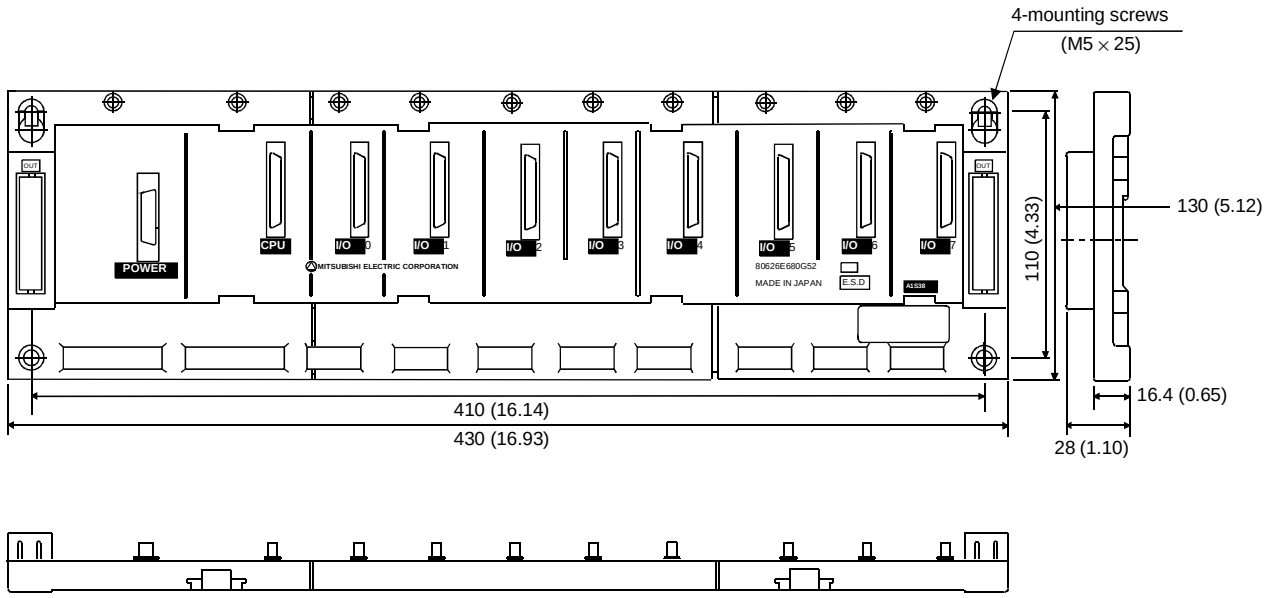


Appendix 6.3.3 A1S35B main base unit



Unit : mm (in.)

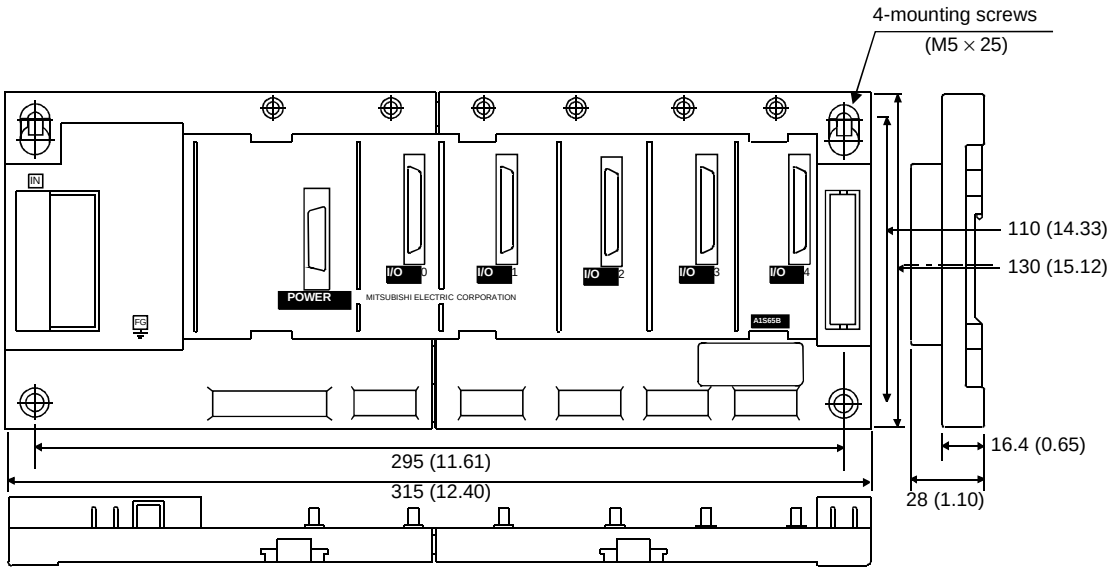
Appendix 6.3.4 A1S38B main base unit



Unit : mm (in.)

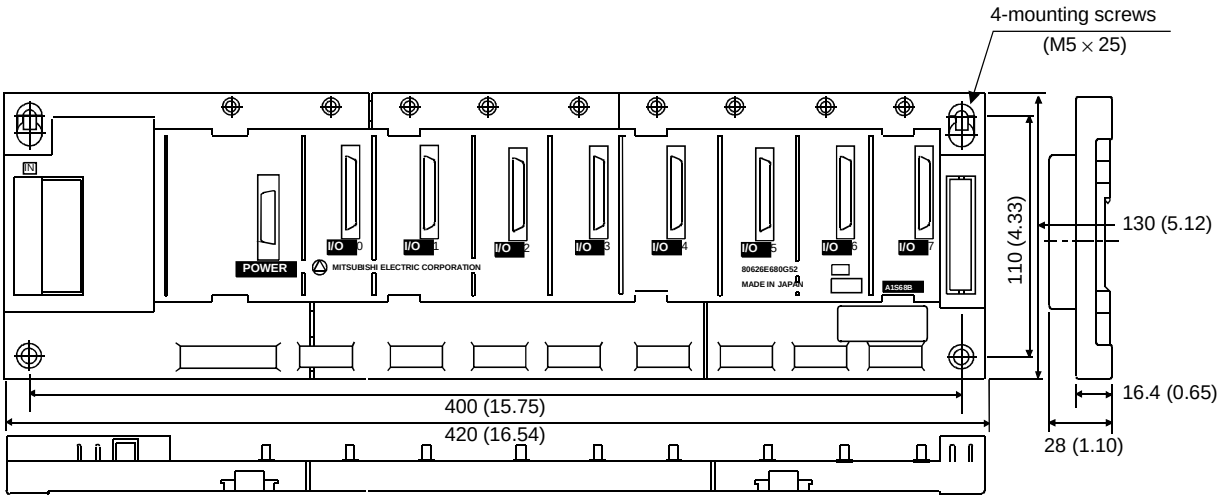
Appendix 6.4 Extension Base Units

Appendix 6.4.1 A1S65B extension base unit



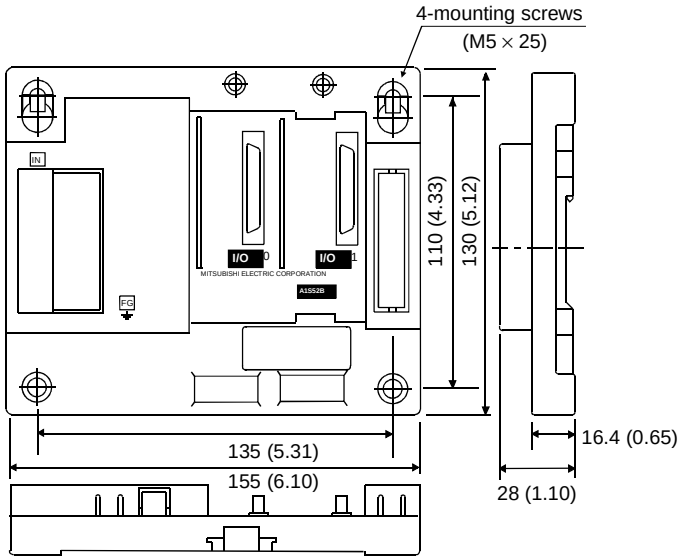
Unit : mm (in.)

Appendix 6.4.2 A1S68B extension base unit



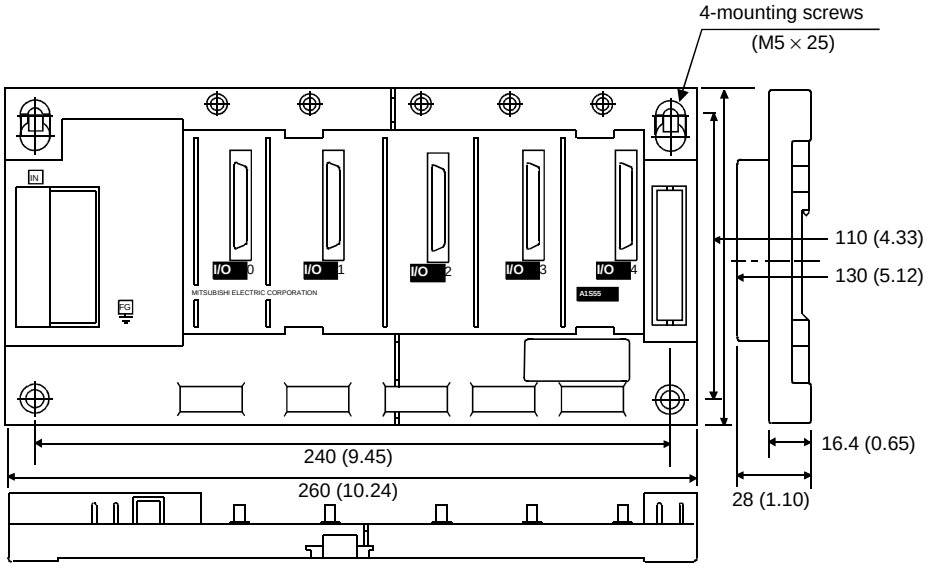
Unit : mm (in.)

Appendix 6.4.3 A1S52B extension base unit



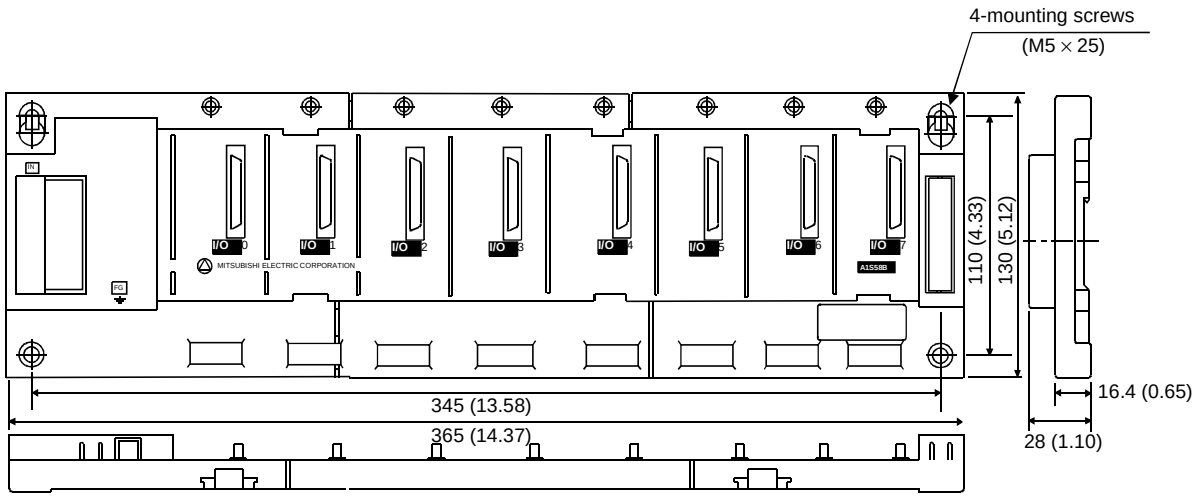
Unit : mm (in.)

Appendix 6.4.4 A1S55B extension base unit



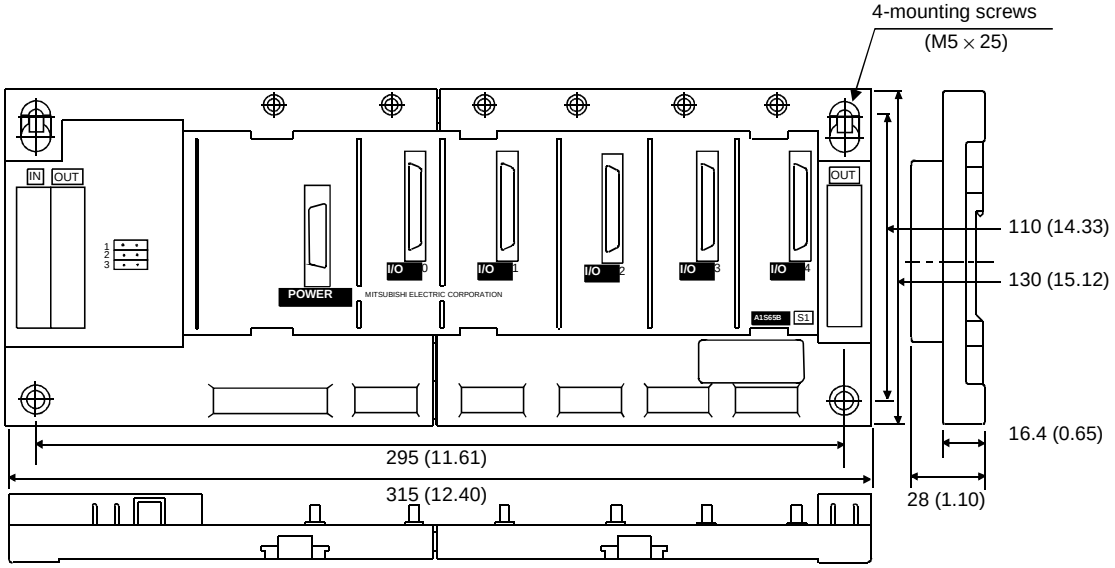
Unit : mm (in.)

Appendix 6.4.5 A1S58B extension base unit



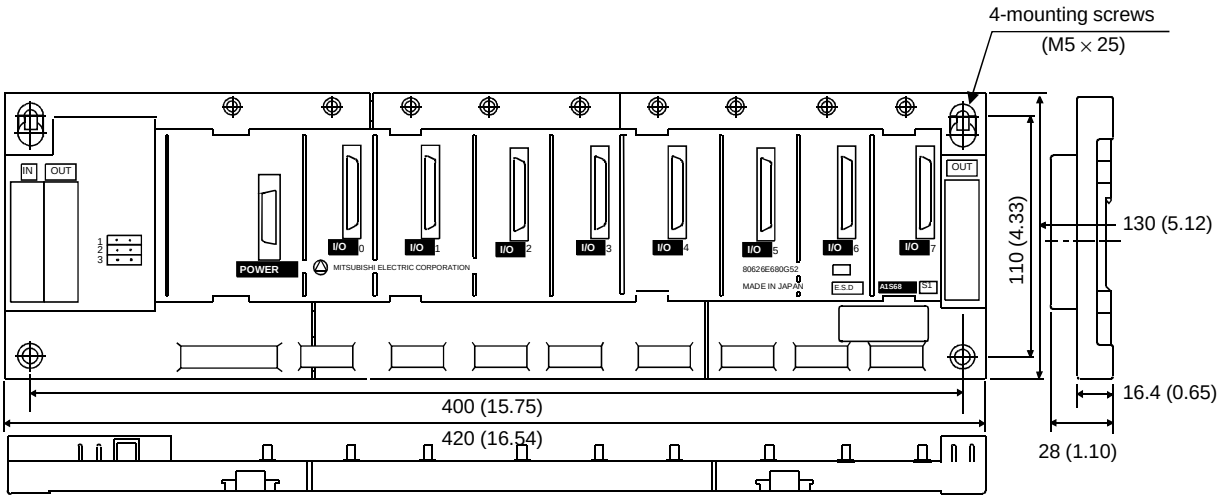
Unit : mm (in.)

Appendix 6.4.6 A1S65B-S1 extension base unit



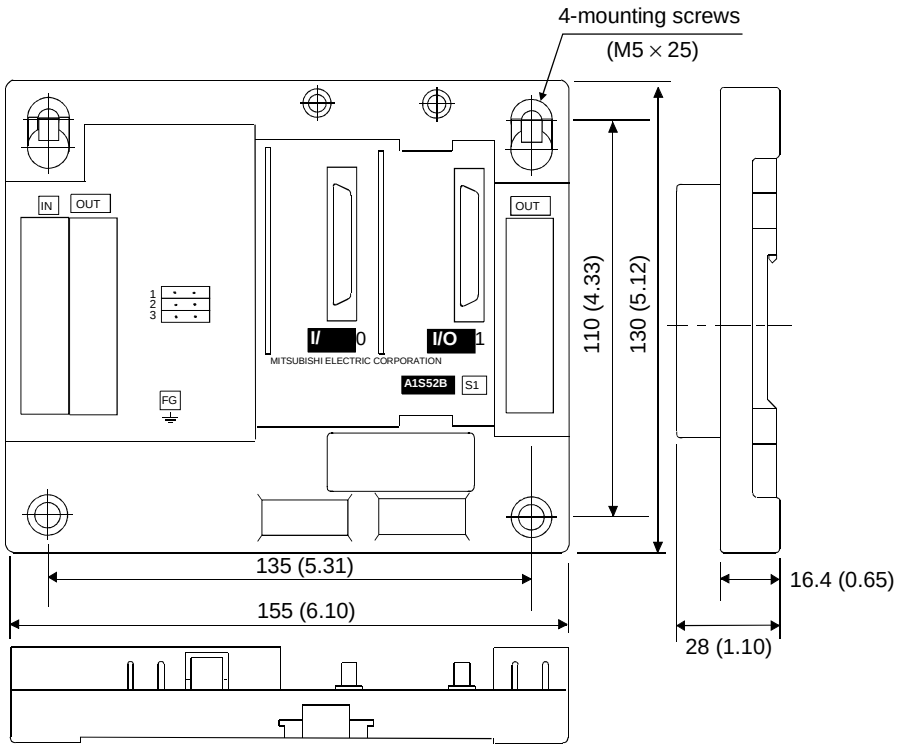
Unit : mm (in.)

Appendix 6.4.7 A1S68B-S1 extension base unit



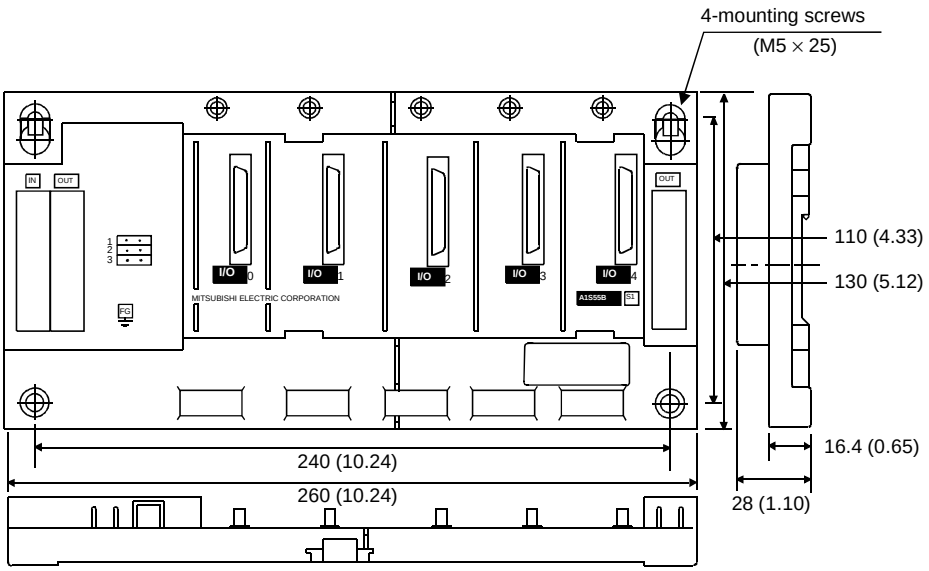
Unit : mm (in.)

Appendix 6.4.8 A1S52B-S1 extension base unit



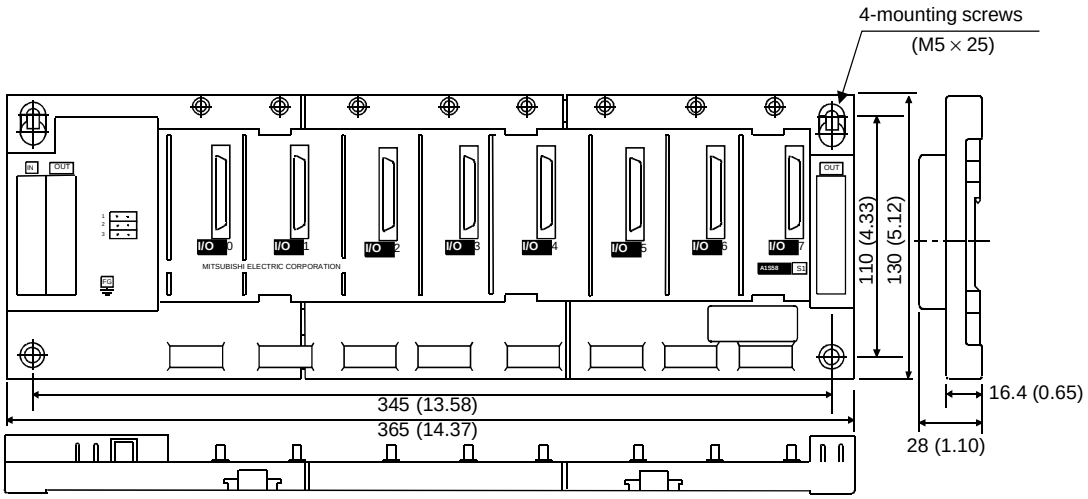
Unit : mm (in.)

Appendix 6.4.9 A1S55B-S1 extension base unit



Unit : mm (in.)

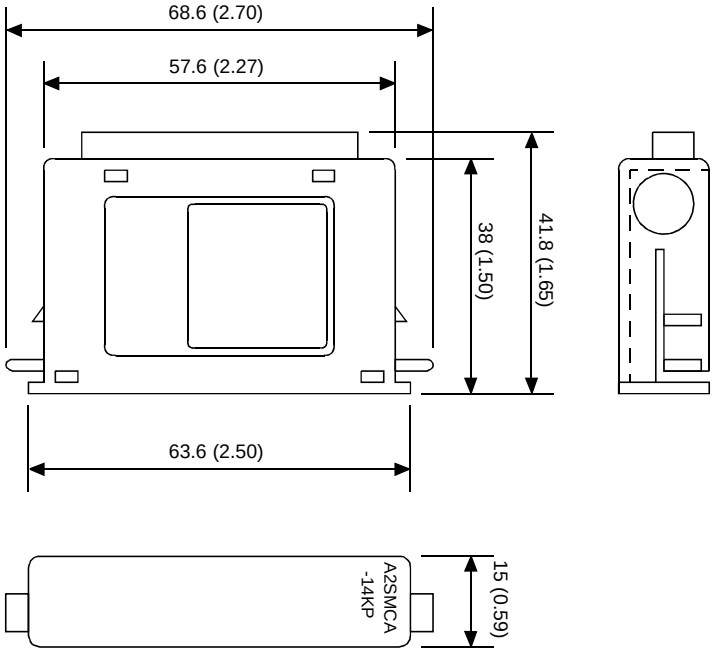
Appendix 6.4.10 A1S58B-S1 extension base unit



Unit : mm (in.)

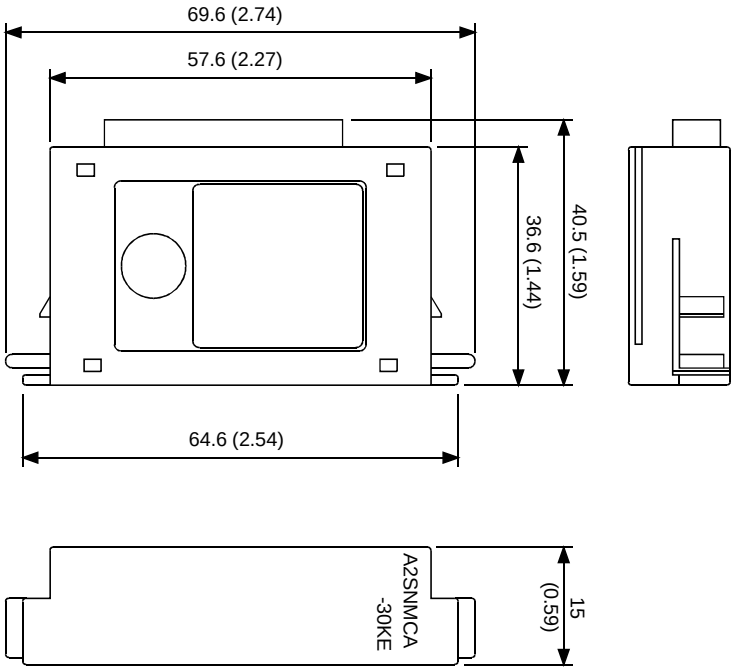
Appendix 6.5 Memory Cassette

Appendix 6.5.1 AnSMCA-[ ] memory cassette



Unit : mm (in.)

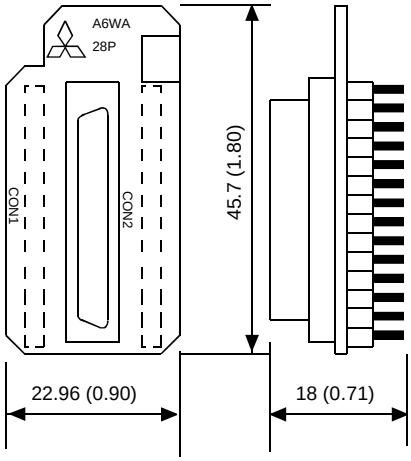
Appendix 6.5.2 AnSNMCA-[ ] memory cassette



Unit : mm (in.)

Appendix 6.6 Memory Write Adapter

Appendix 6.6.1 A6WA-28P memory write adapter



Unit : mm (in.)