Bulletin: 30598-251-01

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Date: February, 1987

Instruction Bulletin

Subject: **SY/MAX®**

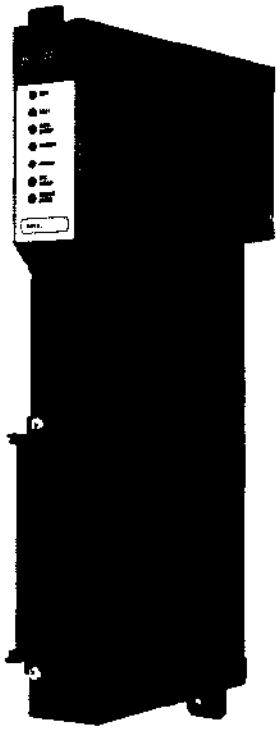
CLASS 8030 TYPES CRM-230, 232
LOCAL/REMOTE TRANSFER INTERFACE SYSTEM

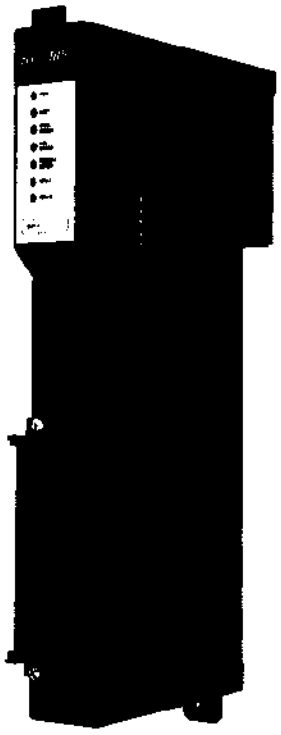
DESCRIPTION

The 8030 CRM-230 Local Transfer Interface and 8030 CRM-232 Remote Transfer Interface modules (collectively referred to as the Transfer Interface System), enable redundant processors to control the input, output system. This instruction bulletin describes the specifications, hardware, installation, and operation of the Transfer Inteface System.

CAUTION

Square D interface modules with different capabilities may be physically interchangeable. Replacement interface modules should be of the same class and type. Any time a replacement is made, the interface's capabilities, processor operation and user programs must be compatible. Refer to the appropriate instruction bulletin for more information.





ATTENTION

These devices contain static sensitive ICs and are subject to damage by electrostatic discharge. Do not handle these devices by the gold edge contacts.

NEW LISTING
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SQUARE D

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1.0 INTRODUCTION

1.1 General Information

The Local and Remote Transfer Interface (LTI and RTI) Modules make up the Transfer Interface System (TIS) for the SY/MAX Programmable Controller family. For critical applications where down-time cannot be tolerated, the TIS will decrease system down-times by enabling redundant processors (Primary and Backup) to control the input/output system, thereby allowing system operation to withstand any single fault in either Primary or Backup Systems without interruption of system I/O control.

1.2 Summary of Operation

The LTI and RTI modules provide the communication between processors and I/O, and supervise the actual transfer of control from a faulty Primary Processor to a Backup Processor. All communication is via a two pair, twisted, shielded cable.

The Transfer Interface System consists of two matched CPU racks, each containing a Model 500 or 700 processor and up to seven Local Transfer Interface Modules. The system designates the controlling CPU rack as Primary and the remaining rack as Backup. Should a fault occur in the Primary system, control would be switched to the Backup and the given designations would change. Each LTI in the Primary rack is paired with another in the Backup rack.

The LTI has two communication channels — a Register Transfer Channel (RTC) and I/O Channel. The RTCs of each LTI pair are connected together to transfer registers from one LTI to the other, synchronize processor scans, and determine when to switch control. The I/O Channel is wired to and controls the input and output devices via the Remote Transfer Interface.

The RTI has two communication channels — A and B, to connect to the I/O Channel of the Primary and Backup LTIs.

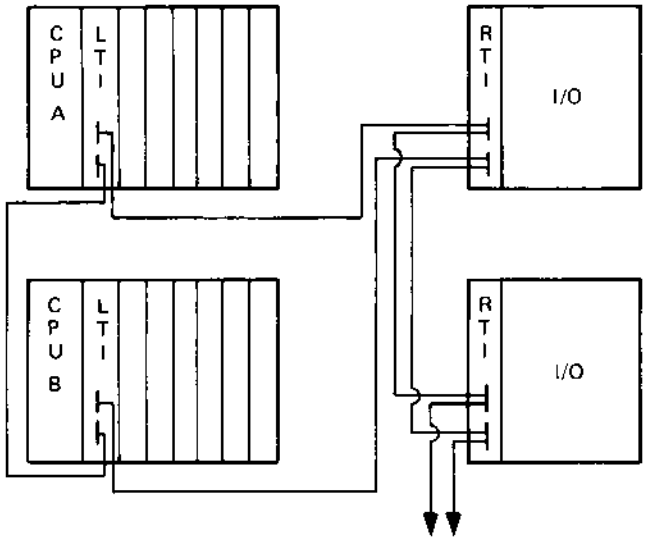


Figure 1.1 — Transfer Interface System

2.0 SPECIFICATIONS

2.1 General Information

The Local and Remote Transfer Interface Modules, as well as the entire SY/MAX Programmable Controller family, are designed and manufactured to comply with U.L. requirements. Refer to UL File Number E85106.

2.2 Electrical

2.2.1 CURRENT DRAW (ON SY/MAX POWER SUPPLY)

8030 CRM-230 Local Transfer Interface 1.6 Amps @ 5 VDC
8030 CRM-232 Remote Transfer Interface 1.0 Amps @ 5 VDC

2.2.2 CAPABILITIES

Registers:
CRM-230 contains 4096 registers (255 for external drop addressing, 3841 for internal data storage). Unused external registers may also be used for internal data storage. All registers which follow those assigned to Channel 2 are retentive.

I/O Channel:
1 I/O Channel per Local Transfer Interface.
255 Registers maximum.
1024 Digital I/O maximum.
8 Drops maximum.

Drops:
128 Digital I/O per drop maximum.
127 Registers per drop maximum.

Available I/O Points:
1024 Digital I/O per LTI.
255 Analog I/O per LTI.
Maximum of 7 LTI's per system.

Register Transfer Channel:
1 Register Transfer Channel per Local Transfer Interface.
32 Registers transferrable per ladder scan.
4096 Registers transferrable upon system startup.

Communication Method:
Continuous full duplex serial differential.

Transmission Rate:
I O Channel — 62.5K Baud.
Register Transfer Channel 375K Baud.

Transmission Distance (using recommended cable -- Belden 8723):
I O Channel - 2500 ft. (762m.) max.
Register Transfer Channel -- 25 ft. (7.6m.) max.

I O Channel Update Times for Digital I O (approximate values):
1 drop, 16 I/O - 5 ms.
1 drop, 128 I/O — 19 ms.
8 drops, 1024 I/O — 91 ms.

Transfer Control Switch Times:
3 CPU scans or 60 ms (whichever is greater) from detection of fault if RTC communication link is intact (regardless of whether or not scans are synchronized, i.e. whether transfer is bumpless or bump).

3 CPU scans or 250 ms (whichever is greater) from detection of fault if processors are not synchronized (bump transfer) and RTC communication link is not intact.

2.2.3 COMPATIBILITY WITH PROCESSORS

The Transfer Interface System is compatible with Model 500 (Series M or later) and Model 700 (Series C or later) processors.

The TIS is not compatible with Model 300 processors.

2.2.4 COMPATIBILITY WITH RACKS

The Local Transfer Interface Module must be mounted in a register slot of the RRK-100 or RRK-200 CPU rack. The Remote Transfer Interface Module is mounted in the CPU slot of any digital or register I O rack except for the Control Station I O rack — the LRK-100.

2.2.5 COMPATIBILITY WITH I/O

The Remote Transfer Interface is compatible with:
All register modules.
All 16 function I/O modules (cannot be used in the CPU rack).
All 8 function I/O modules.
All 4 function input modules.
All 4 function output modules, Series B or later.
Bus Expander, Class 8030 Type CRM-115/116, Series D or later.

2.3 Environmental

Ambient Temperature
Operating: 0°C to 60°C (32° to 140°F).
Storage: -40°C to 80°C (-40° to 176°C).

Humitidy: 5% to 95% non-condensing.

2.4 Physical

Dimensions (W x H x D)
CRM-230, 232 ..... 1.5 x 12.8 x 6.6 in.
3.81 x 32.5 x 16.76 cm.

Weight (approximate)
CRM-230, 232 ..... 3.0 lbs/1.36 kg.

3.0 DESCRIPTION OF HARDWARE

The LTI and RTI modules have seven diagnostic LEDs and a removable terminal strip. A marking area is provided for system identification.

Click here to view graphic.

Figure 3.1 — Local Transfer Interface

Click here to view graphic.

Figure 3.2 — Remote Transfer Interface

3.1 LED Indicators

The Local and Remote Interface Modules have the following LED indicators:

LOCAL TRANSFER INTERFACE	REMOTE TRANSFER INTERFACE
RUN (green)	RUN (green)
HALT (red)	HALT (red)
CHANNEL ERROR (red)	CHANNEL ERROR (red)
PRIMARY (green)	I/O ERROR (red)
BACKUP (green)	MODULE ERROR (red)
RTC ERROR (red)	CPU A (green)
MODULE ERROR (red)	CPU B (green)

Note that when the Transfer Interface System is powered up and operating with a backup in RUN synchronized with the Primary (bumpless transfer mode), the LED indicators will be displayed as follows:

LTI - RUN and either PRIMARY or BACKUP steady ON.
RTI - RUN and either CPU A or CPU B steady ON, with complement (CPU A or CPU B) flashing ON and OFF.

LED functions are as follows:

LOCAL TRANSFER INTERFACE

Name	Color	Function
RUN	GREEN	When ON indicates the I/O channel is fully operational and the CPU is accessing the image table (note CPU need not be in RUN). When OFF indicates the module is either in self-diagnostics or has failed. When flashing (50% duty cycle) indicates that one or more drops have been programmed to halt (bits 1 through 8 of the LTI I/O channel control register).
HALT	RED	The complement of the RUN LED.
CHANNEL ERROR	RED	When ON indicates one or more drops are shut down due to a communication problem. When OFF indicates all drops are operational. When flashing indicates that a drop has shut down due to a failure on the drop (typically a remote bus error).
PRIMARY	GREEN	When ON indicates the LTI is in Primary status. When flashing (50% duty cycle) indicates a Backup which is not able to become Primary. When blinking (10% duty cycle) indicates a Backup in "bump transfer" mode.
BACKUP	GREEN	The complement of the primary LED with the exception of a 90% duty cycle to indicate a backup in "bump transfer" mode.
RTC ERROR	RED	When ON indicates the RTC is not receiving communication. When OFF the RTC is fully operational. When flashing, indicates the RTC is receiving data but the other RTC is not.
MODULE	RED	When ON indicates the LTI has recognized a bus error and has halted the CPU. Note this does not necessarily mean the LTI itself is bad. When OFF indicates the LTI itself is operational, despite the possibility that other LTI error LED's may be ON.

REMOTE TRANSFER INTERFACE

Name	Color	Function
RUN	GREEN	When ON indicates the drop has been initialized and is operating normally. When flashing (50% duty cycle) indicates the CPU is in DISABLE OUTPUTS. When blinking (10% duty cycle) indicates that the LTI halt bit has been set for that drop.
HALT	RED	When ON indicates that the drop either has not initialized or has been shut down dut to program control. When flashing (50% duty cycle) indicates the CPU is in DISABLE OUTPUTS. When blinking (90% duty cycle) indicates that the LTI halt bit has been set for that drop.
CHANNEL	RED	When ON indicates a communication problem with the LTI. When flashing indicates a Primary is present but that no communication has been established with the Backup.
I/O ERROR	RED	When ON indicates a problem has been detected on the remote rack (not necessarily an RTI failure). When flashing indicates outputs on the drop have been FROZEN.
MODULE	RED	When ON indicates a self-diagnostic error. If error is transient, power-cycling the drop will allow recovery.
CPU A	GREEN	When ON indicates CPU A is Primary. When flashing (50% duty cycle) indicates CPU A is in ready Backup status. When OFF indicates CPU A is neither Primary nor a ready Backup.
CPU B	GREEN	Same conditions as CPU A LED except applied to CPU B.

3.2 Communication Channels

3.2.1 LOCAL TRANSFER INTERFACE

The LTI has two communication channels, an I/O Channel and a Register Transfer Channel (RTC). A removable terminal block is used to wire the two pair, twisted, shielded cable to the module.

3.2.2 REMOTE TRANSFER INTERFACE

The RTI has two communication channels, A and B, to connect to the redundant CPU racks (I/O channel of respective LTIs). The RTI has redundant serial transmitters and receivers, but the remaining RTI circuitry is not duplicated. A removable terminal block is used to connect the two pair, twisted, shielded cable to the module.

3.3 LTI RESTART Pushbutton

The RESTART pushbutton on the front of the LTI module serves two purposes, depending on whether the LTI is in the PRIMARY or BACKUP rack.

—In PRIMARY RACK

When the LTI is PRIMARY, the RESTART pushbutton may be used to restore communications on the I/O channel (between an LTI and RTI). The RESTART pushbutton is operational on a PRIMARY LTI when all of the following conditions exist:

1. CPU must be running.
2. Communications error must have originated on the I/O channel.
3. I/O FAILURE OVERRIDE bit must be ON. See Appendix B, LTI Control Registers.
4. It must now be possible to establish valid communications to the affected racks — otherwise no change of state will occur.

NOTE: The RESTART button will only restart drops which were shut down due to communication errors or remote bus errors. It will have no effect if a CPU rack error exists.

WARNING
Pressing the RESTART button on the front of the LTI module may cause outputs to turn ON or OFF as dictated by the resumption of communication.

—In BACKUP RACK

When the LTI is BACKUP, the RESTART pushbutton may be used to regain synchronization of the Register Transfer Channel between the PRIMARY and BACKUP. The RESTART pushbutton is operational on a BACKUP LTI when all of the following conditions exist:

1. CPU must be running.
2. Communications error must have originated on the RTC channel.
3. RTC Failure Override bit must be ON. See Appendix B, LTI Control Registers.
4. It must now be possible to establish valid communications between the LTI's via the RTC cable.

WARNING
Pressing the RESTART pushbutton, with all conditions met, will cause registers to be transferred between LTIs. Ladder scans will be stopped during that time for up to approximately 1/2 second. Thus, the restart should not be attempted during a critical operation.

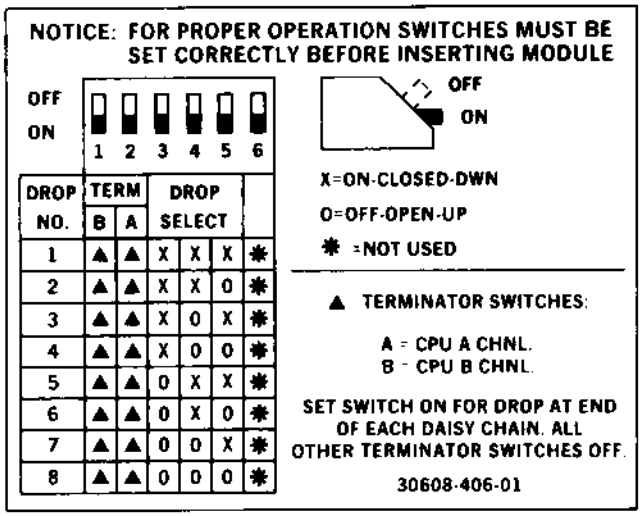
3.4 RTI DIP Switches

The RTI module has six dip switches on the rear of the module near the edge of the circuit board. See Figure 3.3. Each RTI module must be assigned as one of the eight drops on the LTI I/O Channel. The switches must be set correctly for the system to operate properly. See Section 4.4, RTI DIP Switch Settings. Also, terminator switches must be set for the farthest drop on the channel. A label on the side of the module describes the switch settings. See Figure 3.4.

Click here to view graphic.

Figure 3.3 — RTI DIP Switches

NOTE: The Remote Transfer Interface DIP switches are the only hardware changes to be made by the user.



DROP NO.	TERM B	TERM A	DROP SELECT			
1	▲	▲	X	X	X	✱
2	▲	▲	X	X	O	✱
3	▲	▲	X	O	X	✱
4	▲	▲	X	O	O	✱
5	▲	▲	O	X	X	✱
6	▲	▲	O	X	O	✱
7	▲	▲	O	O	X	✱
8	▲	▲	O	O	O	✱

Figure 3.4 — RTI DIP Switch Label

4.0 INSTALLATION

CAUTION

To prevent possible equipment damage, remove power from the CPU and all I/O racks before inserting or removing *any* component (including the LTI or RTI modules or communication cables).

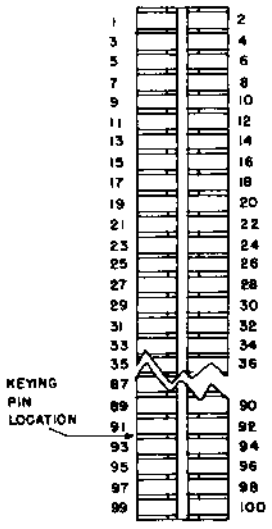
4.1 Inspection

Although each module is subjected to strict quality control procedures, it is always a good practice to give each module a quick visual inspection before installation. Check for any shipping damage that may have occurred.

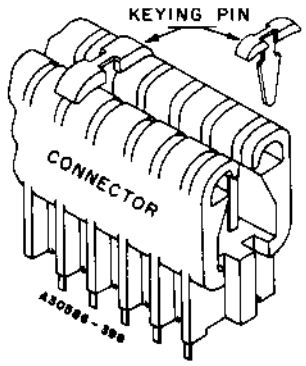
Inspect the LEDs to ensure they are visible. Examine the field-wiring terminals for damage. Inspect the hold down screw on the bottom to verify the screw is securely attached to the module. Examine the upper rear of the module to ensure the mounting plate is secure. Inspect the printed circuit edge connector for damage.

4.2 Module Keying

Each register or CPU slot on a rack assembly may be keyed to accept only one type of module. An optional keying pin kit is available for this purpose, Class 8030, Type CBP-104. The keying pin may be inserted manually into the slot using the keying pin insertion tool provided with this kit. The correct positioning of the keying pin for the LTI module is between pins 92 and 94 (see Figure 4.1). There is no special keying pin location for the RTI module.



Keying Pin Location



Keying Pin Insertion

Figure 4.1 — Module Keying

CAUTION

When inserting or removing the keying pins, use care to avoid touching the contact fingers within the connector. Improper insertion/removal may damage the connector.

4.3 Module Location

4.3.1 LOCAL TRANSFER INTERFACE

The Local Transfer Interface (LTI) module must be placed in the same rack assembly as the Model 500 or 700 processor. The first LTI in a Transfer Interface system should be placed in the third slot of the register rack, though any slot is acceptable. Additional LTIs are placed in adjacent register slots.

4.3.2 REMOTE TRANSFER INTERFACE

The Remote Transfer Interface (RTI) module must be placed into the CPU slot (slot #1) of any rack which is to be a drop. Only one RTI is required and allowed for each drop.

4.4 Setting the RTI DIP Switches

Before putting an RTI into a rack assembly, set the DIP switches for correct operation. The bank of six switches is accessible from the rear of the module. The switches are ON when they are set towards the PC board.

Switches 3, 4, and 5 should be set according to the label on the RTI module (Figure 3.4) to specify the drop number of the rack on the I/O Channel.

Switches 1 and 2 are terminators which must be properly set to minimize the electrical interference on the communications link. For each LTI I/O Channel, the last RTI on the channel (the unit farthest along the link from the LTI) must have the terminator switch ON. Note that because the I/O Channel is redundantly controlled, it is possible to use different wire routing from processor A and from processor B. Therefore, there are two terminator switches on the RTI — one for processor A (switch 2) and one for processor B (switch 1). All other RTIs on the channel must have the terminator switches OFF.

NOTE: Switch 6 is not used.

CAUTION

Before operating the Transfer Interface System, be sure that all RTI DIP switches are set properly. Improper switch settings will cause unpredictable system operation.

4.5 Installation in Rack Assembly

Power must be removed from the rack assembly before installing or removing the Local or Remote Transfer Interface Modules.

After the removal of power, release the latching clamp and insert the module into the appropriate register slot until firmly seated against the stud located above the socket for the slot. *Close the latching clamp and be sure to tighten the captive screw to insure the module is secured and properly grounded.* To remove the module, simply release the latching clamp, loosen the captive screw at the bottom and pull the module out of the slot using the finger tab located on the top of the module.

NOTE: Refer to the Planning and Installation Guide (I.B. 30598-175-XX) for proper grounding procedures.

4.6 Field Wiring

4.6.1 I/O CHANNEL CONFIGURATION

The LTI's I/O Channel *must* be wired in a daisy chain configuration to the RTI modules. Figure 4.2 illustrates this typical configuration. *A "star" wiring configuration is not allowed anywhere along the I/O channel with the Transfer Interface System.*

Note that all LTIs in the CPU rack selected as CPU A must be connected to the CPU A channel of the RTIs. Likewise, LTIs in CPU B rack must be connected to the CPU B channel of the RTIs. There can be no intermixing: wiring from CPU A LTIs must *not* be connected to any of the CPU B RTI terminals and vice versa.

NOTE: "CPU A" and "CPU B" terminals must be wired consistently for each drop (A to A and B to B). Otherwise the RTI will generate error code 29510 and not go to RUN, regardless of the state of the I/O Failure Override bit.

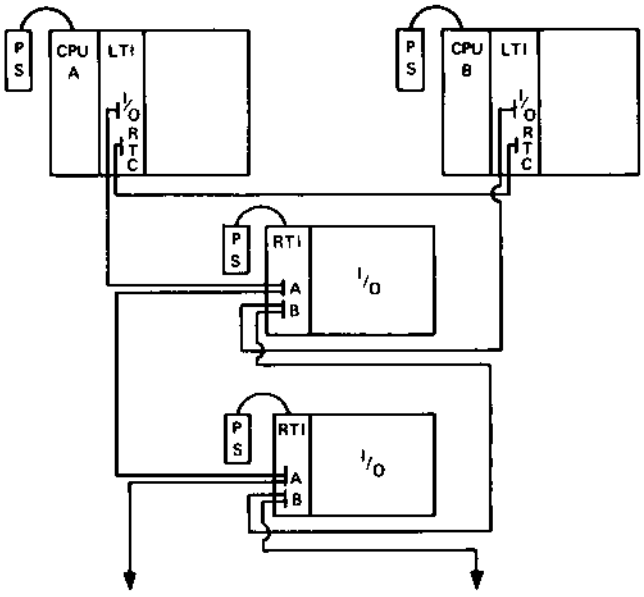


Figure 4.2 — I/O Channel Wiring Configuration

4.6.2 COMMUNICATION CABLE

The communication between modules of a Transfer Interface System takes place via a two pair, twisted, shielded cable. In order to minimize the potential of electrical interference:

1. Route communication cable in separate wire ducts, away from power wiring and electro-magnetic devices.

2. Connect each end of the communication cable shield to the SHD terminal on each device. *Do not connect this shield to an external ground point since the SHD terminals are capacitively coupled to ground.*

Follow all applicable electrical codes for wiring and communication cable routing.

Communication cable should be equivalent to Belden 8723. Using a cable with different specifications may cause unreliable operation.

The maximum communication distance for the Belden 8723 or equivalent cable is as follows:

Communication Channel	Maximum Length
I/O Channel	2500 feet (762 m.)
Register Transfer Channel	25 feet (7.6 m.)

Because the Transfer Interface System uses redundant LTI-to-RTI communication cables, it is possible (and probably desirable) to route the two cables separately or in different wire ducts. This practice will minimize the chances of both communication cables being broken or damaged simultaneously.

NOTE: ADDITIONAL DATA LINE PROTECTION.

In environments where lightning or induced transients over communication lines are likely to cause communication failures, signal line protection devices are recommended. Even though transient protection is designed into SY/MAX communication circuits, additional specialized protection devices are suggested for communication lines that are exposed to the outside environment. Refer to Appendix G, Additional Data Line Protection, for recommended wiring scheme and protection devices.

Authoritative reference material which discusses the art and science of noise reduction and data line protection includes the ANSI/IEEE Std. 518-1982 as well as a book entitled *Noise Reduction Techniques in Electronic Systems* by Henry Ott (Wiley-Interscience 1976).

4.6.3 LTI/RTI CONNECTIONS

There are five terminals on the LTI and RTI modules for each communication link connection. These terminals are labeled 1, 2, 3, 4, and SHD.

The twisted-pair continuity of the communication cables must be maintained in the communication links (i.e., Black with Red and Green with White for Belden 8723 cable). The RTC communication link for each pair of LTI modules are connected together as in Figure 4.3. This distance is restricted to a maximum of 25 feet.

*Note that for the RTC communication link, the wiring crisscrosses: terminals 1 & 2 of one LTI connect to terminals 3 & 4 of its matched LTI, and vice versa.

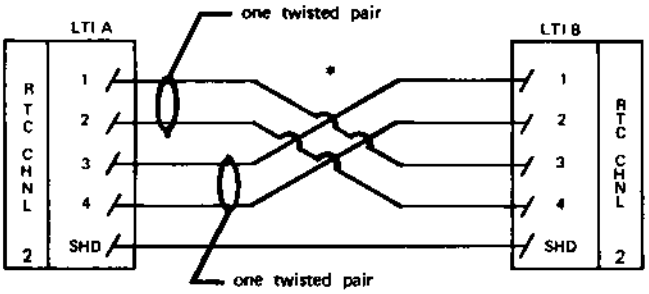


Figure 4.3 — RTC Channel: LTI-to-LTI Connections

The I/O communication link betwen the LTIs and RTIs is wired as shown in Figure 4.4. A maximum of two communications wires should be connected to each RTI terminal since each RTI in the daisy chain should be wired to the next RTI "straight through."

Note that for the I/O communication link, the wiring is direct: there is no crisscrossing.

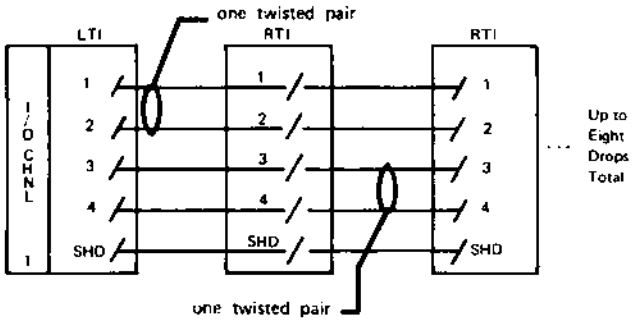


Figure 4.4 — RTC Channel: LTI-to-RTI Connections

4.7 Power Supplies

The Transfer Interface System (TIS) will continue to keep the programmable controller system running if there is a fault in either the Primary or Backup CPU rack power supplies. To enable the TIS to withstand such a fault, *each* CPU rack must be powered by a separate power supply. To further insure redundancy, power supplies can be connected to separate branch circuits. In addition we recommend that a CPU rack power supply should *not* be used to power any other rack assemblies.

Ideally, to promote redundancy the processors and I/O racks should be on three (or more) separate branch circuits; otherwise they should all be on the same circuit. If one processor is on the same circuit as some of the remote racks and that circuit should lose power, this will defeat the purpose of redundant processor control.

For additional reliability, redundant SY/MAX power supplies may be used to power each respective rack. This feature is available by utilizing two PS-11, -21, or -31 Power Supplies with a CC-51 redundant cable. Refer to Power Supply instruction bulletin 30598-159-01 or later for additional information.

5.0 OPERATION

5.1 General Description

The Transfer Interface System allows redundant SY/MAX processors to communicate with and control input and output devices.

The Transfer Interface System (TIS) consists of:

1. Local Transfer Interface (LTI) Modules which reside in register slots of the redundant CPU racks.
2. Remote Transfer Interface (RTI) Modules placed in the CPU slot of remote digital or register I/O racks.
3. Communication cable to support I O and LTI-to-LTI transmissions.

The TIS is composed of two matched CPU racks, each containing a Model 500 or 700 processor and up to seven Local Transfer Interface Modules. The system designates the first processor to power up and go into RUN as the Primary (or controlling CPU) and the other redundant processor as Backup. Should a fault occur in the Primary system (communication error, CPU rack power supply failure, processor failure, or LTI failure), control would be switched to the Backup and the aforementioned designations would be exchanged: the Backup would become the Primary and vice versa.

A key point to understanding the Transfer Interface System is that it will attempt to keep the PC system operational and running in the event of a single CPU rack or I/O communication fault in either of the redundant systems. If a fault should occur in the Primary system, control is switched to the Backup system, which then becomes the Primary controlling system. The failed system, which is now in the failed Backup status, must be repaired and put into RUN in order for the Transfer Interface System to again be able to sustain another fault.

The Transfer Interface System is capable of making two types of transfers — bumpless and bump transfers. Bumpless transfers are those that occur when the Backup is completely synchronized with the Primary processor. I/O states, data values and processor scans are synchronized in both units, so there are no sudden changes in the I/O when this type of transfer occurs. Bump transfers are those that take place when the Backup has lost synchronization with the Primary. The Backup can lose synchronization for several reasons, including broken communication cables or severe noise. When the Backup is out of sync, data and I/O values may be different in the two units. If a transfer occurs before the Backup is able to regain synchronization, some I/O values may change when the new processor takes over. This is a "bump" transfer. If it is undesireable to allow bump transfers, the Backup can be programmed to the shutdown when it loses sync with the Primary, rather than continue to run out of sync.

The LTI has two communication channels — an I/O Channel and a Register Transfer Channel (RTC). The function of the RTC will be explained later.

The I/O Channel is a serial, multi-drop communication channel that is wired to the RTI drops to control input and output devices. The LTI receives instructions from the CPU. The LTI then serializes this information and transmits it over the I/O Channel to the appropriate RTI. This channel operates full duplex at a rate of 62.5K baud.

The Remote Transfer Interface (RTI) has two communication channels (A and B) to connect to the I/O Channel of the Primary and Backup LTI modules, respectively. Data such as I/O commands and status is transmitted back and forth between the LTIs and RTIs. The information being exchanged is stored in an image table located in each LTI and RTI.

The continuous exchange of information between the LTI and RTI image tables is independent of the CPU scan. Transmitted information includes ON/OFF commands for I/O, storage register information, housekeeping functions (i.e., loss of communications, error control, freeze or reset of I/O). In addition, information regarding the status of the Primary and Backup systems is exchanged via the I/O Channels.

The LTI module stores control register information which is transmitted to the RTI. This information (user programmable bits) defines the action to be taken in the event of a fault at any drop. It can allow the operational drops to keep running or to shut down. The shutdown state of the outputs will then be either a reset (OFF) or freeze (maintain last state) condition.

Each Local Transfer Interface in the Primary rack must be matched to another in the Backup rack. The Register Transfer Channels of each LTI pair are connected together. Through the RTCs, internal registers are transferred from the Primary LTIs to the Backup LTIs, processor scans are synchronized, and determination is made when to switch from Primary to Backup control.

Actual programming steps are described in the programming equipment instruction bulletins. For details on user programmable bits, refer to Appendix B, LTI Control Registers.

For an example Transfer Interface System, See Appendix D.

5.2 Local Transfer Interface Registers

The 8030 CRM-230 Local Transfer Interface has 4096 registers. Although these registers exist, the ability to address them is dependent upon the type of SY/MAX Processor used. The first 255 registers are available for addressing external inputs and outputs, register modules, storage registers or internals. The remaining registers (3841) are only available for use an internal relay equivalents, timers, counters, and data storage.

The first four registers immediately following the registers assigned for external I/O are required for the Register Transfer Channel (LTI-to-LTI communications link) and must be rack addressed to channel 2, drop 1. Note if all 255 registers (the maximum) were assigned to external I/O, these would then be assigned to registers 256 through 259.

5.2.1 EXTERNAL REGISTERS

A maximum of 255 consecutive registers can be assigned to the LTI I/O Channel. The I/O Channel can be connected to up to 8 drops. (A drop is an I/O rack with a RTI installed.) Any drop may have a maximum of 127 registers assigned to it. The first 8 registers assigned to a drop are available for digital or register I/O. (8 registers x 16 points per register yield 128 I/O points per drop.) Any registers beyond the first 8 assigned to each drop are only for register I/O.

To maintain identical control status, both the Primary and Backup LTI modules (and CPUs) read the condition of all external registers. Only the Primary processor can alter these registers, thereby controlling the I/O.

Upon halting or loss of power to the Primary processor (assuming Backup cannot take I/O control) the registers assigned to drops will be reset to zero (OFF). However, it is possible to freeze (maintain last state) registers assigned to drops. For more information, refer to Appendix B, LTI Control Registers.

5.2.2 INTERNAL REGISTERS

Internal registers (those not assigned to drops) are used for internal relay equivalents, timers, counters, and data storage. These registers retain information when the processor halts or there is a loss of power (provided CPU rack has battery backup power).

The Register Transfer Channel is used to ensure the matched LTIs have identical internal registers. Upon system startup, internal registers (a user definable group) are automatically transferred from the Primary to the Backup system. In addition, a block of 32 registers may be transferred at the end of every processor scan to ensure identical status. See Section 5.4 for a full description of register transfers.

5.2.3 CONTROL REGISTERS

All LTI modules have a group of control registers used for diagnostics and control. An error code register and a channel control register are available for the I/O and Register Transfer Channels. For more information, refer to Appendix E, Error Codes, and Appendix B, LTI Control Registers.

5.3 Rack Addressing

Rack addressing is a user programmable identification scheme that enables a SY/MAX processor to monitor and control I/O points by assigning registers to them. It provides a memory map of where (i.e., in which registers) I/O information will be stored and handled by the processor (CPU). Note that rack addressing must be identical for both processors.

Once the register addresses have been assigned, they are fixed. If a change in address assignments is required, the user rack addressing software must be changed.

5.3.1 PROCESSOR (CPU) CONSIDERATIONS

The CPU (Model 500 or 700 Processors) determines the maximum system addressing range. SY/MAX processor capabilities are shown in Figure 5.1.

5.3.2 I/O CHANNEL ADDRESSING

The first 255 LTI registers may be assigned to the I/O Channel as external I/O drops (up to 8 drops). To rack address a TIS system, external I/O registers are assigned as drops on Channel 1. All address assignments for the drops must be made in a sequential ascending order. The register addresses for each drop are further distributed in ascending order to individual slots within the drops. Any of the remaining 255 registers not assigned to drops may be used as internal registers.

4 additional registers will be required to utilize the LTI to LTI communication link (Register Transfer Channel).

5.3.3 RTC ADDRESSING

The Register Transfer Channel (LTI-to-LTI communication link) requires four of the first 259 LTI registers for operation. These registers are rack addressed for Channel 2, Drop 1. They establish parameters for the transfer of internal registers and synchronization of the two processors. These registers can be written to by the ladder diagram program, and have the following functions:

REGISTER 1: Startup Transfer Register — determines the number of registers transferred on "start up." See Section 5.4.2, Startup Transfer.

REGISTER 2: End-of-Scan Transfer Register — determines which block of 32 registers are transferred at the end of each scan. See Section 5.4.3, End of Scan Transfer.

REGISTER 3: Scan Synchronization Register — determines the maximum allowed synchronization time between redundant processors. See Section 5.4.4, Processor Scan Synchronization.

REGISTER 4: Primary/Backup Read/Write Register — provides "cross-talking" capability between redundant processors. See Section 5.4.5, Primary/Backup Read/Write Bit Exchange.

5.3.4 LTI CONTROL REGISTERS

LTI control registers are dynamically assigned on the basis of physical position in the CPU Rack and rack addressing assignments.

LTI control registers are automatically assigned in descending order starting with S8163 for the LTI with the lowest numbered

CPU Model	Register Addressing Capability	Self Contained CPU Registers	Maximum Supportable LTI Modules	Practical I/O Compatibility
500	2008 (1)	460 (2)	7	2000
700	8000 (1)	0	7	7168

(1) Only the bits of the first 256 registers in each LTI may be forced ON/OFF.

(2) For internal use only as relays and storage registers. These registers should *not* be used since they *cannot* be transferred. Only registers that reside in LTI modules can be transferred from Primary to Backup.

Figure 5.1 — CPU Address Capabilities

CPU rack slot number. The first LTI control registers are defined as follows:

S8163 — Error Code Register
S8162 — I/O Channel Control Register
S8161 — RTC Control Register

Following the above sequence, S8160 would be the Error Code Register of the second LTI in the rack.

For more information on the operation of the LTI control registers, refer to Appendix E, Error Codes, and Appendix B, LTI Control Registers.

5.3.5 RACK ADDRESSING EXAMPLE

The following example illustrates the concept of rack addressing. Actual programming procedures are not covered. See SY/MAX Programmer instruction bulletins for rack addressing programming.

This example consists of a Transfer Interface System with Model 500 Processors and their associated LTI Modules. The I/O Channels are wired to three drops. CPU racks are arbitrarily labeled A and B, and are wired to the appropriate terminals of the RTI's.

CPU (PROCESSOR) RACKS

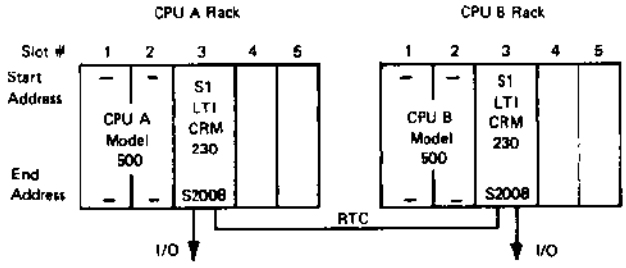


Figure 5.2 — CPU Rack Addressing

Figure 5.2 illustrates CPU rack addressing for this example of a Transfer Interface System.

CPU Rack:

SLOT 1 — The Model 500 has been assigned none of its 460 internal registers (since they cannot be transferred between processors).

SLOT 2 — The Model 500 physically takes up two register slots. Slot 2 does not require address assignments.

SLOT 3 — The starting address of the LTI module (CRM-230) is S1 (register 1). Although the LTI has 4096 registers available, its ending assignment is 2008 since this is all the Model 500 Processor can address.

SLOT 4, 5 — No modules reside in these slots — address assignments are not required.

Note that the start and end addresses of the system slots are shown. However, when programming address assignments, only ending addresses can be entered. After ending addresses are entered for a slot, the corresponding starting addresses will be automatically assigned beginning with the next available register. For a full explanation of the rack addressing programming procedure, refer to the CRT Programmer instruction bulletin.

NOTE: The CPU A and B rack address assignments *must* be identical for proper operation.

SYSTEM WITH 1 CHANNEL AND 1 DROP

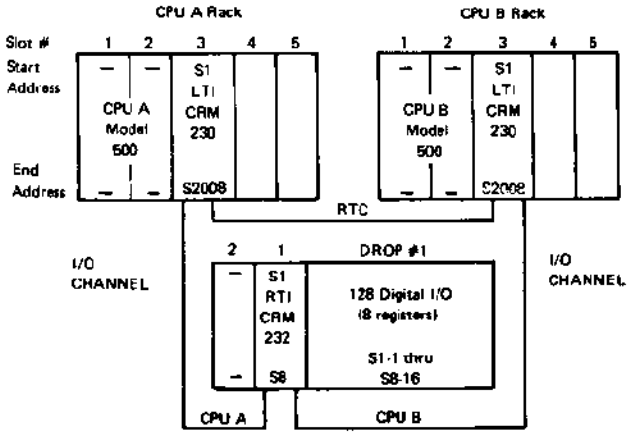


Figure 5.3 — Channel 1, Drop #1 Rack Addressing

Figure 5.3 illustrates rack addressing for the first drop of the I/O Channel (Channel 1, Drop #1). This drop is a rack assembly with 128 digital I/O points.

Channel 1, Drop #1:

SLOT 1 — To accommodate 128 digital I/O points, eight 16-bit registers are required (S1-1 thru S8-16).

SLOT 2 — No address assignments required.

Note that the addresses for digital I/O are always assigned to slot 1.

SYSTEM WITH 1 CHANNEL AND 2 DROPS

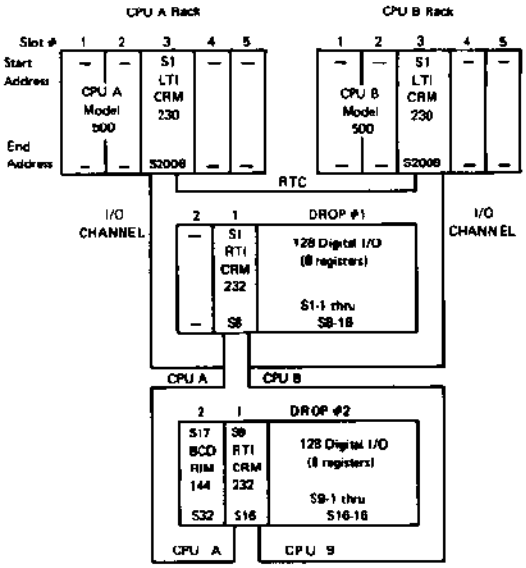


Figure 5.4 — Channel 1, Drop #2 Rack Addressing

Figure 5.4 illustrates rack addressing for the second drop of the I/O Channel (Channel 1, Drop #2). This second drop also has 128 digital I/O points but unlike Drop #1, it has a register module. The BCD input module resides in the register slot (slot 2), and requires 16 register addresses to be fully operational.

Channel 1, Drop #2:

SLOT 1 — Eight registers are assigned for the 128 digital I/O (S9-1 thru S16-16).

SLOT 2 — 16 registers are required for the BCD input register module (S17 thru S32).

The total requirement for this drop is 24 registers. Notice that the start address for drop #2 is one more than the ending address for drop #1. The first digital address for drop #2 is S9-1 and the last is S16-16. Therefore, slot 1 has an ending register address of S16. Slot 2 ends at S32, allowing for the required 16 registers needed by the BCD register input module.

SYSTEM WITH 1 CHANNEL AND 3 DROPS

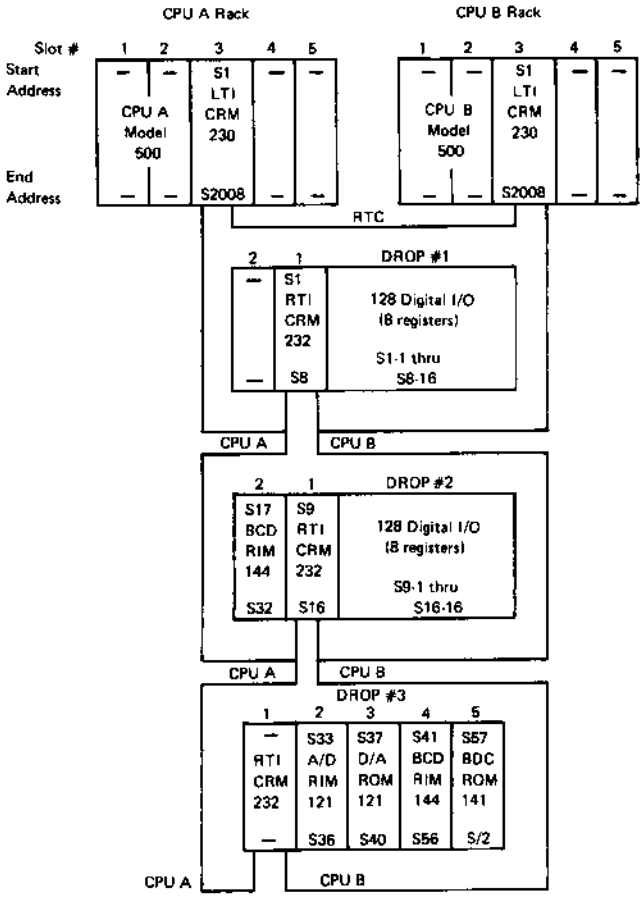


Figure 5.5 — Channel 1, Drop #3 Rack Addressing

Figure 5.5 illustrates rack addressing for the third drop on the I/O Channel (Channel 1, Drop #3). This drop is a rack assembly with register I/O.

Register requirements for register modules vary. As an example, a four-channel analog module requires four registers. A BCD I/O module can use up to 16 registers.

Channel 1, Drop #3:

SLOT 1 — No address assignments are required since there are no digital I/O points.

SLOT 2 — Four registers are assigned to a four channel analog input module (S33 thru S36).

SLOT 3 — Four registers are assigned to a four channel analog output module (S37 thru S40).

SLOT 4 — 16 registers are assigned to a BCD input module (S41 thru S56).

SLOT 5 — 16 registers are assigned to a BCD output module (S57 thru S72).

RTC (Channel 2, Drop #1):

Now that all external registers have been assigned, the Register Transfer Channel must be addressed. The *RTC requires four registers* be assigned for operation. These registers must be rack addressed for Channel 2, Drop #1.

Slot 1 — S73 to S76

The last external register assigned was S72. Therefore, the next four registers (S73 thru S76) are assigned to the RTC (Channel 2, Drop #1, Slot 1). The function of these registers is as follows:

S73 — Startup Transfer Register. See Section 5.4.2.
S74 — End-of-Scan Transfer Register. See Section 5.4.3.
S75 — Scan Synchronization Register. See Section 5.4.4.
S76 — Primary/Backup Read/Write Bit Exchange Register. See Section 5.4.5.

Internal Registers

In the example Transfer Interface System the last external register assigned was S72. The next 4 registers were allocated to the RTC channel and go on thru S2008. Defined internal registers would begin with S77. Since only the first 256 registers of a LTI module can be forced, it is recommended that internal relays be located at addresses S77 thru S256 since only these are forceable. Note that even though 256 registers are forceable, only 255 may be transmitted over external LTI communication channels.

NOTE: The user should plan ahead for any anticipated system expansion when assigning register addresses. See Section 5.3.7.

5.3.6 MULTIPLE LTI MODULES

If more drops or registers are required than those that can be supported by one pair of LTIs, additional pairs of LTI modules can be added.

An LTI module only provides storage register locations to a processor which can address them. The LTI module does not increase the CPU addressing range capability. See Section 5.3.1.

Each matched pair of LTI modules *must* have identical rack addressing and be connected together by their Register Transfer Channels.

The LTI control register assignments are dependent on the LTI modules' position. See Section 5.3.4 and Appendix B.

Refer to the example TIS presented in Section 5.3.5. If the system required more than the eight external I/O drops afforded by the single LTI pair, more matched pairs could be added as shown in Figure 5.6. Up to seven LTI modules can be supported by a Model 500 or 700 processor.

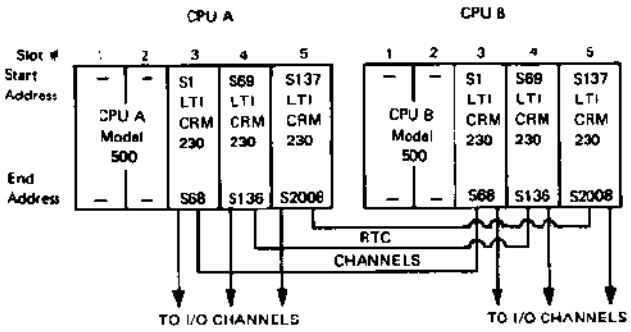


Figure 5.6 — Multiple LTI Rack Addressing

Figure 5.6 assumes that each matched pair of LTI modules supports eight I/O drops (with eight registers per drop). Note that the maximum address assignment continues to be S2008 since this is a limitation of the Model 500 Processor. Addresses are assigned as follows:

CPU Rack:

SLOT 1 — The Model 500 has been assigned none of its 460 internal registers.

SLOT 2 — Does not require address assignments.

SLOT 3 — Since the I/O Channel is assumed to have eight drops of eight registers each, this requires 64 registers. In addition, four registers are required for the RTC channel. Thus, the first 68 registers (S1 thru S68) are assigned to the LTI module in Slot 3.

SLOT 4 — This LTI module is identical to the previous one, therefore the next 68 registers (S69 thru S136) are assigned to this slot.

SLOT 5 — The remaining addressable registers (S137 thru S2008) are assigned. The arbitrary assignment of external registers would reside in S137 thru S200. Internal registers would reside in S205 thru S2008 (with the four RTC registers located at S201 thru S204).

Note that each matched pair of LTI modules have identical Rack Addressing Assignments and are connected together by their Register Transfer Channels (RTC's).

5.3.7 SYSTEM EXPANSION

Expansion can be accomplished by adding to an existing drop or adding an additional drop. When a TIS is expanded, the user must develop and enter the ladder logic program for the newly added I/O points. For the specific programming procedures, refer to the CRT Programmer Instruction Bulletin.

NOTE: When expanding a TIS, remember that the matched LTI pairs must have *identical* address assignments.

I/O Expansion Considerations

1. The addition I/O must fit within the processor addressing capability.
2. The additional I/O must be able to be supported by the existing LTI modules; if not, additional pairs of LTI modules will be required.
3. Expansion of an I/O drop requires that external registers are available for use at that location — either from previously allocated address assignments or the reallocation of registers for that location.
4. The addition of more registers on an I/O Channel will lengthen the LTI/RTI update time. However, if the registers were previously allocated to the I/O Channel, the LTI/RTI update time should not be significantly increased by additional drops.

The following is a brief description of the two basic expansion alternatives — drop expansion and drop addition.

Drop Expansion

Drop expansion by a mere addition of hardware alone can be accomplished if the previously entered rack addressing has allocated registers for it; otherwise, additional registers must be allocated for the drop. Therefore, the current system configuration and the defined rack addressing has to be reviewed when contemplating expansion of an existing TIS drop.

Drop hardware expansion can be accomplished by simply replacing the existing rack with a larger rack assembly or, in the case of a four-function digital I/O rack assembly, expander modules (Class 8030 Type CRM-115/116) may be used to add a second four-function digital I/O rack to the drop.

Drop Addition

Adding a drop to the I/O Channel can be done at any time provided the limitations of the processor or LTI are not exceeded. To add a drop, alteration of the existing rack addressing assignments and ladder program will most likely be necessary, unless previous address allocation allows for additional drops.

If expansion of a TIS is anticipated, plan ahead and assign internal relays and registers so they will not need to be reprogrammed when any additional drops are added. Recall the example of Section 5.3.5 (Internal Registers). If a fourth I/O drop was anticipated at a later date, it would be advisable to plan for this expansion by starting internal relays at an address location well beyond S77. For example, if internal relays are addressed starting with S129, then S73 thru S124 would remain available for I/O drop expansion.

NOTE: If more addresses are assigned to external drops, the RTC register addresses *must* be changed. In this example, they would have to be moved from S73-S76 to S125-S128.

WARNING

Care must be taken when altering existing rack addressing. Automatic shifting of addresses will occur from the point of alteration. Registers may end up being changed to locations which were not intended by the designed to be used as I/O points, thus possibly causing unexpected control action to occur.

Once hardware and software modifications are made, verify that they are correct before putting the system into RUN or DISABLE OUTPUTS.

For information on how to alter rack addressing assignments, refer to the CRT Programmer Instruction Bulletin.

When adding a drop or changing rack addressing for a specific I/O Channel, the LTI/RTI update time may be altered. Refer to Appendix A, LTI/RTI Update Time.

5.4 Register Transfer Channel

5.4.1 GENERAL DESCRIPTION

One of the functions of the LTI Register Transfer Channel is to ensure internal register values are identical in the Primary and Backup systems. The TIS uses two types of Register Transfer methods to maintain identical Primary and Backup systems. These two methods are the Startup Transfer and the End of Scan Transfer. Both methods occur over the RTC at 375K Baud to ensure fast updating.

Upon Backup system startup, a Startup Transfer occurs: internal registers (timers, counters, data, etc.) are transferred from the Primary to Backup LTI modules. See Section 5.4.2. This ensures the Primary and Backup system registers are identical, and must occur before a Backup can go into RUN and assume ready status. From this initial point of synchronization, the Primary and Backup systems read the same input conditions; thus internal registers will be updated simultaneously from this point on, provided the processors remain in synchronization with each other.

Although the Primary and Backup processor scans are synchronized (see Section 5.4.4), the crystal oscillators (that operate timers) are not synchronized. Therefore, it is possible that timers in the Primary and Backup processors may not be identical. Also, register values which are changed as a result of communication with external devices may differ. For critical applications where these differences cannot be tolerated, the user can enable an end of scan transfer: 32 registers can be transferred from Primary to Backup at the end of every scan. See Section 5.4.3.

Once the four RTC registers have been assigned through rack addressing, a number may be entered into them by any of the following methods:

1. DATA ENTER or DATA mode of a SY/MAX Programmer
2. SY/MAX Loader/Monitor
3. Communication from an External Device
4. Ladder Diagram Program (i.e., LET rungs)

Descriptions of each of the four registers follows.

5.4.2 STARTUP TRANSFER

The Startup Transfer Register is defined as the first register assigned to the Register Transfer Channel (Channel 2, Drop 1). The number that resides in this Startup Transfer Register will determine how many registers will be transferred from Primary to Backup LTI modules.

The value entered into the Startup Transfer Register should be the last (highest) register the user desires to be transferred when the Backup goes from a HALT-to-RUN transition. A value of zero (default) will cause all 4096 registers (defined and undefined) of the LTI to be transferred. Likewise, if the entered value is outside the LTI's defined address range, all 4096 registers will be transferred.

IMPORTANT: the Startup Transfer Register is cleared to zero every time the LTI is power-cycled. Thus, the only way to preserve the register value in the event of a power-cycle is via the ladder diagram program.

NOTE: To transfer only defined registers of the LTI, the Startup Transfer Register must contain a value equal to or less than the last internal register defined for the LTI in rack addressing (see the following Startup Transfer example).

Startup Transfer Example

Assume that address assignments are made to the TIS as in Section 5.3.5. For this example, defined registers for the LTI are as follows:

External Registers	S1 - S72
RTC Registers	S73 - S76
Internal Registers	S77 - S2008

Since the Startup Transfer Register is defined as the first register assigned to the RTC, we have:

Startup Transfer Register = S73

If S73 contains the default value 0 when the Backup system goes through a HALT-to-RUN transition, registers S1 through S4096 (all defined and undefined registers) will be transferred from Primary to Backup systems. Clearly, in this application this is excessive and unnecessary, since the system cannot even address registers beyond S2008.

The user can restrict the number of registers transferred to the Backup by changing the contents of S73. If we assume that only the first 1,000 registers need to be synchronized (even though 2,0008 are addressed), per the example ladder rung below, only registers S1 through S1000 will be transferred.

Note that by specifying the number of registers to be transferred to the Backup, the Startup Transfer Delay Time (described below) can be effectively reduced.

Startup Transfer Delay Time

The purpose of the Startup Transfer is to completely synchronize the Transfer Interface System. During the Startup Transfer, the Primary processor scan will be delayed for a short period of time to prevent register values from changing during the transfer. Therefore, the user must insure that the Backup processor is not placed into RUN during a critical Primary operation.

The number of milliseconds that the Primary system will be delayed is dependent on the number of external and internal registers that are transferred. This delay time can be approximated by the following formula:

External Registers x (.148)
\+ Internal Registers x (.111)
Startup Transfer Delay Time (ms)

A quick calculation will reveal a Primary scan delay for our rack addressing example of approximately 457 ms. for a default value in S73 of 0 (all 4,096 registers) vs. 114 ms. for a value of 1,000 (first 1,000 registers only).

5.4.3 END OF SCAN TRANSFER

The End of Scan (EOS) Transfer Register is defined as the second register assigned to the Register Transfer Channel (Channel 2, Drop 1). The number that resides in this End of Scan Transfer Register will determine the starting address of a block of 32 registers to be transferred from Primary to Backup LTI modules at the end of every processor scan.

To enable this transfer of registers, the EOS Transfer Register bit (bit 16 of the RTC Control Register — see Appendix B.4.3, LTI Control Registers) must be set ON (1) in the Backup system.

The total time required to transfer the 32 registers at the end of scan is approximately 4 ms. Since the processor has various housekeeping tasks to do at the end of scan, and some of these tasks take place in parallel with the End of Scan Transfer, the actual increase in processor scan time will be less than the 4 ms transfer time.

The user should enter into the End of Scan Transfer Register the address of the first register of a block of 32 registers to be transferred at the end of scan. Registers outside the LTI's defined address range will not be transferred. A value of zero (default) will result in no registers being transferred.

IMPORTANT: the EOS Transfer Register is cleared to zero every time the LTI is power-cycled. Thus, the only way to preserve the register value in the event of a power-cycle is via the ladder diagram program.

NOTE: Only registers defined to exist in the LTI modules may be transferred.

In order for the End of Scan Transfer to occur without disrupting the processor scan, a limit of 32 registers may be transferred. However, by ladder programming, the EOS Transfer Register can be manipulated in such a way that different blocks of 32 registers are transferred at the end of each scan, thus successfully transferring more than 32 registers. See the following EOS Transfer example.

EOS Transfer Register Bit

In order for the End of Scan Transfer to occur, the EOS TRANSFER REGISTERS bit (bit 16) must be set ON (1) in the RTC Control Register of the Backup LTI. See Appendix B.4.3, LTI Control Registers. When this bit is not set (cleared to zero) the End of Scan Transfer will not be enabled.

EOS Transfer Register Example

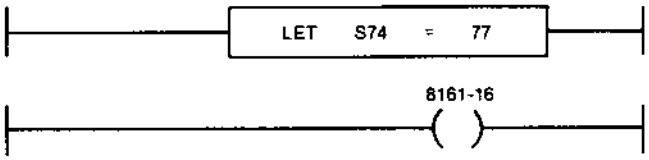
Assume that address assignments are made to the TIS as in Section 5.3.5. For this example, defined registers for the LTI are as follows:

External Registers	S1 - S72
RTC Registers	S73 - S76
Internal Registers	S77 - S2008

Since the End of Scan Transfer Register is defined as the second register assigned to the RTC, we have:

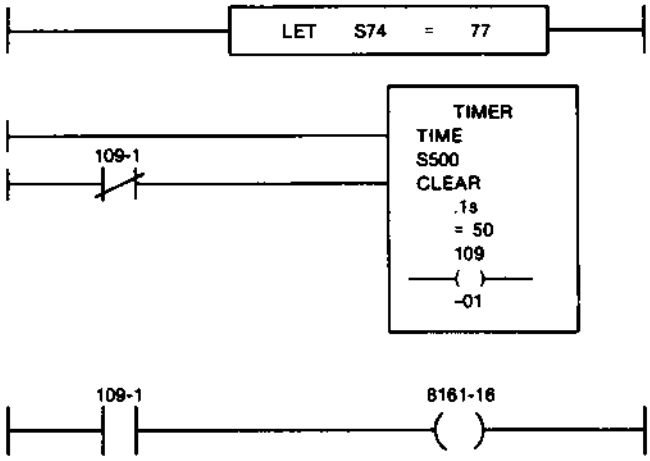
EOS Transfer Register = S74
EOS Transfer Registers Bit = S8161-16

Suppose the TIS has 32 critical timers that must be synchronized between Primary and Backup systems. Assuming that these timers reside in registers S77 through S108, we can transfer them from Primary to Backup at the end of every scan with the following rungs programmed in the Backup processor:



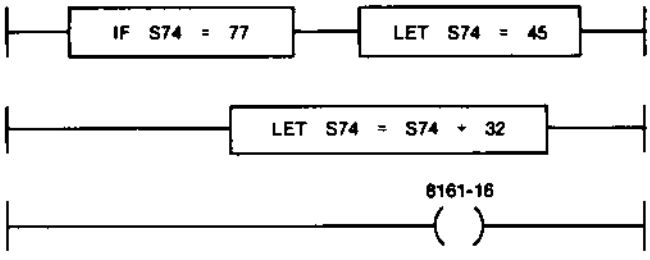
The first rung determines that a block of 32 registers, beginning with S77 (S77 through S108) will be transferred at the end of every scan. The second rung sets the EOS TRANSFER REGISTERS bit ON to enable the transfer.

Instead of transferring the registers at the end of every scan, we could instead selectively transfer them as a function of time as follows:



These rungs will enable the End of Scan Transfer of registers S77 through S108 once every five seconds. The EOS TRANSFER REGISTERS bit could just as easily be set according to some other control logic.

Suppose the TIS has 64 critical timers to be synchronized. Assume that thee timers reside in registers S77 through S140. Though we cannot transfer all 64 registers at one time, we can alternately transfer blocks of 32 registers every other scan. The following rungs perform this operation:



These rungs will enable the Primary to Backup transfer of registers S77 through S108 at the end of the first scan, and registers S109 through S140 at the end of the second scan. Thus, different blocks of 32 registers can be transferred alternately.

NOTE: To minimize the number of registers which have to be transferred over the RTC, keep all critical timers and counters in a *block of continuous registers*. Optimum performance can be obtained if a maximum of 32

registers are used, since the number of registers which can be transferred at the end of any one given scan is 32.

5.4.4 PROCESSOR SCAN SYNCHRONIZATION

To ensure the virtually bumpless transfer from a Primary to a Backup system, the processor scans are synchronized. Thereafter, both processors receive the same RTI input data simultaneously, and programmed rungs are solved identically. Without this synchronization, processor scans may not be identical due to independent processor scan times or different Primary or Backup programs.

Processor scans are synchronized via the Register Transfer Channels of the LTI modules. Through the RTC, the processor that finishes its scan first is delayed for a period of time to allow the lagging processor to complete its scan. After both scans have been completed, both processors will begin scanning simultaneously. This scan hold or delay time is programmable within limits.

While the rack addressing in both Primary and Backup must be identical, the ladder diagram programs do not, and the scan hold time is programmable to accommodate different program lengths within the Primary and Backup processors. However, since it is good programming practice to minimize the difference lengths between programs, program differences such as shutdown routines should be placed in subroutines that are only scanned when needed. See Appendix F.3, Different Primary/Backup Systems.

Modifying Scan Hold Time

The Scan Synchronization Register is defined as the third register assigned to the RTC (Channel 2, Drop 1). The number that resides in this Scan Sync Register will determine exactly how long a faster scanning processor will wait for the lagging processor before it resumes scanning.

The value in the Scan Sync Register can be modified from 5 to 500. This value will determine the number of milliseconds (ms) a faster scanning processor will be held for the lagging processor. If a number is not entered into the Scan Sync Register, the scan hold time will default to 100 ms (register default value of 0). An entered value outside the acceptable range will default to the closest limit (5 or 500). Entered values will round to the next 5 ms increment.

Loss of Synchronization

If the programmed scan hold or delay time has elapsed and the lagging processor has not yet completed its scan, the Backup processor will fall out of synchronization with the Primary. The Primary will continue scanning and controlling the I/O, but will not be able to perform an End of Scan Transfer until the Backup re-synchronizes with a Startup Transfer.

Should the Primary and Backup systems fall out of synchronization, the Backup processor will HALT unless the RTC FAILURE OVERRIDE bit (bit 13) of the RTC Control Register is set (see Appendix B.4.3, LTI Control Registers).

Bit 15 of the RTC Control Register, called the RE-SYNC bit, can be used to enable an unsynchronized Backup to request a Startup Transfer to re-synchronize with the Primary. If the Backup successfully re-synchronizes, it will attain a full ready Backup status. If the re-sync attempt is unsuccessful, the Backup will continue to try to re-synchronize as long as its RE-SYNC bit is set ON (1). See Appendix B.4.3. Note that if a fault should occur in the Primary while the Backup is trying to re-synchronize, a "bump transfer" will occur.

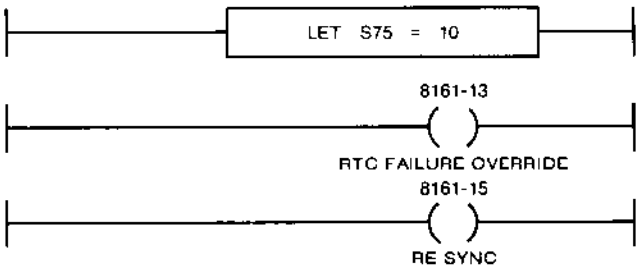
Assuming the TEST bit (bit 14) is cleared, by setting ON the RTC Failure Override bit (bit 13) and the Re-Sync bit (bit 15), the user will allow the Backup to temporarily fall out of sync (for the sake of preserving redundant control) but at the same time attempt to re-establish system synchronization.

NOTE: In deciding whether or not to set the Re-Sync bit, the user must be aware that each re-sync attempt with a Startup Transfer will delay the Primary system. See Section 5.4.2.

In order for the Primary and Backup systems to attempt to re-synchronize with a Startup Transfer, the following conditions must be true:

1. Backup TEST bit must be reset OFF (0).
2. Backup RTC FAILURE OVERRIDE bit must be set ON (1).
3. Backup RE-SYNC bit must be set ON (1).
4. Proper RTC communication must exist.

The following examples illustrate how to automatically re-synchronize systems. The examples assume address assignments as made in Section 5.3.5, whereby the Scan Sync register is defined as S75 (the third register assigned to the RTC).

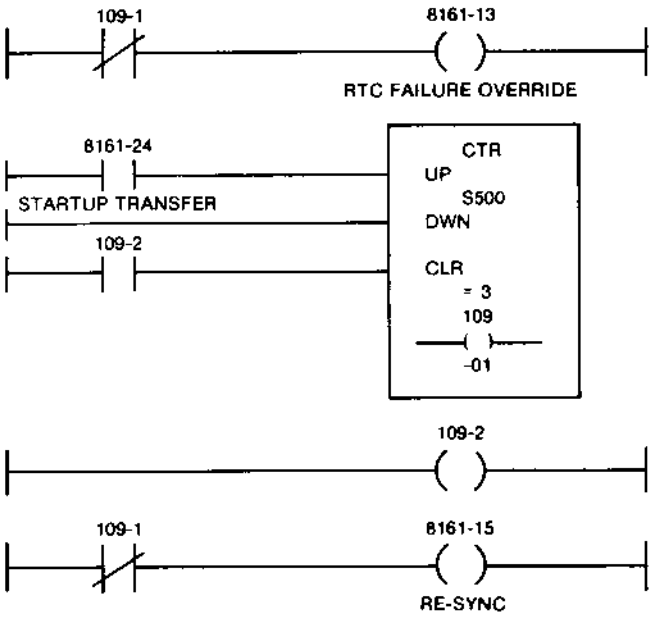


The first rung establishes that a faster scanning processor will wait 10 ms for a lagging processor. This rung should be programmed in both the Primary and Backup processors. If this rung were not programmed (and S75 = 0), the faster processor would wait 100 ms (default time) for the lagging processor.

The remaining two rungs set the RTC FAILURE OVERRIDE and RE-SYNC bits. Note that it is assumed the TEST bit (8161-14) is reset OFF (0). If the lagging processor doesn't reach the end of its scan within 10 ms of when the first processor does, a request for a "Startup Transfer" will be initiated in order to re-synchronize.

Note that the above rungs assume that only one LTI module resides in each processor rack. Additional LTI modules would require additional rungs to re-synchronize the entire system (i.e., RTC Failure Override and Re-Sync coils would be 8158-13 and 8158-15 respectively for the second LTI, etc.). For multiple LTI systems, all LTI's will perform a Startup Transfer whenever any one LTI requests it.

Considering some of the potentially adverse effects on the scan time of the Primary which can result from continuously enabling Startup Transfers, the next example illustrates rungs which can be used to allow the Backup to attempt to re-synchronize no more than three times before halting.



The logic keeps track of the number of Startup Transfer requests executed by monitoring S8161-24. After the third attempt, RTC FAILURE OVERRIDE and RE-SYNC are disabled; consequently the Backup will now shut down in the event synchronization is lost.

NOTE: For multiple LTI systems, the STARTUP TRANSFER bits for *all* of the LTI's should be run in parallel to one internal coil, since only the LTI that is initiating the Startup Transfer will set its bit.

Control Register bits can also be used to enable a Primary processor to prevent a Backup from initiating a Startup Transfer. See Appendix F.2, Primary/Backup Bit Exchange.

5.4.5 PRIMARY/BACKUP READ/WRITE BIT EXCHANGE

In the fourth register assigned to the Register Transfer Channel (S76 in the example of Section 5.3.5), eight bit locations are used in order for the Primary and Backup processors to write bits to each other at the end of every scan. These bits are transferred back and forth as long as the Primary and Backup are both synchronized. The bits are transferred over the RTC; thus if the RTC connection is broken, the bits will no longer be updated.

These bits can be used for user-controlled interaction between the Primary and Backup processors. See Appendix F.2, Primary/Backup Bit Exchange, for programming examples.

6.0 SYSTEM START-UP

6.1 Preliminary Considerations

This section is intended to be an independent step-by-step guide to help the user get the Transfer Interface System (TIS) up and running with a minimum of complications. To this end, we recommend that the user first become familiar with the TIS by reading other sections of this bulletin, in particular Sections 3, 4, 5, and Appendix B.

Before applying power to the TIS the following precautions must be taken:

1. Check to see that the system is installed as described in Section 4 (Installation). In particular, insure that:
   a) the DIP switches are set correctly (Section 4.4)
   b) the RTC and I/O channels are wired correctly (Section 4.6.3).
2. Check to see that all field wiring is correct.
3. Insure that both processors have their keyswitches in the HALT position.
4. Ensure that all RTI racks in the system are always powered up prior to the CPU racks.

6.2 Rack Addressing And Programming

After observing the above considerations — in particular that both processors are keyswitched to HALT — the user can now apply power to the TIS. At this stage the user does not need to be overly concerned with the status of the LED indicators; however both processor HALT indicators should be flashing ON and the HALT indicator of the RTIs should be ON steady.

The user can now enter "rack addressing" and the ladder program for the TIS (see Section 5.3, Rack Addessing, for a detailed example of "rack addressing"). It is recommended to perform a CLEAR ALL to memory prior to entering "rack addressing" and the ladder program. It is also recommended, in order to expedite the initialization process, to just enter a simple ladder program at this point. Later on, once the TIS is up and running and proper hardware operation has been verified, a comprehensive program can be entered.

CAUTION

In order to promote user familiarity and avoid complications in Startup, the user should not set ON any control register bits at this point — either via the DATA mode or the ladder program.

Once "rack addressing" and the ladder program have been entered into *both* processors (same "rack addressing" for both), power down both processors in preparation for the succeeding steps below. DO NOT at this point put the processors in RUN.

6.3 Power Up Sequence

Now that the processors have "rack addressing" and ladder programs loaded into them, the Power Up Sequence can be initiated. The user is advised to perform the power up sequence as described below, to insure correct initialization of the TIS. Along with insuring correct initialization this sequence will determine the Primary/Backup status of the system. See Appendix C.

In the following sequence the user will power up the processors separately and check them out by observing the status of the LED indicators, and then put both processors in operation for redundant control.

NOTICE

When initially keyswitching a CPU that has a new "out of the box" LTI installed to DISABLE OUTPUTS or RUN, the processor will remain in HALT and the LTI will indicate a MODULE ERROR. The processor error register (8175) will identify the LTI in error, and the LTI error register will contain error code 901. This is a normal occurrence, reflecting the fact that the LTI storage registers are corrupt (contain random data). Keyswitching the CPU from HALT to DISABLE OUTPUTS or RUN a second (or third) time will clear the error.

Proceed with the Power Up Sequence:

1. With both processors powered down, now power up the processor that will be designated Backup, and keyswitch it to DIABLE OUTPUTS. Verify by the status of the LED indicators, shown in Figure 6.1, that the unit is operating correctly. Note that when switching processors from one state to another the LED indicators will momentarily change states before stabilizing.

   If an LED display other than indicated in Figure 6.1 occurs, refer to the above NOTICE. If trouble persists, refer to the troubleshooting Section 6.4.

2. Once the unit is operating correctly in DISABLE OUTPUTS, the unit can be further verified to be operating correctly by keyswitching it to RUN. Be reminded that when the processor is in RUN, it controls external I/O via the ladder program. The correct LED indication when the unit is in RUN is shown in Figure 6.2.

PROCESSOR	LTIs	RTIs
RUN -- flashing	RUN — ON PRIMARY — ON RTC ERROR -- ON	RUN — flashing HALT — flashing CHNL ERROR — flashing CPU A or B — ON

Figure 6.1 DISABLE OUTPUTS LED Display

PROCESSOR	LTIs	RTIs
RUN — ON	RUN -- ON PRIMARY — ON RTC ERROR — ON	RUN — ON HALT — OFF CHNL ERROR -- flashing CPU A or B — ON

Figure 6.2 RUN LED Display

3. Once the unit designated to be Backup is operating properly, *power it down* in preparation for the succeeding steps.

4. With the processor designated to be Backup powered down, apply power to the processor to be designated Primary, then keyswitch it to DISABLE OUTPUTS. As before, verify by the status of the LED indicators, shown in Figure 6.1, that the unit is operating correctly.

   If an LED display other than indicated in Figure 6.1 occurs, refer to the NOTICE above. If trouble persists, refer to the Troubleshooting Section 6.4.

5. Once the unit is operating correctly in DISABLE OUTPUTS, keyswitch it to RUN and verify by the status of the LED indicators, shown in Figure 6.2, that the unit is operating correctly.

6. After the processor designated to be the Primary is operating correctly in RUN, leave it *powered up* and in RUN in preparation for the following steps.

7. With the Primary in RUN (for at least 10 seconds), apply power to the Backup and keyswitch it to RUN. If the Register Transfer Channel communication link is connected and operating correctly, the "RTC ERROR" LED on the Primary will turn OFF and the Backup will initialize and go into RUN. If the TIS is operating correctly there should be no ERROR indicators illuminated at this time; on the RTIs, CPU A or B will be ON steady with the complement CPU A or B flashing.

8. Now that the Transfer Interface System is up and running, a more comprehensive ladder program can be entered and appropriate control bits set to adapt the TIS to the particular user application.

6.4 Troubleshooting

In the Power-Up Sequence the user verifies correct operation of the TIS by observing the status of the LED indicators. If the LED indications are not as illustrated in the Power-Up Sequence, the user is advised to refer to Section 3.1 (LED Indicators) and to Appendix E (Error Codes) for help.

It should be noted that the illustrated LED indications for the power-up sequence assume "rack addressing" matches existing external I/O.

Some typical causes for the LED indications to be different than as illustrated in the Power-Up Sequence are described below:

1. When initially keyswitching a CPU that has a new "out of the box" LTI installed to DISABLE OUTPUTS or RUN, the processor will remain in HALT and the LTI will indicate a MODULE ERROR. The processor error register (8175) will identify the LTI in error, and the LTI error register (S8163 if the first LTI) will contain error code 901. This is a normal occurrence, reflecting the fact that the LTI storage registers are corrupt (contain random data). Keyswitching the CPU from HALT to DISABLE OUTPUTS or RUN a second (or third) time will clear the error.

2. The I/O LED indicator on the processor will illuminate if "rack addressing" includes drops that don't actually exist, are not wired, or are not communicating for some reason. Also, on the affected LTIs the HALT, CHNL ERROR, and MODULE ERROR indicators will be ON. Interrogation of the error codes (Appendix E) will reveal the drop in error.

3. The RTI HALT and CHNL ERROR LED indicators will remain ON steady — regardless of the keyswitch position of the processor — if the RTI is not communicating with the LTI (e.g., RTI not wired).

4. The RTI HALT, CHNL ERROR, and CPU A (or B) LED indicators will remain ON steady — regardless of the keyswitch position of the processor — if the RTI drop number is incorrect (e.g., RTI DIP switch setting does not match an existing drop in "rack addressing").

5. Bear in mind that, since these modules annunciate system errors that may actually originate in another module, error LEDs on the LTI or RTI themselves do not necessarily indicate a failure in these modules. If beset by erratic and seemingly contradictory indications, we suggest following a pattern which includes power-cycling all remote and CPU racks with the CPU keyswitch in HALT. This should be followed by turning each of the CPUs to RUN, accompanied by the user recording error code information as described in Appendix E. Useful information is contained in Register 8175 as well as the apropriate LTI error registers (S8163, S8160, etc.). Registers 8183 and 8184 may also contain relevant information, depending on the nature of the failure. The procedures of Appendix E can then be followed to help narrow down the source of the problem.

APPENDIX A — LTI/RTI UPDATE TIME

A.1 General Information

This appendix provides equations for calculating the LTI/RTI update time. Update time refers to the time required to pass information in either direction between the LTI image table and the RTI image table and should not be confused with throughput time. Throughput time, often called system response time, is the time elapsed from the actuation of an input device to the occurrence of an output action. Throughput time must also include I/O module response time and CPU scan time. Further information regarding throughput (overall system response) is covered in the Planning and Installation Guide Instruction Bulletin #30598-175-XX.

A.2 Drop Update Time

One of two equations are used to calculate drop update time. For the purpose of these equations, drops will be put into two categories, digital and register. The digital drop is a pure digital drop (8 or less registers) with no register modules. The register drop contains register modules or a combination of register and digital I/O modules.

A.3 Update Time Equation Variables

D = Total digital drops on the channel. (0-8)
R = Total register drops (or digital/register drops) on the channel. (0-8)
DR = Total register addresses assigned to all digital drops. (0-64)
RR = Total register addresses assigned to all register drops. (0-255)
X = Register addresses assigned to the drop being evaluated. (1-8). If more than 8 registers are assigned, use X = 8.

A.4 Drop Update Time Equations

Digital Drop Update Time (ms) =
$2.31\ D + DR + X + 0.79$

Register Drop Update Time (ms) =
$2.31\ D + DR + 3.15R + 1.24(RR + X) + 1.52$

Actual performance times may be better than calculated for channels with many registers due to improved message efficiency.

APPENDIX B — LTI CONTROL REGISTERS

B.1 General Information

Control registers 8001 through 8163 (contained in the processor) are used to monitor, and in some cases, control the Transfer Interface System (TIS). These registers reflect the condition of the TIS and contain information about registers and I/O modules.

The 8030 CRM-230 Local Transfer Interface (LTI) is a two channel module which utilizes three registers to communicate directly with the processor (CPU). The first register is an error code register. The second is a control register for channel 1 (I/O Channel). The third is a control register for channel 2 (Register Transfer Channel-RTC). The number of control registers used to monitor a particular TIS is based on the number of LTI modules in the system. Each matched pair of LTI modules uses three control registers.

Each register consists of two parts, a DATA field and a STATUS field. The DATA field can be programmed by the user for control functions. The STATUS field, as the name implies, is used just to monitor status of specific system conditions.

B.2 Register Allocation

The first matched pair of LTI modules in a Transfer Interface System have register S8163 designated as their error code register. The I/O Channel (channel 1) control register is S8162. The RTC (channel 2) control register is S8161.

Figure B.1 lists the error code, I/O Channel, and RTC control registers for Transfer Interface Systems using up to seven matched-pair LTI modules.

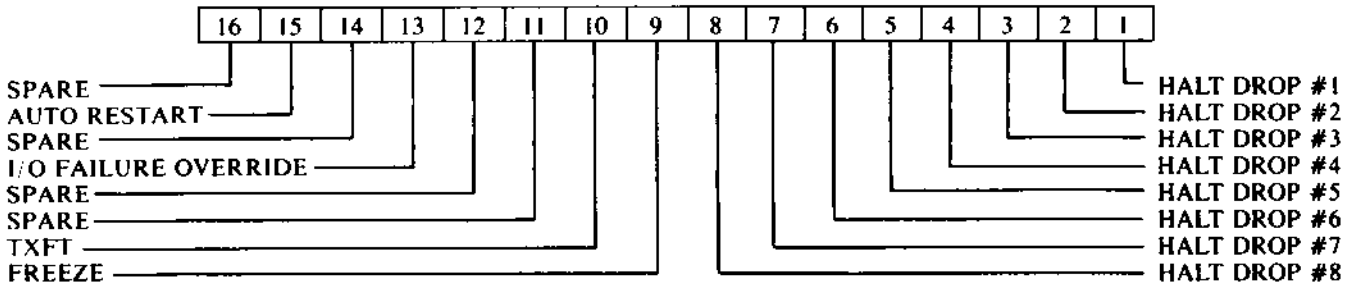
The contents of the error code registers are discussed in greater detail in Appendix E, Error Codes. The contents and format for the channel control registers follows.

Register	LTI	Location	Function
S8163	First	(Right of CPU)	Error Code
S8162	First		I/O Channel (1) Control Data & Status
S8161	First		RTC Channel (2) Control Data & Status
S8160	Second	(Right of first LTI	Error Code
S8159	Second	module)	I/O Channel (1) Control Data & Status
S8158	Second		RTC Channel (2) Control Data & Status
S8157	Third	(Right of second LTI	Error Code
S8156	Third	module)	I/O Channel (1) Control Data & Status
S8155	Third		RTC Channel (2) Control Data & Status
S8154	Fourth	(Right of third LTI	Error Code
S8153	Fourth	module)	I/O Channel (1) Control Data & Status
S8152	Fourth		RTC Channel (2) Control Data & Status
S8151	Fifth	(Right of fourth LTI	Error Code
S8150	Fifth	module)	I/O Channel (1) Control Data & Status
S8149	Fifth		RTC Channel (2) Control Data & Status
S8148	Sixth	(Right of fifth LTI	Error Code
S8147	Sixth	module)	I/O Channel (1) Control Data & Status
S8146	Sixth		RTC Channel (2) Control Data & Status
S8145	Seventh	(Right of sixth LTI	Error Code
S8144	Seventh	module)	I/O Channel (1) Control Data & Status
S8143	Seventh		RTC Channel (2) Control Data & Status

Figure B.1 — LTI Control Register Assignments

B.3 LTI Control Register — I/O Channel

B.3.1 I/O CHANNEL DATA FIELD

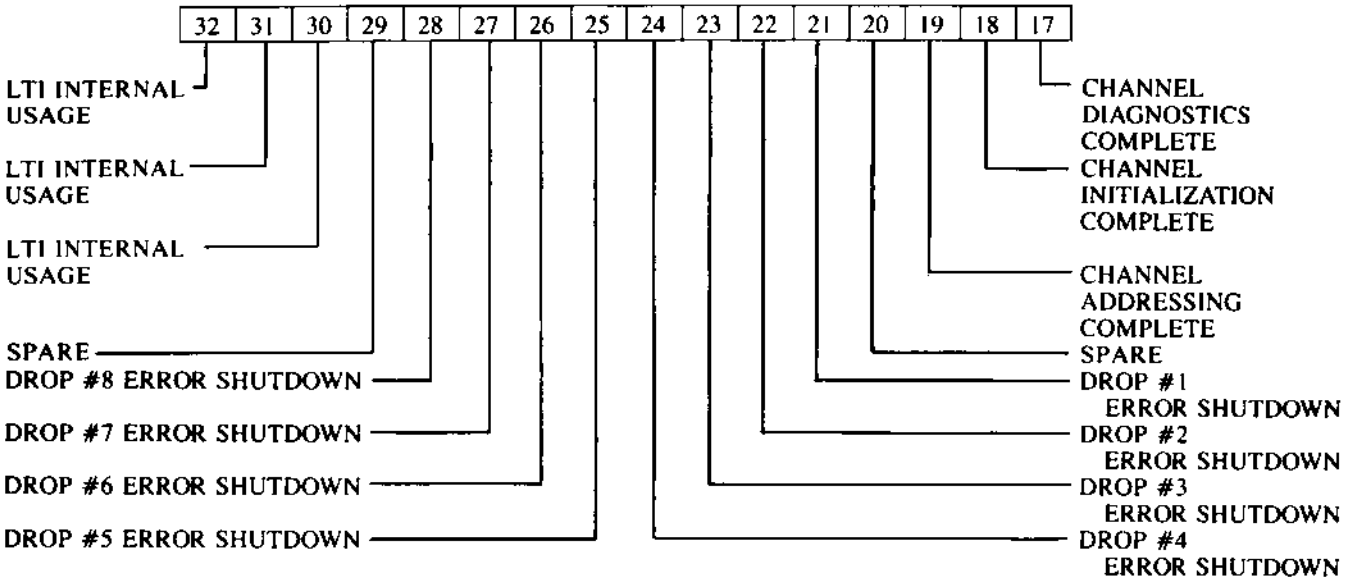


I/O Channel — Data Field

Control Register Bit	Name	Description
1 2 3 4 5 6 7 8	Halt Drop #1 Halt Drop #2 Halt Drop #3 Halt Drop #4 Halt Drop #5 Halt Drop #6 Halt Drop #7 Halt Drop #8	When OFF (0) the drop will operate as the ladder program indicates. When ON (1) the drop will be shut down. 1. Input status still valid. 2. Outputs turn OFF. 3. Register I/O clear (depending upon module type). 4. A drop shutdown under Primary control will not cause a transfer from Primary to Backup.
9	FREEZE	When ON (1) and a loss of transmission, transmission error, or CPU rack error occurs, all outputs are maintained in their last state. This bit is ignored in a Primary LTI if a running Backup is able to take control.
10	TXFT (Transmission Fault Tolerance)	Transmission Fault Tolerance determines whether three or ten consecutive transmission errors are allowed to occur before a channel error is acknowledged and an attempt is made to transfer to Backup. OFF (0) = Three errors ON (1) = Ten errors
11	Spare	
12	Spare	
13	I/O FAILURE OVERRIDE	When OFF (0) and drop error occurs, I/O channel will shut down and processor will HALT. When ON (1), and — Backup is ready: TIS will switch control to the backup rather than run with the channel in error (thus ignoring the I/O Failure Override bit). Backup is not ready: Allows the I/O channel to continue operating if a drop error occurs.
14	Spare	
15	AUTO RESTART	When ON (1) allows the I/O Channel to attempt to reestablish valid communications with any drop shut down due to transmission errors (bit 13 must be set to enable bit 15 to be recognized). This control bit performs the same function as the RESTART button on the primary LTI module. This bit is only active in a Primary system with no Backup; otherwise control will be switched to the ready Backup.
16	Spare	

Figure B.2 — LTI I/O Channel Control Register Data Field

B.3.2 I/O CHANNEL STATUS FIELD



I/O Channel — Status Field

Control Register Bit	Name	Description
17	Channel Diagnostics Complete	When ON (1) LTI Channel has completed its diagnostics.
18	Channel Initialization Complete	When ON (1) 1. RTIs have completed their diagnostics. 2. Valid LTI/RTI communication. 3. Image table updating sequence complete.
19	Channel Addressing Complete	When ON (1), indicates the CPU has loaded valid rack addressing information into the LTI.
20	Spare	
21 22 23 24 25 26 27 28	Drop #1 Error Shutdown Drop #2 Error Shutdown Drop #3 Error Shutdown Drop #4 Error Shutdown Drop #5 Error Shutdown Drop #6 Error Shutdown Drop #7 Error Shutdown Drop #8 Error Shutdown	If drop has been rack addressed: When OFF (0) drop is operating. When ON (1) drop is shut down due to error. If drop has NOT been rack addressed: When OFF (0) no drop exists. When ON (1) drop exists without addressing.
29	Spare	
30	Internal Usage	
31	Internal Usage	
32	Internal Usage	

Figure B.3 — LTI I/O Channel Control Register Status Field

B.3.3 DETAILED DESCRIPTION OF LTI I/O CHANNEL CONTROL BITS

The LTI I/O Channel control register, bits 1-16, are initially reset OFF (0) when the LTI is installed. Once altered by programming equipment, data entry, or by the ladder program, these bits will retain their state until altered again.

HALT DROP Bits (1-8)

Any drop on an I/O Channel may be programmed to halt (turn OFF all of its associated outputs). This is done by setting its LTI HALT DROP bit ON (1). A drop programmed to halt will have valid updated input status contained within the LTI image table. (Since this halt condition is generated by the user, no error lights are turned on, no transfer takes place, and the CPU will remain in RUN.)

FREEZE Bit (9)

The FREEZE bit is ignored in a Primary LTI if a running Backup is able to take control. Assuming the Backup is halted, the FREEZE bit functions as follows.

When the FREEZE bit (bit 9) is set ON (1), all outputs on the I/O Channel will retain their last state, ON or OFF, in the event of any of the following conditions:

1. A Communication error at a drop (e.g., broken cable).
2. The CPU HALT bit (S8176-1) is set ON (1). (i.e., CPU error or programmed halt.)
3. Power is lost at the local (CPU) rack.

Although the FREEZE bit may be set ON (1), the operation of the FREEZE function depends upon the detected error. In the following cases, the DROPS WILL NOT BE FROZEN, but reset OFF (0), *regardless* of the state of the FREEZE bit:

1. Drop with internal error. (i.e., power loss, faulty RTI, read-after-write or bus error.)
2. CPU turned into HALT via keyswitch or setting the CPU HALT/RUN bit, S8716-3.

NOTE: The CPU must not have been halted by an error prior to these actions. If the CPU is halted due to an error, turning the keyswitch to HALT will not reset frozen drops.

Turning OFF Frozen Drops

1. Power cycling a drop with frozen outputs will reset (OFF) all the outputs, regardless of the state of the processor.
2. When valid communication exist, setting a Primary CPU HALT bit (S8176-3) ON (1) will result in turning OFF frozen outputs.

Restarting Frozen Drops

1. Place the CPU in either RUN or DISABLE OUTPUTS, by either turning the CPU keyswitch or clearing the CPU HALT bit (S8176-3), will allow all drops with valid communications to restart in accordance with the user program.
2. Power cycling the CPU when it is in either RUN or DISABLE OUTPUTS will restart frozen drops.
3. If the CPU is still running (because the I/O FAILURE OVERRIDE bit was ON (1)), then turning on the AUTO RESTART bit (bit 15) will restart the frozen drop(s) if valid communications now exist between the CPU and drop(s).
4. Pushing the RESTART button on the LTI (assuming CPU and communications are fully operational and LTI I/O FAILURE OVERRIDE bit is set ON (1)) will also restart frozen drops.

TRANSMISSION FAULT TOLERANCE Bit — TXFT (10)

If LTI to RTI communication is disrupted (in environments with extreme noise for example), the TIS will attempt to establish a valid data transmission three times before acknowledging a communication error and attempting to switch control to the Backup system. Should a communication error be acknowledged in a Primary without a ready Backup, the TIS will take action according to the status of the I/O FAILURE OVERRIDE bit (bit 13).

Transmission Error Detection

Two types of data transmission error detection methods are used in the LTI/RTI communication link. The first detection method counts the number of times a specific block of data is determined to be invalid. The second method counts the number of consecutive blocks of data which are determined to be invalid. The cumulative values for each type of transmission error are kept internally by the LTI and RTI modules. When a good transmission occurs on a communication channel, the respective transmission error counters are reset to zero.

The user has the option of increasing the transmission fault tolerance level from three to ten transmission errors. This is done by setting the Transmission Fault Tolerance bit ON (1). Be aware that setting the number of transmission errors to ten will require additional time for the system to recognize a transmission error and either attempt a transfer from Primary to Backup or shut down a Primary that does not have a ready Backup.

Note that the transmission fault tolerance bit only affects the operation of the system when invalid data is detected. Another type of error — communication loss — is detected by internal timers in the system. A pause in communication of greater than 3 ms will cause an error to be generated. Therefore, if there is a complete loss of transmission due to cable damage or hardware malfunctions, the TIS will attempt to transfer control from a Primary to Backup almost immediately.

When the LTI acknowledges excessive transmission errors (more than the TXFT) the TIS will switch control from Primary to Backup. Should the Backup not be able to take control, the system will shut down unless the I/O FAILURE OVERRIDE bit (bit 13) is set ON (1).

I/O FAILURE OVERRIDE (Bit 13)

The purpose of the I/O FAILURE OVERRIDE bit is to allow portions of the TIS to continue operating in the presence of an I/O error. The actual response of the system depends on two major factors — the type of I/O error involved and whether there is a ready Backup available.

There are 4 major types of I/O errors —

1. Distorted communications (typically caused by noise).
2. Complete loss of transmission (usually caused by hardware failure or cable problem.)
3. Power Loss at remote drop.
4. Remote drop bus error.

The system responds in the same manner for the first 3 types of errors. For remote drop bus errors, the response is different.

System Response With A Ready Backup

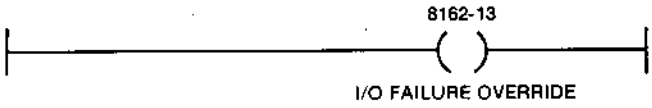
If there is a Backup "online" (i.e., one that is in full run and able to take control) and the Primary detects one of the first 3 types of I/O errors, the system transfers control to the Backup unit *regardless* of the setting of the Primary's I/O FAILURE OVERRIDE Bit. The former Primary then goes into HALT with an I/O error. If the error remains, the new Primary will continue to run or go into HALT in accordance with the condition of its I/O Failure Override bit.

If, however, the I/O error is a remote drop bus error, the system responds differently. In that case, a transfer is *not* made. Instead, the Backup goes to HALT with an I/O error *regardless* of the setting of its I/O FAILURE OVERRIDE Bit. The original Primary then either continues to run if *its* I/O FAILURE OVERRIDE Bit is set (1) or it will also go to HALT with an I/O error if the bit is cleared (0). The system responds differently to remote bus errors because they represent a more serious failure of the remote I/O. Transferring control to the Backup could cause unpredictable I/O operation, so the Backup is forced to HALT.

System Response When Backup Is Not Ready

A Backup may not be "ready" for a number of reasons. Its power may be off, it may have been manually keyswitched to HALT, its TEST bit may be set, or it may be in HALT because of some error. Whenever the Backup is not ready to take over, the Primary responds to all four types of I/O errors in the same manner. If its I/O FAILURE OVERRIDE Bit is cleared (0) when an I/O error is detected, the processor will go to HALT with an I/O error. If the bit is set ON (1), the drop in error will shut down, but the CPU will continue to RUN and allow the rest of the I/O channels to continue operating.

The I/O FAILURE OVERRIDE bit for the first LTI can be set on (1) with the following rung programmed in the ladder program.



If I/O FAILURE OVERRIDE is desired, this rung must be programmed as the first rung in the ladder program. An exception to this rule is if the timed interrupt or any other feature which requires programming the special TLET S8165 rung is used. For this exception, the I/O FAILURE OVERRIDE bit should be set by the very next rung. If multiple I/O FAILURE OVERRIDE bits need to be set via the ladder program, their corresponding rungs should be first in the program or immediately follow the special TLET S8165 rung.

CAUTION

Care must be taken whenever the I/O FAILURE OVERRIDE bit is set ON (1), because the system will continue to operate when drop errors occur. However, with the I/O Failure Override bit set, it is also possible to selectively halt drops through ladder programming by setting ON (1) individual HALT DROP bits.

NOTE: The I/O FAILURE OVERRIDE bit, which controls the operation of the I/O Channel, should not be confused with the RTC FAILURE OVERRIDE bit described in Section B.4.3.

AUTO RESTART Bit(15)

If a drop has been shut down due to a transmission error, setting the AUTO RESTART bit (bit 15) ON (1) will allow the LTI to automatically attempt to reestablish valid communication to that drop (provided the processor is operating in RUN or DISABLE OUTPUTS mode). In order to keep the processor running under error conditions, the I/O FAILURE OVERRIDE bit (bit 13) must be ON (1).

The AUTO RESTART bit enables the system to recover from a transmission error without pushing the RESTART button. This bit acts in the same manner as does the RESTART button on the front of the respective LTI module with one exception — drops with remote bus errors (which have subsequently been cleared) can be restarted with the Restart pushbutton but not with the Auto Restart bit. For more information on the RESTART button, see Section 3.3.

NOTE: The AUTO RESTART bit is only active in single processor control (Primary without Backup); otherwise, control will be switched to the Backup before a restart is attempted by the Primary.

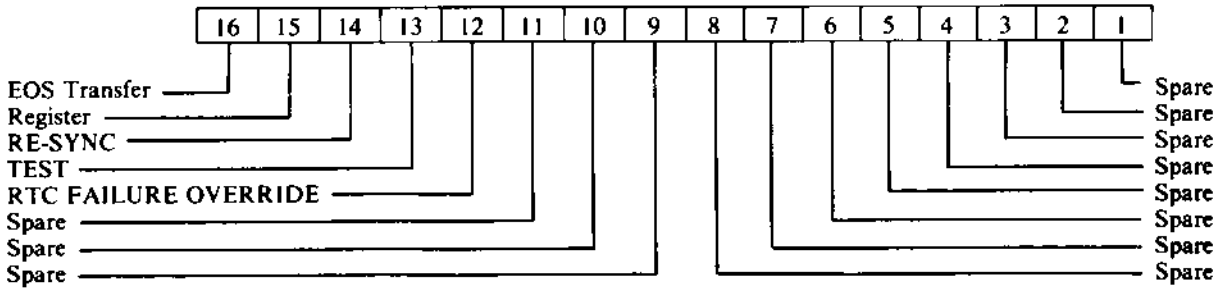
DROP ERROR SHUTDOWN Bits (21-28)

DROP ERROR SHUTDOWN bits are used for diagnostic purposes. They are turned ON (1) when their respective drops shut down. When used in conjunction with having the I/O Failure Override bit set ON (1), these bits can be extremely useful in implementing ladder control programs to effect user defined control functions — such as selective shut downs of the individual drops, as opposed to having all drops shut down.

NOTE: The DROP ERROR SHUTDOWN bit will be displayed as ON (1) for a drop that is present but not defined in the rack addressing. The drop error bit of an undefined drop bening ON (1) will not affect the shutdown operation of the TIS.

B.4 LTI Control Register — Register Transfer Channel

B.4.1 RTC DATA FIELD

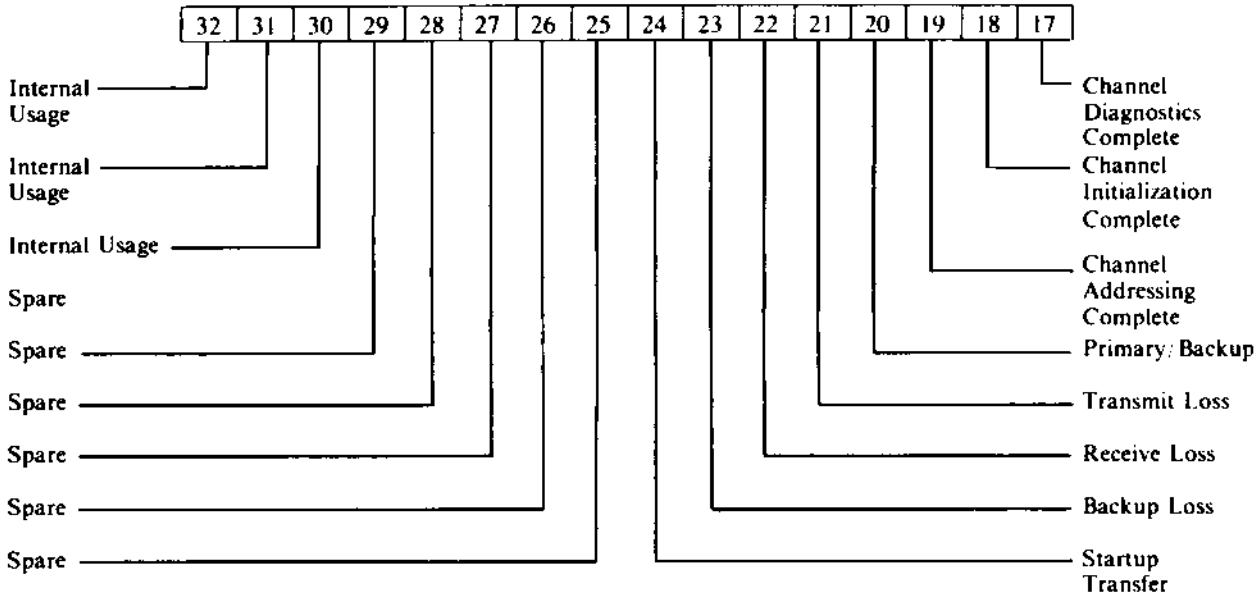


RTC Data Field

Control Register Bit	Name	Description
1 2 3 4 5 6 7 8	Spare Spare Spare Spare Spare Spare Spare Spare	
9	Spare	
10	Spare	
11	Spare	
12	Spare	
13	RTC FAILURE OVERRIDE	When set ON (1) in a Backup LTI, will allow Backup processor to continue to RUN despite losing synchronization with the Primary. This bit is active only in the Backup LTI.
14	TEST	When set ON (1) in a Backup LTI, the LTI (upon a HALT to RUN transition) will *not* request a Startup Transfer from the Primary processor.
15	RE-SYNC	When set ON (1) in a Backup LTI that is in RUN, the Backup system will attempt a Startup Transfer to re-synchronize the TIS. To enable the RE-SYNC bit, the RTC FAILURE OVERRIDE bit must also be set ON (1) and the TEST bit must be reset OFF (0).
16	EOS TRANSFER	When set ON (1) in a Backup LTI that is in RUN, the Backup LTI will request an End of Scan Transfer of 32 registers. The block of 32 registers to be transferred is determined by the value residing in the End of Scan Transfer Register (second register assigned to the RTC).

Figure B.4 — RTC Control Register Data Field

B.4.2 RTC STATUS FIELD



RTC Remote Transfer Channel Status

Control Register Bit	Name	Description
17	Channel Diagnostics Complete	Set ON (1) when LTI self-test is successfully completed. Reset OFF (0) when self-tests are in progress.
18	Channel Initialization Complete	Set ON (1) when LTI is in RUN with a verified address map and I/O channel is initialized.
19	Addressing Complete	Set ON (1) when address map has been loaded and verified.
20	Primary/ Backup	Set ON (1) when LTI is Primary. Set OFF (0) when LTI is Backup.
21	Transmit Loss	Set ON (1) when matched LTI has its RECEIVE LOSS bit set.
22	Receive Loss	Set ON (1) when LTI has not received communication from its matched pair.
23	Backup Loss	Set ON (1) in Primary LTIs that do not have a Backup that can become Primary. Reset OFF (0) when a Backup in full RUN is present. Backup LTIs will also set their BACKUP LOSS bit when they are unable to become Primary.
24	Startup Transfer	Set ON (1) one scan before a Primary does a Startup Transfer. Reset OFF (0) upon completion of the Startup Transfer.
25	Spare	
26	Spare	
27	Spare	
28	Spare	
29	Spare	
30	Internal Usage	
31	Internal Usage	
32	Internal Usage	

Figure B.5 — RTC Control Register Status Field

B.4.3 DETAILED DESCRIPTION OF LTI RTC CONTROL BITS

The LTI RTC control register data bits, bits 1-16, are initially reset OFF (0) when the LTI is installed. This default state of the RTC register data bits puts the Transfer Interface System (TIS) in a strictly "bumpless transfer" mode. Primary and Backup processors must be operating in synchronization with each other or else the Backup will not remain in RUN. In the event of a failure in the Primary, a bumpless transfer will occur — the Backup will pick up exactly where the Primary left off.

The user can alter these data bits via data entry or the ladder program. Once the bits are altered, there states are maintained until changed again by the user or all power (including battery backup) is lost.

RTC FAILURE OVERRIDE Bit (13)

Primarily this bit determines whether the TIS will be restricted to a synchronized bumpless transfer more or, for the sake of maintaining redundant backup, allow unsynchronized operation of the Primary and Backup, thus permitting a "bump transfer" to occur in the event of a failure in the Primary.

By leaving the RTC Failure Override bit reset OFF (0) in the Backup, the Backup will not be allowed to RUN out of sync with the Primary: should the Backup fall out of synchronization with the Primary, the Backup will generate an error and go into HALT.

NOTE: The Backup will fall out of sync if there is a failure in the RTC communication between the Primary and Backup LTIs, if the difference between the Primary and Backup scan times exceeds the scan hold time residing in the Scan Synchronization register or, if the Backup loses communication with one or more drops.

By setting the RTC Failure Override bit ON (1) in the Backup, the Backup is allowed to continue in RUN in the event that it falls out of sync with the Primary. Therefore, if a failure occurs in the Primary, a bump transfer is permitted. A bump transfer is a transfer that takes place when the Primary and Backup are out of sync with each other; thus, their I/O information may not be exactly the same. A bump transfer, due to alternate verification procedures, may take longer to execute than a bumpless transfer.

NOTE: In order to maintain TIS consistency when the Primary and Backup exchange rules, it is recommended that the RTC control register bits, in particular the RTC Failure Override bits, be programmed the same in both the Primary and Backup.

If the Backup loses sync with the RTC Failure Override bit set ON (1), it can be re-synchronized (provided that the RTC communication link is intact) by one of the following three methods:

1. Setting Re-Sync bit 15 ON (1).

2. Pressing the restart button on the Backup LTI that is in error.

3. Keyswitching the Backup from HALT to RUN.

Note that all three methods will cause a Startup Transfer to occur, thereby momentarily interrupting the processor scan and freezing all I/O. See Section 5.4.2.

TEST Bit (14)

This bit only affects a Backup LTI when there is a Primary LTI in RUN. When the TEST bit is set ON (1), the Backup LTI will not request a Startup Transfer of registers upon its HALT to RUN transition. This will allow the Backup system to be tested without initiating a Startup Transfer upon each HALT to RUN transition which would interrupt the Primary scan.

The test bit may be set (via any SY/MAX programmer) in the Primary *or* Backup LTI. In either case, the Backup will be forced into the test mode.

NOTE: With the TEST bit set, the Backup LTI cannot become Primary. For multiple LTI systems, the TEST bit must be set ON (1) for *all* Backup LTI modules to prevent any Startup Transfers.

To indicate that the TEST bit is ON (1), the PRIMARY and BACKUP LEDs will flash alternately on the Backup LTI; the Backup CPU LED on the RTI will be off, indicating a ready Backup is *not* present.

Upon resetting the TEST bit, the Backup will halt unless the RTC Failure Override bit is set.

RE-SYNC Bit (15)

The re-sync bit is only active in a Backup LTI that is in RUN. If the Backup loses sync with the Primary, having the Re-Sync bit ON (1) will cause the Backup to request a Startup Transfer in an attempt to re-synchronize the system. See Section 5.4.4.

For the re-synchronization to take place, the following conditions must be true:

1. Backup TEST bit must be reset OFF (0).

2. Backup's RTC FAILURE OVERRIDE bit must be set ON (1) if the error originates on the RTC channel; I/O FAILURE OVERRIDE bit must be ON (1) if error originates on I/O channel.

3. Backup RE-SYNC bit must be set ON (1).

4. Proper RTC communications must exist.

If the re-sync attempt is successful, the Backup will synchronize with the Primary. If the attempt is unsuccessful, the Backup will continually request a Startup Transfer to attempt to re-synchronize the system as long as the above four conditions are true and re-synchronization hasn't occurred.

NOTE: Whenever a Startup Transfer occurs, the Primary system scan time can be delayed for up to 1/2 second. See Section 5.4.2.

Certain conditions, such as broken RTC or I/O communication wires that make intermittent contact, can cause repeated Startup Transfers to be requested. Even though the operating system firmware only allows one Startup Transfer to be attempted every 100 scans, the resulting interruptions of the Primary processor's ladder scan must be taken into consideration. Thus, it is recommended that the RE-SYNC bit only be activated occasionally, and then only during non-critical operations (those that could be interrupted briefly for a Startup Transfer). Note the time required to execute a Startup Transfer can be minimized by only transferring those registers necessary for proper operation. See Section 5.4.2.

If the Backup is already in sync with the Primary when the Re-sync bit is turned ON (1), a Startup Transfer will not be requested.

For multiple LTI systems, all LTI's will perform a Startup Transfer whenever any one LTI requests it.

END OF SCAN (EOS) TRANSFER REGISTERS Bit (16)

This bit is only active in Backup LTIs in RUN. If this bit is set ON (1), at the end of every scan the Backup LTI will request a transfer of 32 registers from the Primary. The specific registers to be transferred are determined by the value residing in the End of Scan Transfer Register, the second register assigned to the RTC. Note if synchronization is lost, EOS register transfers will cease. See Section 5.4.3.

PRIMARY/BACKUP Bit (20)

This bit is turned ON (1) when an LTI becomes Primary and turned OFF (0) when it becomes Backup; it can be interrogated to initiate control action based on its Primary/Backup status.

TRANSMIT LOSS Bit (21)

This bit is turned ON (1) in a Primary or Backup LTI when its matched LTI has its receive loss bit turned ON.

RECEIVE LOSS Bit (22)

This bit is turned ON (1) in a Primary or Backup LTI when it is no longer receiving RTC communications.

BACKUP LOSS Bit (23)

This bit is turned ON (1) in Primary LTI modules that do not have a Backup that can become Primary. The bit is turned OFF (0) when Backup LTI modules are in RUN and are able to become Primary.

Backup LTIs set their BACKUP LOSS bit ON (1) when they are unable to become Primary.

STARTUP TRANSFER Bit (24)

This bit is turned ON (1) one scan before a Primary performs a Startup Transfer and is cleared at the completion of the Transfer. For multiple LTI systems, only the LTI that is initiating the Startup Transfer will turn on its Startup Transfer bit, even though all LTIs perform a Startup Transfer when any one requests it.

APPENDIX C — PRIMARY/BACKUP DETERMINATION

C.1 General Information

In order for the Transfer Interface System to work properly, rules exist to determine which system assumes Primary status. Figure C.1 lists the different possible states of each processor and an associated state priority number.

CPU State	Primary CPU Priority Number	Backup CPU Priority Number
RUN	7	6
RUN (I/O Failure Override bit set and drop error present)	5	6
DISABLE OUTPUTS	4	3
HALT	2	1
NO POWER	0	0

Figure C.1 — Processor State Priority

The RTC continuously tests the state of each processor rack. The processor that has the highest state priority will be declared as Primary. If both processors are in the same state, the system that was most recently Primary (indicated by the Primary/Backup history bit 20) will retain its Primary status. Should both processors have identical history bits, the processor which attains a higher priority state first will be declared Primary. In the event of a total tie, the LTI connected to the CPU A channel of the RTIs will become Primary.

C.2 Primary Determination at Power Up

At power up, A Backup system with no RTC communication will wait five seconds before making Primary determination. This is to allow the last Primary to have the first change at controlling the I/O system. If after five seconds the Backup finds no Primary, it will interrogate the I/O drops to see if they are communicating with a Primary processor. If they are, the Backup will assume a RTC fault, generate an error, and go into HALT (depending on the status of its RTC Failure Override bit). If the Backup finds that no RTIs are communicating with a Primary, it will assume Primary status when it goes into RUN.

If the Backup rack is powered up exactly five seconds before the Primary rack, it is possible for different LTIs in the same rack to have different Primary/Backup statuses. To prevent this ambiguous situation, at the end of every scan each processor will check to see that all LTIs in its rack have the same Primary/Backup status. If different Primary/Backup statuses exist, the processor will declare an error and go into HALT. The user can clear this error by power cycling and making sure that the rack to be designated as Primary is powered up at least ten seconds before the Backup rack.

If both systems power up as Primary at exactly the same time, they will both switch to Backup status. If one switches to Backup status before the other, the lagging system will remain Primary. If both systems become Backup at the same time, the processor connected to the CPU A channel will become Primary.

C.3 Primary Determination After Power Up

As described in Section C.1 of this appendix, during normal operation the Primary rack will be the rack with the highest state priority. If both racks are in the same state priority, the Primary rack will be the one with the Primary/Backup history bit set ON (1).

If a Backup does not have valid communication from the Primary RTC, it must determine from the RTIs whether or not to become Primary. This is possible since all RTI communication contains Primary/Backup status information. If it is determined from the RTIs that there is no Primary control, the Backup LTI will assume the Primary system is powered down and become Primary. If the Backup determines from the RTIs that there is Primary control, it will assume an RTC communication error, and follow action in accordance with the status of the RTC FAILURE OVERRIDE and TEST bits.

If a Primary in full RUN detects a communication problem with an I/O drop, it will tst to see if there is a Backup in full RUN able to become Primary. If so, the Primary will declare an I/O error and go into HALT, forcing a transfer to the Backup. Therefore the Backup becomes the new Primary. If a ready Backup is not found, the Primary will act in accordance with the I/O Failure Override bit (S8162-13).

A transfer from Primary to Backup will not occur in the event that an RTI declares a remote drop bus error. In this case, the Backup will go into HALT with an I/O error, regardless of the status of its I/O Failure Override bit while the Primary will either remain in RUN or not, in accordance with the status of its I/O Failure Override bit. This insures the safest and quickest manner of handling this type of fault.

C.4 Primary Determination Examples

The following examples illustrate several situations in which the TIS determines Primary/Backup status.

Example 1: Both Primary and Backup are in RUN when an LTI in the Primary generates an error: When the PRimary processor detects the error, it will declare an error and HALT. Since the Backup system is now in a higher state priority, it will assume Primary status and the system will continue to RUN.

Example 2: Primary processor in RUN, Backup in DISABLE OUTPUTS, when an LTI in the Primary generates an error: This is identical to Example I except the Backup will assume Primary status and the system will go into DISABLE OUTPUTS.

Example 3: Primary processor in RUN, Backup in HALT, when an LTI in the Primary generates an error: When the Primary processor detects the error, it will HALT the system. Since the Primary processor is still in a higher state, the Primary system will not switch to Backup status. The Backup will assume Primary status in the event the Backup processor is placed in DISABLE OUTPUTS or RUN.

Example 4: Primary in RUN, Backup powered down, when an LTI in the Primary generates an error: Since no Backup is present, the Primary processor will HALT with an error (unless the I/O failure override bit is set). If the Backup processor is powered up with its keyswitch in RUN or DISABLE OUTPUTS, it will first come up as a Backup, and then a transfer will take place, converting the Backup to the Primary.

Example 5: Primary processor in DISABLE OUTPUTS, when the Backup is placed in RUN: This is an illegal and inconsistent condition which should not be allowed to occur. Depending on rack addressing, program length, and other factors, the Backup may either HALT with an error or go into RUN. If the Backup goes to RUN, a transfer will result in real world outputs becoming active.

Example 6: Primary in RUN with I/O FAILURE OVERRIDE bit set ON (1), Backup in HALT, when the Primary experiences a communication failure with an I/O drop: Because the Primary (state 5) is in a higher state than the Backup (state 1), no transfer will take place, and the Primary system will remain in RUN with the bad drop shutdown. If the Backup is placed into RUN, the Primary will go into HALT with an error, and the Backup will become Primary.

Example 7: Primary and Backup processors in full RUN, both have the I/O FAILURE OVERRIDE bit set when an RTI declares *a remote drop bus error:* No transfer will take place. When the Backup detects a remote bus error, it immediately goes into HALT with an error, ignoring the I/O FAILURE OVERRIDE bit. The Primary continues to RUN, shutting down the bad drop.

Example 8: Primary processor is in RUN with I/O FAILURE OVERRIDE bit set ON (1) while the Backup processor is in RUN with I/O FAILURE OVERRIDE bit reset OFF (O): If the Primary system's I/O channel cable is severed, the Primary will recognize the communication error. Because a full Backup is present, the Primary will ignore its I/O FAILURE OVERRIDE bit and go into HALT with an error. When the Primary processor HALTs, all LTIs in the Primary rack will simultaneously go to Backup status, while the Backup becomes Primary.

Example 9: Both Primary and Backup systems are in full RUN, only the Primary I/O FAILURE OVERRIDE bit is set, and the Transmission Fault Tolerance bit (TXFT) is cleared: At this time, a noisy communication channel causes an RTI to miss three successive data blocks (which exceeds the fault tolerance determined by the TXFT bit). The RTI declares a communication error and the Primary generates an error and goes into HALT. When the Primary processor HALTs, all LTIs in the Primary rack go to Backup status and the Backup becomes Primary.

APPENDIX D — EXAMPLE TRANSFER INTERFACE SYSTEM

D.1 General Information

This appendix illustrates a complete Transfer Interface System. To help stress fundamentals of the TIS, this example uses a simple configuration. Actual applications may be more involved (i.e., with multiple LTIs), but the basic principles are the same. The example system is shown in Figure D.1.

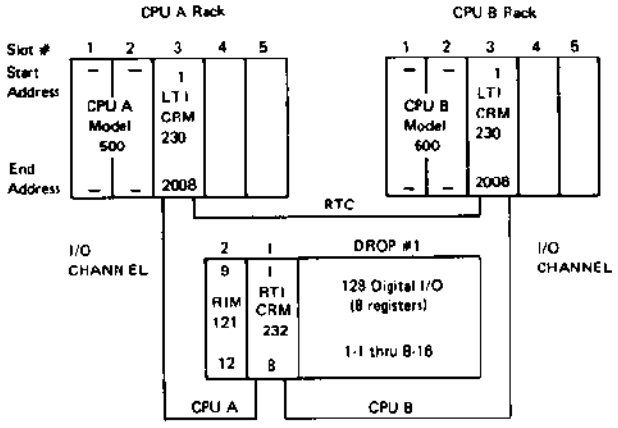


Figure D.1 — Example TIS

The above example consists of Model 500 processors, one set of LTI modules, and one I/O drop (with an RTI, Analog Input Module, and Digital I/O).

D.2 Rack Addressing

Refer to Figure D.1 and observe address assignments made. Note that the matched LTI modules (connected by their RTCs) must have identical rack addressing.

CPU Rack

SLOT 1 — The Model has not been assigned any internal registers. Recall that only LTI registers are transferrable.

SLOT 2 — Slot 2 of a Model 500 is not allocated any address assignments.

SLOT 3 — Although the LTI has 4096 registers available, the Model 500 can only address 2008 registers (S1 through S2008).

SLOT 4, 5 — No modules reside in these slots — address assignments are not required.

Addresses are now assigned to the I/O drop.

Channel 1, Drop #1

SLOT 1 — To accommodate 128 digital I/O points, eight 16-bit registers are required and assigned for the RTI (S1-1 through S8-16).

SLOT 2 — The analog input module requires four registers, therefore addresses S9 through S12 are assigned.

RTC (Channel 2, Drop #1)

Now that all external registers are assigned, the Register Transfer Channel must be addressed.

Channel 2, Drop #1

SLOT 1 — The next successive four registers (S13 through S16) are assigned to the RTC.

The individual function of these four registers is defined as follows:

S13 — Startup Transfer Register
S14 — End of Scan Transfer Register
S15 — Scan Synchronization Register
S16 — Primary/Backup Read/Write Bit Exchange Register

Internal Registers

The remaining registers assigned to the LTI (S17 through S2008), are internal registers that may be used as timers, counters, internal relays, etc. It is recommended that internal relays be located at addresses S17-S256 since only these are forceable.

If future expansion is a possibility, the registers expected to be required (beginning with S17) should be set aside in the program in anticipation of their future use as external rgisters.

D.3 Programming

To operate the TIS, no special programming or register presetting is necessary; the TIS will default as follows:

*Startup Transfer Register (S13) —	All 4096 registers of the LTI (register default value of 0)
*End of Scan Transfer Register (S14) —	No block of 32 registers designated due to register default value of 0. (Registers cannot transfer anyway unless EOS TRANSFER REGISTERS bit is set ON (1)
Scan Synchronization Time-out Register (S15) —	100 ms (register default value of 0)

FREEZE (S8162-9) — OFF
TXFT (S8162-10) — OFF (three transmission errors will be tolerated)
I/O FAILURE OVERRIDE (S8162-13) — OFF
I/O AUTO RESTART (S8162-15) — OFF
RTC FAILURE OVERRIDE (S8161-13) — OFF
TEST (S8161-14) — OFF
RE-SYNC (S8161-15) — OFF
EOS TRANSFER REGISTERS (S8161-16) — OFF

*Cleared upon any LTI power-cycle. Other registers and bits are battery-backed.

The LTI will default to the above conditions when it is initially powered up. If other than the default conditions are desired, the user must change the control register bits and the contents of the RTC registers. This can be done with the DATA mode of a programmer or through the ladder program itself.

For example, assume the TIS application requires the following conditions:

Startup Register Transfer — *S1 through S500*
End of Scan Register Transfer — *S17 through S48*
Scan Synchronization Timeout — *15 ms*

→ RTC registers (Section 5.4)

FREEZE — OFF
TXFT — OFF (Three transmission errors)
I/O FAILURE OVERRIDE — *ON*
I/O AUTO RESTART — *ON*
RTC FAILURE OVERRIDE — OFF
TEST — OFF
RE-SYNC — OFF
EOS TRANSFER REGISTERS — *ON*

→ LTI Control Registers (Appendix B)

Assuming the above functions are to be set by the ladder program (recommended method), the rungs listed in Figure D.2 are entered into both Primary and Backup programs. The first three rungs enable the I/O FAILURE OVERRIDE, I/O AUTO RESTART, and EOS TRANSFER REGISTERS functions. The last rung sets the RTC relative registers to obtain the desired number of START-UP TRANSFER registers, the correct range of END OF SCAN TRANSFER registers, and the desired SCAN SYNC TIMEOUT value.

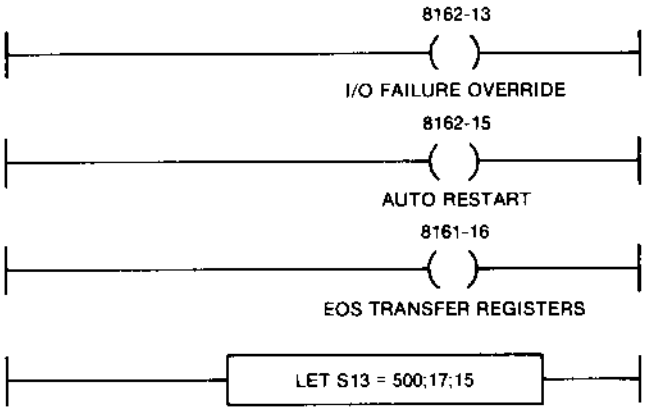


Figure D.2 — Programming Rungs for TIS Requirements

D.4 TIS Startup

Once the TIS has been rack addressed and any special function rungs have been programmed, the system is ready to RUN. See Section 6.0, System Startup.

NOTE: When initially testing TIS hardware, we recommend the I/O AUTO RESTART and I/O FAILURE OVERRIDE BITs be reset OFF (0). If these bits are programmed ON as coils within the ladder program, the insertion of an OPEN circuit function will reset (turn OFF) the coils.

Assuming CPU A is required to be Primary, CPU B should be powered up first and tested. If the CPU B system tests OK, power it down and then apply power to CPU A. After the CPU A system has been powered up and running for at least ten seconds, reapply power to CPU B.

APPENDIX E — ERROR CODES

E.1 Introduction And Description

E.1.1 GENERAL INFORMATION

Errors detected by the processor and error codes annunciated on the CRT provide the operator with information useful in isolating problems.

Some errors are indicated as messages on the screen display while other error indications involve error code numbers. Since the messages are self explanatory, this appendix deals directly with the numbered error codes.

These error code numbers can be broken into two general categories and are indicated in different locations on the CRT screen.

In the first category are the *peripheral to PC system interaction errors* of which three classifications of error codes exist. These errors are indicated at the bottom of the screen display or for some special cases, in the status register of a communications rung.

In the second category are the *PC system operational errors* which are errors detected within the processor or any one of the modules contained in a programmable controller system. These errors are indicated in the STATUS Mode display next to the label ERROR NUMBER. The number displayed is also the number contained in the error code control register 8175 or possibly in a Local Transfer Interface Module error code control register (when using remote I/O).

E.1.2 PERIPHERAL TO PC SYSTEM INTERACTION ERRORS

These types of errors are associated with attempts to perform illegal operations with the processor or the communication hardware is not functioning properly. This category of error will only be generated when using the keyboard to command processor operations or when the processor is attempting communication with other responding devices.

The three classifications of peripheral to PC system interaction error codes are: Processor, Transmission, and Tape. When an error occurs while a programmer is connected to the processor, one of these messages will be shown on the display along with a number. Should an error occur during the execution of a processor communication rung a Processor Error will be used to indicate the fault. The number code will be shown when the status register of the communication rung is displayed.

Processor Errors

These errors indicate that the operation attempted was not successfully completed. The error code numbers range from 01 thru 99. To resolve the error situation, check the error code description in the following table, use the CLEAR key to clear the error indication if the error has been displayed on a programmer, and take the appropriate recourse action. Error codes indicated by an asterisk (*) in the following Error Code Table, may also be displayed in the status register of a communications rung.

PROCESSOR ERROR CODE TABLE

Error Code No.	Error Description
01*	Illegal protocol opcode, the device does not recognize the instruction. Re-enter the desired operation.
02	Illegal intermediate code format. Re-enter the desired operation.
03*	An illegal address has been attempted.
04	Illegal rack addressing has been attempted.
05*	An instruction has been attempted which is not allowed in the processor. (Example: Square root in Model 300 processor.)
06	Item being searched for cannot be found.
07*	An attempt has been made to alter data in a protected register. Check Control Register 8176.
08	An attempt has been made to access protected memory. Check Control Register 8176.
09*	An attempt has been made to alter data in a READ only register or a register containing external inputs.
10	An attempt has been made to exceed memory limitations.
11*	Communications error (receiver overflow). Re-enter the desired operation.
12	Illegal CPU rack addressing; register assignments must be divisible by four.
13*	Communications error (link error). This error is generated by the processor. Check Control Register 8175 or the status register of the communication rung. Check cable connections between devices.
14	The operation that has been attempted is not allowed in RUN.
15*	Communication overflow. Check the baud rate for compatibility between communicating devices. Re-enter the desired operation.
16	The register count in a communication run is too large for the processor.
17*	The remote device is inactive. This error code is generated by the Network Interface Module. Check cable connections between devices.
18	The rung number used is not allowed.
19*	An illegal READ parameter has been assigned.
20	An illegal channel number, or no channel number has been assigned.
21*	Trying to change a forced bit or WRITE to an external output while the processor is in HALT.
22	The forcing function is inhibited from the processor COMM port.
23*	An attempt has been made to alter data in a fenced register.

Error Code No.	Error Description
24	An attempt has been made to force a nonforceable register.
25*	CPU error, check Control Register 8175. Refer to the following section on CPU/LI errors.
26	Rack Addressing and user memory overlap.
27*	Memory error. A CLEAR ALL operation is required.
28	An illegal baud rate was selected.
29*	An attempt has been made to send a message with an illegal route.
30	An attempt has been made to alter PROM memory after the PROM inhibit coil was entered in memory.
31*	See Tape Errors.
32	Operation is not allowed in PROM memory (such as inserting, deleting, or replacing a rung).
33*	See Tape Errors.
34	For UVPROM processors only: Read after Write error; parity error; or security jumper was removed and no UVPROM inhibit coil was programmed into memory.
35*	See Tape Errors.
36	Replace rung operations are not allowed on this rung. Use delete and insert operations only.
37*	See Tape Errors.
38	Unused.
39*	Alarm already set within the D-LOG Module.
40	Unused.
41*	An illegal register WRITE. The D-LOG Module does not accept a register WRITE into certain registers.
42	Unused.
43*	An illegal operation has been attempted. D-LOG Module protected.
44	Unused.
45*	Operation is not allowed. D-LOG Module tape operation is in progress.
46	Unused.
47*	Operation is not allowed due to keyswitch position.
48	Programming of an MCR in subroutine area is not allowed.
49	I/O, Register or Channel is safeguarded.
50	Rack Addressing is not alterable when forcing is active.
51*	A module is not seated properly or missing, or no rack address assigned to the module, or the address exceeds the capability of the processor.
52	Unused.
53*	See Tape Errors.
54	Illegal MARK number.
55	See Tape Errors.

Error Code No.	Error Description
56	Unused.
57	Unused.
58	Unused.
59	Unused.
60	Illegal MARK number. GOTO or GOSUB with numbers above 8189 not allowed.
61	MARK ST. SUB rung cannot be inserted-append only allowed.
62	RTN (return) rungs are not allowed in ladder area.
63	MARK number previously used in the program. Each MARK instruction must have a unique number assigned.
64	Operation is not allowed while the processor is in RUN. Cannot delete a RTN if any GOSUB contains the same MARK number.
65	Operation is not allowed. Cannot delete MARK ST. SUB rung unless all subroutines are deleted.
66	Operation is not allowed — cannot delete MARK having an associated RTN (return).
67	Operation is not allowed – RTN rungs must have an associated MARK number.
68	Operation is not allowed - only one RTN per MARK number is allowed.
69	Operation is not allowed while the processor is in RUN GOSUB cannot invoke a subroutine having no RTN.
70	Operation is not allowed while the processor is in RUN — GOTO rung cannot jump to a MARK having an associated RTN.
71	Operation is not allowed while the processor is in RUN — cannot delete MARK until all GOSUBs or GOTOs with the same number are deleted.
72	Operation is not allowed while the processor is in RUN – rung cannot have unused MARK number. A GOTO or GOSUB with an undefined MARK is not allowed. The MARK must be programmed before the GOTO or GOSUB is programmed.
73	Unused.
74	Unused.
75	Unused.
76	Unused.
77	Unused.
78	Unused.
79	Operation is not allowed when the processor is in RUN while the Timed Interrupt is enabled.

Tape Errors

These errors are generated when performing tape operations. When the processor is operating with a Loader/Recorder through the use of communications rungs, the status register of that rung can be checked for the presence of an error condition.

Error Code No.	Error Description
31*	The end of the tape was encountered before the operation could be completed.
33*	Tape Data Error detected, the block of data involved in the Read or Write operation was faulty.
35*	The tape cartridge is not seated properly or is missing, or the "Record" tab on the cartridge has been set to the Write Inhibit position.
37*	An attempt to Skip or Read a file was made when already past the last file on the tape.
53*	Illegal Tape Format — Erase Track Required.
55*	Tape operation has been aborted. Retry the operation.

Transmission Errors

Communication errors due to hardware problems are annunciated on the CRT screen by the message "Transmission Error" followed by a number.

The error code numbers that appear most frequently are numbers 1, 72, and 74. When an error such as this occurs, check all cable connections and BAUD rates (Register 8169), then use the CLEAR key to clear the error indication. When all connections are secure, retry the operation.

E.1.3 PC SYSTEM OPERATIONAL ERRORS

These error codes indicate PC system operational errors and consist of a five digit decimal value. These error codes or (ERROR NUMBERS) are the contents of the Control Register 8175 data field (bits 1-16). Seven possible classifications of operational error codes exist and they are:

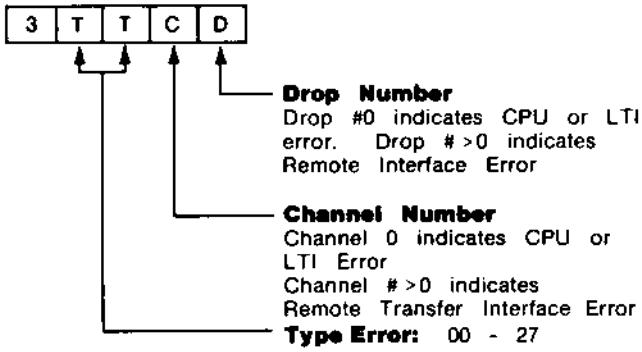
ERROR NUMBER	TYPE OF ERROR
30000 - 32700	CPU/LTI ERROR
29000 - 29999	MISCELLANEOUS ERROR
20000 - 28192	SLOT REGISTER ERROR
19000 - 19016	SLOT ERROR
10000 - 18192	READ AFTER WRITE ERROR
01000 - 09999	PROCESSOR COMMUNICATION PORT ERROR
00001 - 00999	GENERAL ERROR

When an error condition occurs, the appropriate error code is loaded into Control Register 8175 only if the register contains zero or if it presently contains an error code of lower priority (a smaller number). The previous error code is then lost (if a Model 300) or moved to Register 8183 (if a Model 500 or 700).

The same operational errors are used by the Transfer Interface System to indicate errors in devices under its control. In this case, Register 8175 or the ERROR NUMBER in the CRT Status display will indicate the starting address of the Local Transfer Interface which has the problem. Once located, inspection of the error control register inside the Local Transfer Interface will reveal which of the remote devices contains the error. Refer to Section E.2 for greater detail on using the error codes to isolate system faults.

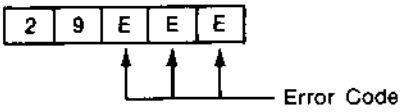
CPU/LTI Error (30000-32700)

This error indicates a problem with either the processor (CPU) or Local Transfer Interface Module.



TT	ERROR DESCRIPTION
00	Status Register Read/Write Parity Error
01	Image RAM Read/Write-Parity Error
02	Internal Register Data Error
03	Illegal PROM Format
04	Illegal Opcode Encountered in RUN
05	Bus Error Signal Error (Interrupt detected on Bus)
06	Software Watchdog Error
07	Not Used
08	Software Diagnostic Error
09	User Memory Read Write-Parity Error
10	Illegal Data in User Memory
11	PROM Memory Corrupted
12	Illegal Addressing Map Code
13	Transmission Error Exceeds Tolerance
14	Loss of Transmission
15	More External I/O Registers Assigned Than Module Can Handle
16	Too Many Registers Assigned to the Drop
17	Addressing More Drops than Channel can handle
18	Addressing Number of Channels Exceeded Module Capabilities
19	Addressing Map Checksum Error
20	Bus Error — Watchdog Time Out
21	BPU Diagnostic Error
22	Parity Circuit non-functional
23	Clear Line Error
24	Executive Scratch RAM Error
25	Watchdog Tolerance Error
26	Hardware Diagnostic Error
27	Module Inactive

Miscellaneous Errors (29000-29999)



EEE	Error Description
000	Subroutine Nesting Error.•
100	Time to Process the Timed Interrupt Subroutine has Exceeded the Time Base.•
101	Timed Interrupt Routine Missing.
102	Time to Solve a Rung has Exceeded the Tolerance Set Within a Timed Interrupt.•
201	MCU Software Mismatch with LCU.
202	LCU Software Mismatch with MCU.
300	Mixed Primary/Backup LTIs in CPU Rack.*
301	LTI Timeout on EOS Transfer. ■
302	LTI Timeout on Start-Up Transfer.■
500	Number of Assigned Local Transfer Interface Registers must be at least 8 for 1 defined channel, 12 for 2 defined channels.
501	Insufficient Local Transfer Interface Control.
510	RTI Wired Improperly — Channels A and B are mixed.
511	LTIs in CPU racks A and B have equal states of operation and no primary determination can be made in HALT.
512	Backup Transfer System cannot be in RUN when Primary Transfer System is in DISABLE OUTPUTS.
513	Rack Addressing between LTIs in racks A and B (Primary and Backup) are not the same.
514	Backup cannot be in run with Test bit set when Primary goes to HALT. Backup must also go to HALT.
515	Backup cannot become Primary until synchronization has occurred and Primary goes to HALT.
516	Backup unable to become Primary because remote bus error exists. Also error generated by Primary to allow transfer to Backup when Primary keyswitched to HALT.
517	Backup has lost synchronization and does not have RTC FAILURE OVERRIDE bit set.
518	Two Primary processors were found in RUN; this processor was halted with a bus error.

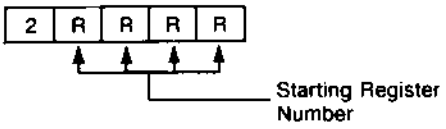
- • Control Register 8184 will contain the rung number where the error took place. If 8184 equals zero, check Rack Addressing.

- * The data field of Control Register 8184 contains the bit table of primary or back-up status (bit set indicates primary) while the status field of Control Register 8175 identifies the slots which contain LTIs (bit set indicates LTI present).

- ■ The data field of Control Register 8184 identifies the first register assigned to the LTI that caused the error while the status field of Control Register 8175 contains the elapsed time (in msec.) that the scan was held.

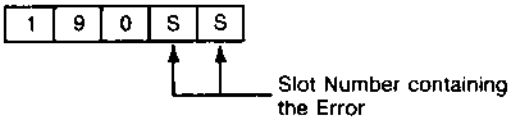
Slot Register Error (20000-28192)

In the event of a Slot Register Error, the ERROR NUMBER (last four digits) will point out the first register number assigned to the CPU register slot containing a faulty register module. Further inspection of that register's status field will provide additional diagnostics.



Slot Error (19000-19016)

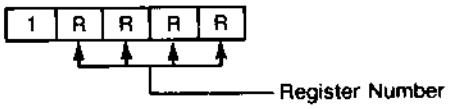
In the event of a Slot Error, the ERROR NUMBER will point out the slot number experiencing the error.



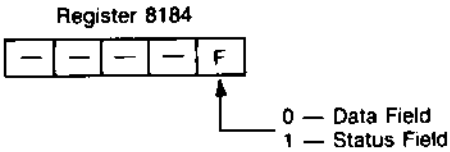
NOTE: ERROR 19000 same as ERROR 32000.

Register Read After Write Error (10000-18192)

A read after write error indicates a particular bit in a register has not maintained the condition written to it by the processor. The error number (last four digits) will point out which register encountered the problem.



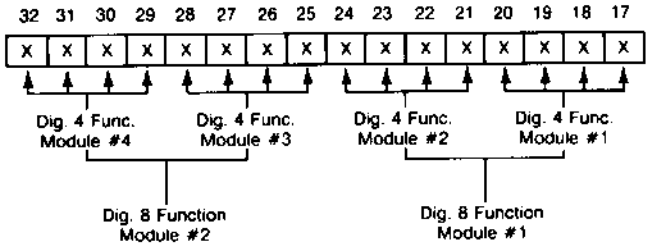
By displaying the status field (bits 17-32) of the control register containing the error code, the bit or bits causing the malfunction will be indicated (by a 1). Since each register contains both a status field and a data field, control register 8184 is used to indicate which set of bits contains the problem.



If the faulty register is used to control outputs and control register 8184 indicates the bad bits are contained in the data field, most likely an output module has caused the problem. Following is a diagram which can be used to isolate the output module having the problem.

In addition, note that a parity error can also be detected in a register and is indicated by a zero in all bit positions.

Status Field of Control Register 8175 or of Local Transfer Interface Error Control Register.

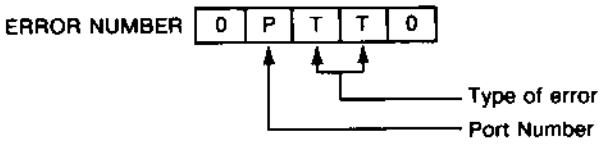


Checks:

a. If X = 0, bit was read correctly.
b. If X = 1, bit was read incorrectly.
c. If all X's = 0, parity error was detected.

Processor Communication Port Error (01000-09999)

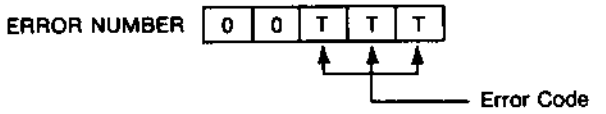
To clear a communication port error, toggle the processor keyswitch from HALT to RUN, or Clear S8175. If this does not clear the error, cycle power to the processor. These errors can be seen in the STATUS Mode Display by the ERROR NUMBER. Also check remote device and cable connections.



TTT	ERROR DESCRIPTION
11	Communications overflow.
12	Buffer overflow.
13	Illegal data.
14	Wrong reply (odd/even).
15	Checksum error.
16	Framing error.
17	Parity error.
18	Inability to communicate thru Port #P.
19	Retry timeout.

General Errors (00001-00999)

The ERROR NUMBER in the Status Display indicates the problem.



TTT Error Code	Error Description
900	Control registers corrupted.*
901	Data registers corrupted.*
960	HALT or HALT/RUN bit set.
962	Tolerance equal to or greater than the rate.
963	Timed Interrupt time base is less than 3.
964	GOTO and GOSUB to same MARK.***
965	Illegal Internal Error Code.
966	User Subroutine Stack Error.***
967	A MARK rung with the same reference number is required.***
968	GOTO to MARK with RTN (return).***
969	GOSUB to MARK with no RTN (return).***
970	Scan Time of processor is greater than 1 second or scan limit in S8167 has been exceeded.**
971	Scan Time limit of processor has been exceeded due to long LTI start-up transfer. (Check register 8184 for elapsed time in msec.)
979	Rack Addressing missing.
980	Keyswitch in RUN and no program in memory.
981	PROM inhibit coil not in memory (PROM processor).
983	Safeguarding rung not in memory or programmed incorrectly.
984	Undefined register programmed in user memory.**

* Control registers are normalized and data registers are cleared. Toggling keyswitch will allow CPU to run.

** S8184 will contain the rung number being executed when the error occurs.

*** S8184 will contain the MARK number.

E.2 Using Error Codes To Isolate P.C. System Faults

E.2.1 GENERAL CONCEPT

When a P.C. system which was once operating correctly malfunctions, one of three situations can arise: either the whole P.C. system shuts down, one or more drops shut down, or a run time communication port error is detected. Once the malfunction is identified as existing in one of these three categories, the P.C. SYSTEM OPERATIONAL ERROR CODES can be used to isolate the fault. Recognition of the first category is obvious; however, the second category can exist only when the P.C. system incorporates remote I/O and the override bit is set in the Local Transfer Interface Module.

The third category of malfunction deals with communications to external devices and requires that control register 8175 be monitored by the program for errors in the range 01000 to 09999. These types of errors are different from those described in the "Processor Errors" section in that they are generated by the processor itself and not by the external device.

E.2.2 WHEN THE SYSTEM SHUTS DOWN

When the processor halts, register 8175 should be the first point of interogation. The error code indicated will be one in the following number ranges:

Error Code	Description
30000-32700	CPU/LTI Error
29000-29999	Misc. Error
20000-28192	Slot Register Error
10000-18192	Read After Write Error
00001-00999	General Errors

In the case of the 20000-28192 Slot Register Errors two courses of action may be taken depending on the register number indicated by the last four digits. If the register is the first assigned to a register module, interrogating the status field of that register will indicate the error. (Refer to appropriate register module Instruction Bulletin.) If the register number is the first assigned to a Local Transfer Interface Module (when using the Transfer Interface System), then further interrogation of the LTI error code register is required. (Refer to Appendix B.2 to determine the address of the LTI error code register/s.) When the LTI error code register is interrogated, the number will be in the following ranges:

LTI Error Code	Description
30000-32728	CPU/LTI Error
20000-28192	Slot Register Error
10000-18192	Read After Write Error

In the case of the 10000-18192 Read After Write Errors, the affected bit or bits are indicated in the status field of the *LTI error code register.*

Following is a flow chart which illustrates the previously described procedure.

P.C. SYSTEM
SHUTS DOWN

STEP 1: INTERROGATE S8175

- IF 30000-32700; Refer to "CPU/LTI Error"
- IF 29000-29999; Refer to "Misc. Error"
- IF 20000-28192; IF 19000-19016; Refer to STEP 2, following Ensure module(s) are seated properly in rack.
- IF 10000-18192; Look at status field of S8175 for an indication of the affected bits and refer to "Read After Write Error"
- IF 0001-9999; Refer to "General Error" and interrogated control register S8184 when indicated.

STEP 2: USING THE REGISTER NUMBER INDICATED BY THE LAST FOUR DIGITS DETERMINE THE SLOT TO WHICH THE REGISTER IS ASSIGNED

- IF assigned to a register module; Look at status field of the register number indicated by the error code then refer to appropriate register module Instruction Bulletin for the meaning of the error number.
- IF assigned to a Local Transfer Interface Interrogate the LTI error code register then refer to STEP 3

STEP 3: INTERROGATE THE LTI ERROR CODE REGISTER

- IF 30000-32700; Refer to "CPU/LTI Error"
- IF 20000-28192; Using the register number from error code (last four digits), determine slot to which register is assigned. The register module in that slot, generated the error. Look at status field of that register then refer to appropriate register module Instruction Bulletin for the meaning of the error number.
- IF 10000-18192 Look at status field of LTI error code register for an indication of the affected bits and refer to "Read After Write Error"

Refer to Appendix B.2.2 of the Model 500 or Model 700 Instruction Bulletins for examples.

E.2.3 WHEN A REMOTE RACK SHUTS DOWN

When the P.C. system incorporates a Transfer Interface System and a remote rack or racks halts without causing the rest of the system to halt, the error code register of the Local Transfer Interface module controlling that drop will contain the error number of the fault. When the LTI error code register is interrogated, the number will be in the following ranges:

LTI Error Code	Description
30000-32728	CPU/LTI Error
20000-28192	Slot Register Error
10000-18192	Read After Write Error

In the case of the 10000-18192 Read After Write Errors, the affected bits are indicated in the LTI error code register.

Following is a flow chart which illustrates the previously described procedures.

REMOTE RACK/S
SHUTS DOWN

↓

STEP 1: INTERROGATE APPROPRIATE LOCAL TRANSFER INTERFACE ERROR CODE REGISTED

IF 30000-32700; Refer to "CPU/LTI Error"

IF 20000-28192; Using the register number from error code (last four digits), determine slot to which register is assigned. The register module in that slot, generated the error. Look at status field of that register then refer to appropriate register module Instruction Bulletin for the meaning of the error number.

IF 10000-18192; Look at status field of LTI error code register for an indication of the affected bits and refer to "Read After Write Error."

Refer to Appendix B.2.3 of the Model 500 or Model 700 Instruction Bulletin for examples.

E.2.4 PROCESSOR COMMUNICATION PORT ERROR DETECTED

These errors are different from those Processors Errors associated with communications listed earlier in this appendix. The difference is that Processor Communication Port Errors are detected by the processor rather than the external communicating device. The only Processor Error that has any relationship to Processor Communication Port Errors (01000-09999) is Processor Error code 13. When error 13 is indicated in a status register of a communication rung, interrogation of control register 8175 will result in the display of one of the Processor Communication Port Errors (01000-09999).

These errors can also be detected when an external device is asking for information from the local processor. In this case, there is no communication rung status register to indicate the fault. Therefore, it is up to the user to implement the means to annunciate these types of errors.

APPENDIX F — APPLICATION CONSIDERATIONS

This appendix lists several points to consider with Transfer Interface System applications. The TIS is designed to be as straightforward or complex as the user desires. Control register bits can be used to tailor the TIS to particular customer applications.

F.1 General Considerations

1. The user must realize that the TIS is designed to withstand any *single* Primary/Backup fault and remain operating. The fault must be repaired before the TIS can withstand another fault. If, however, the RTC Failure Override bits are set, the TIS can withstand a fault in RTC communications plus one other *single* Primary/Backup fault.

   By setting the I/O Failure Override bit ON, the processor can continue in RUN: the user can program individual drop shutdowns, as opposed to having the processor go to HALT and all drops unconditionally shut down when one drop shuts down due to an I/O error.

2. Due to the fast transfer times and the fact that I/O are frozen during the switch, the TIS yields an essentially bumpless transfer. Input signals present for longer than the transfer time wil not be lost.

3. When using the I/O FAILURE OVERRIDE bits programmed as ladder rungs (Appendix B, LTI Control Registers), these rungs must be the first rungs in the ladder program. An exception to this rule is if timed interrupts or any other features which require programming the TLET S8165 rung are used. In this case the I/O FAILURE OVERRIDE bit rungs should immediately follow.

4. It is important to remember that each LTI in a TIS has its own control register. Control bits must be set/reset in each LTI to ensure proper operation, i.e., in order to test a Backup system (by cycling the RUN-HALT keyswitch) without initiating a Startup Transfer, the TEST bit must be set ON (1) for *all* Backup LTI modules.

5. The Startup Transfer of registers will delay the Primary processor scan. Therefore, it is recommended that a Startup Transfer not be initiated during a critical Primary process. See Section 5.4.2.

6. The status of FORCED I/O is not transferred from one processor to the other. Even if the register which contains the bit being FORCED is included in an End of Scan Transfer, the FORCE state will not be included.

7. To preclude nuisance I/O transmission errors upon system power-up, ensure that all RTI racks in the system power up prior to the CPU racks.

8. Processor types may be mixed (e.g., a Model 700 Primary may be used with a Model 500 Backup) though differences in scan time, instruction set, and rack addressing must be taken into account.

9. In keeping with #4, in order to preserve the "bidirectional" nature of the TIS, we strongly recommend having control bits set identically in all LTIs in both the designated Primary and Backup. Bear in mind that each LTI will have its own group of two control registers plus an error code register.

10. Processor types may be mixed (e.g., a Model 700 Primary may be used with a Model 500 Backup) though differences in scan time, instruction set, and rack addressing must be taken into account.

F.2 Primary/Backup Bit Exchange

As described in Section 5.4.5, in the fourth register assigned to the Register Transfer Channel, eight bit locations are used to allow the Primary and Backup to interact with each other.

At the end of every synchronized scan, 4 bits (2 from the Primary, 2 from the Backup) are transferred back and forth between matched LTIs. Two Backup WRITE bits (1 & 2) are transferred to Primary READ bit locations (5 & 6); and two Primary WRITE bits (3 & 4) are transferred to Backup READ bit locations (7 & 8). The user decides what data is transferred back and forth by writing that data into bits 1 & 2 and 3 & 4, respectively. Figure F.1 illustrates this bit "cross-talk" of the Primary/Backup READ/WRITE register.

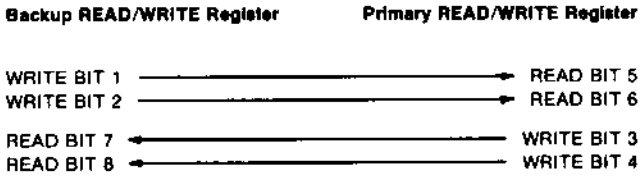


Figure F.1 Bit Exchange of READ/WRITE Register

Example 1 —
Using the same rack addressing illustrated in Section 5.3.5, Figure F.2 illustrates how READ/WRITE bits can be used so that the Primary program can control the Backup program.

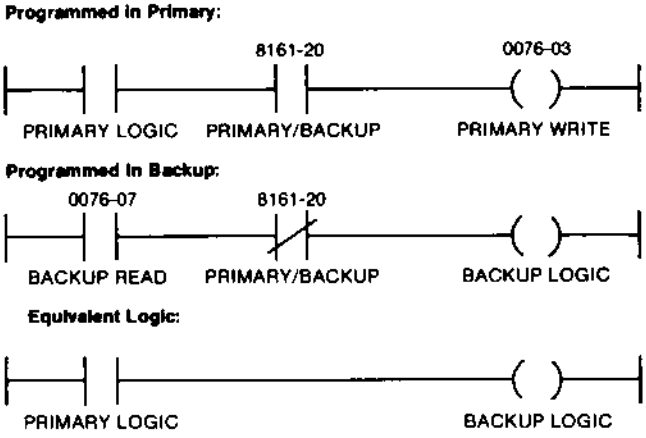


Figure F.2 — Primary-to-Backup Control

Control bit 8161-20 will be set ON (1) in the first Primary LTI, and reset OFF (O) in its Backup LTI. Thus, 8161-20 is used to enable the particular PRI/BAK WRITE/READ rungs. This contact is not required for the circuit to function.

In Figure F.2, when the Primary logic contact is closed (the Primary/Backup contact is already closed by definition), the PRIMARY WRITE coil is energized. At the end of the Primary processor scan, this bit is transferred to the BACKUP READ bit in the Backup. Therefore, contact 0076-07 is closed (the Primary/Backup contact is also closed by definition), and the Backup logic coil is energized.

Thus, the equivalent circuit is a Primary logic contact controlling a Backup logic coil.

Example 2 —
Conversely, Figure F.3 illustrates how the Backup program can control the Primary program.

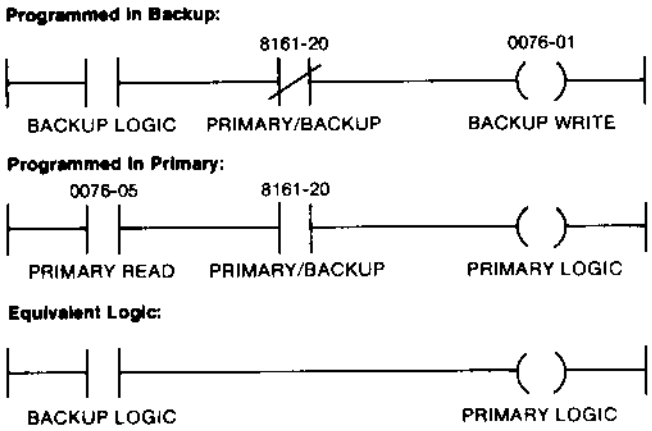


Figure F.3 — Backup-to-Primary Control

Example 3 —
Because a Startup Transfer will delay the Primary system, the user may wish to program a few rungs that will enable the Primary system to disable a Startup Transfer from being initiated by the Backup system.

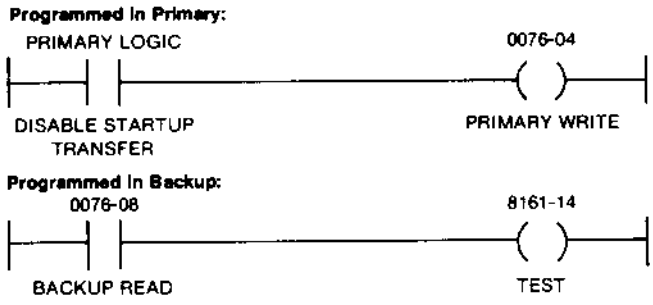


Figure F.4 — Primary Disable of Startup Transfer via Ladder

When the Primary logic contact is closed, the Backup TEST bit will be set ON (1). Recall that when the TEST bit is ON, the Backup LTI will not initiate a Startup Transfer and cannot become Primary.

F.3 Different Primary/Backup Systems

Although most applications will use identical Primary and Backup programs, some systems may benefit from having different Primary and Backup programs. For instance, the application may require a different Backup program to initiate a shutdown or alarm sequence if the Primary system fails.

Recall that the user can vary the amount of time that the TIS will allow between End of Scan times of the Primary and Backup scans. This can be done by altering the contents of the Scan Synchronization Register (see Section 5.4.4).

Another alternative for application requiring different Primary/Backup programs is to use the subroutine capabilities of the Model 500 and 700 Processors. Any shutdown or alarm routines can be programmed as subroutines and not be scanned until the Backup becomes Primary. Thus, Primary/Backup scans should be similar when both are in RUN. Figure F.5 illustrates this principle.

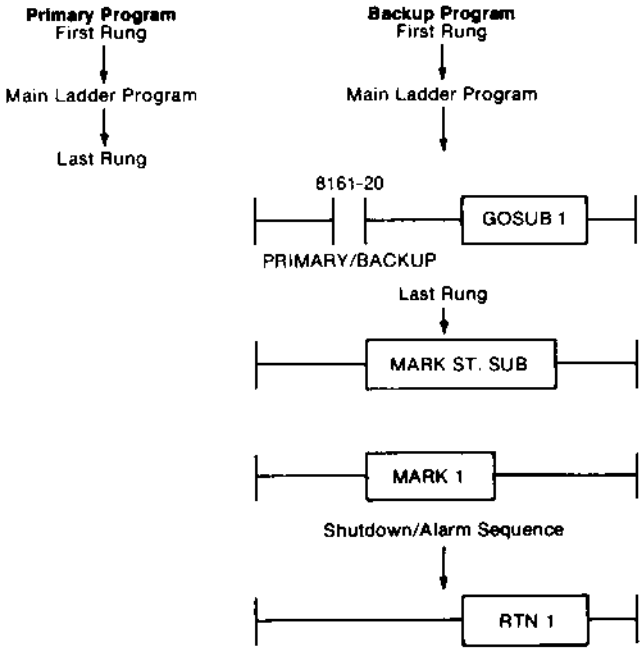


Figure F.5 — Backup Shutdown/Alarm Sequence

Examining Figure F.5 — as long as the TIS is completely operational with Primary and Backup processors in RUN, the two scan times should be nearly identical. If the Primary system should HALT and the Backup become the new Primary, Subroutine #1 will be enabled. This subroutine may contain a shutdown sequence for the machine or plant, or a program to alarm plant personnel that the previous Primary system is down and must be repaired to bring the complete TIS on line.

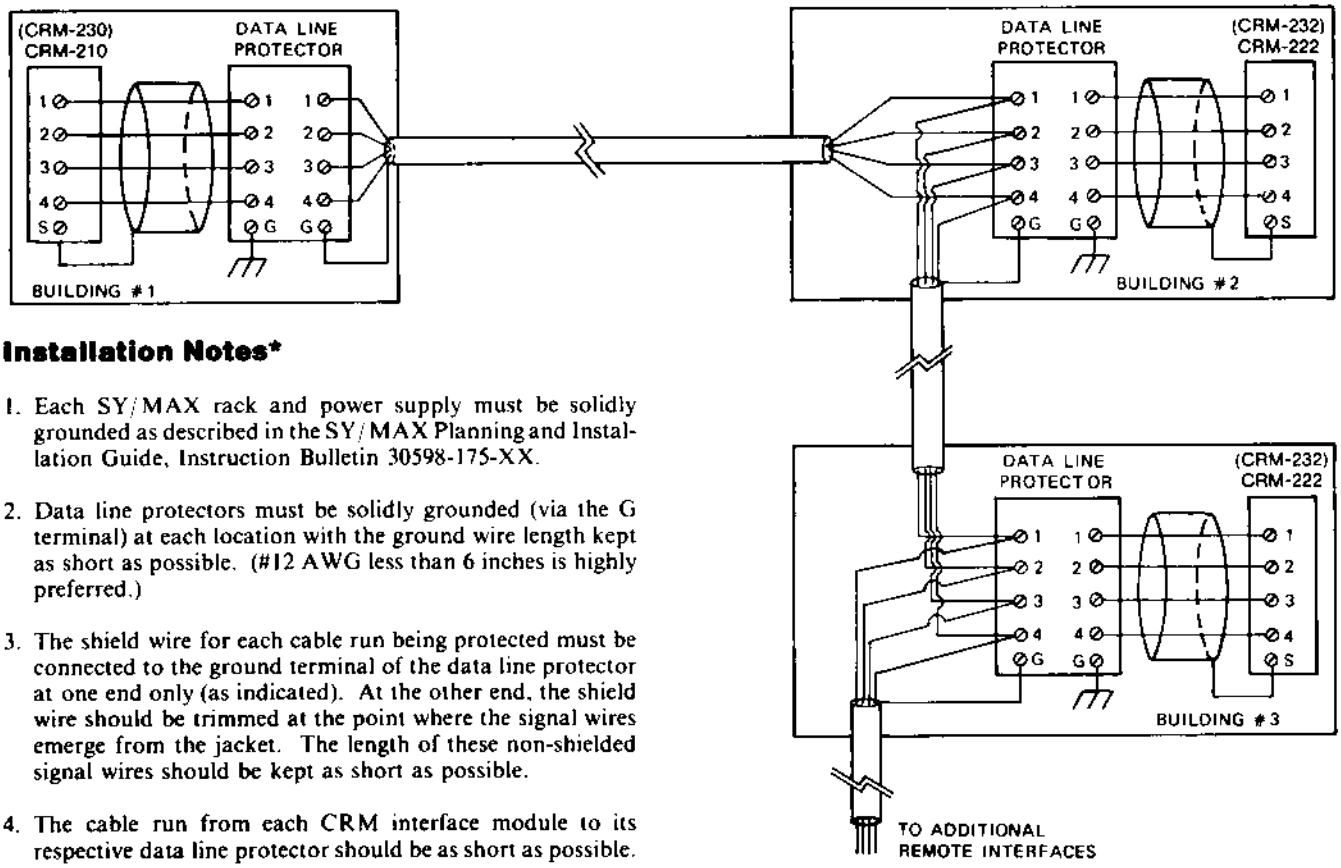
This principle can be extended to enable a Primary subroutine should be the Backup system HALT.

F.4 Redundant I/O

The TIS provides redundancy in the event of failures in processors, LTIs, racks, power supplies and communication cables. The TIS does *not* provide redundant I/O.

Apart from the TIS, redundant power supplies may themselves be used to drive individual racks. This capability exists when using a CC-51 cable with two PSI-11, -21, or -42 power supplies. Refer to Power Supply Instruction Bulletin #30598-159-01 or later.

APPENDIX G — ADDITIONAL DATA LINE PROTECTION



Installation Notes*

1. Each SY/MAX rack and power supply must be solidly grounded as described in the SY/MAX Planning and Installation Guide, Instruction Bulletin 30598-175-XX.

2. Data line protectors must be solidly grounded (via the G terminal) at each location with the ground wire length kept as short as possible. (#12 AWG less than 6 inches is highly preferred.)

3. The shield wire for each cable run being protected must be connected to the ground terminal of the data line protector at one end only (as indicated). At the other end, the shield wire should be trimmed at the point where the signal wires emerge from the jacket. The length of these non-shielded signal wires should be kept as short as possible.

4. The cable run from each CRM interface module to its respective data line protector should be as short as possible.

5. If building #2 contains multiple drops, they must be daisy-chained together with shield terminals wired per Figure 3.4 in the LI/RI Instruction Bulletin 30598-247-XX. A second data line protector would be required for the last drop in the chain in building #2, to protect the cable run from building #2 to #3.

6. A recommended data line protector is the DLP-20-6V10 manufactured by MCG Electronics, Inc., 160 Brook Avenue, Deer Park, NY 11729, Telephone: (516) 586-5125.

*NOTE: The figures and references pertain to the LI/RI (CRM-210/220 or 222) but the lay-out and wiring also apply to the external I/O for the LTI/RTI system.

Addendum

SY/MAX®

Class 8030 Type CRM230 Local Transfer Interface (LTI) Modules
Series D3 (No Revision Designation) and Earlier

(Addendum for Instruction Bulletin #30598-251-01)

WARNING

Potential hazard for personal injury or property damage.

CONDITION:
Under certain circumstances there is a remote possibility of outputs not following the application program properly when using the Type CRM230 Local Transfer Interface Module.

For the problem to exist the following must occur:

1. The system must be set up to run with "I/O Failure Override" and "I/O Auto Restart" enabled (bits 13 and 15 of register(s) 8162, 8159, 8156, etc., set ON).
2. The system must be in RUN.
3. One or more of the remote drops connected to the CRM230 loses communication.
4. A restart is attempted by the I/O Auto Restart bit or the RESTART pushbutton.

RESULT:
When re-establishing communication with the failed drop (via the "I/O Auto Restart" bit or the "Restart" button on the LTI) a remote chance exists that the system outputs will not follow the application program.

SOLUTIONS:

1. **Do not use** "I/O Auto Restart" (bit 15 of register(s) 8162, 8159, 8156, etc.) or the "RESTART" button on the front of the LTI in the referenced modules to re-establish communication with remote drops.

   If communication to a remote drop has failed and "I/O Failure Override" is enabled, the primary CPU will halt and the system will continue to run on the backup CPU. To re-establish communication to the complete RTI system, do the following:
   A. Toggle the keyswitch on the halted processor (formerly the primary) to HALT and back to RUN.
   B. If the communication fault was cleared, the former primary CPU will resume control over all drops; toggling the keyswitch on the backup CPU to HALT and back to RUN will result in "ready Backup" status.
   C. If the communication fault remains, the former primary CPU will resume control over all properly communicating drops. Once the fault is cleared, the keyswitching procedure may be used to allow full system recovery, i.e. a running primary CPU with a ready backup CPU.

2. Use modules that are Series D3 **and** Revision 2.0 or later.

Figure 3.1 — Local Transfer Interface

Figure 3.2 — Remote Transfer Interface

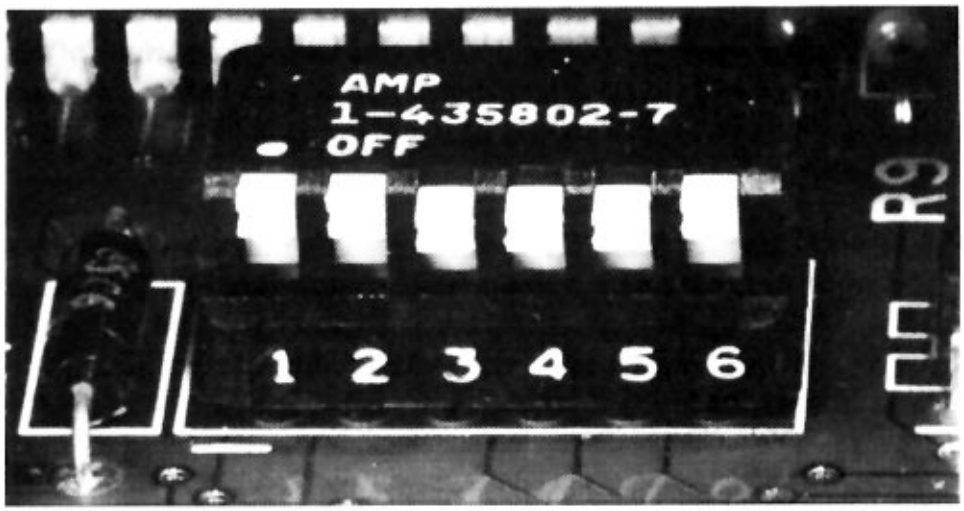


Figure 3.3 — RTI DIP Switches