7.6 DI135

7.6.1 Technical Data

Module ID	DI135
General Information	
Model Number	7DI135.70
Short Description	2003 digital input module, 4 inputs 24 VDC, sink, incremental encoder operation: 50 kHz, event counter operation: 100 kHz, 1 comparator output 24 VDC, screw-in module, Order terminal block TB712 separately!
C-UL-US Listed	Yes
B&R ID Code	$12
Module Type	B&R 2003 screw-in module
Slot	AF101 adapter module, CP interface
Power Consumption	Max. 0.4 W
Inputs	
Number of Inputs	4
Wiring	Sink
Input Voltage Minimum Nominal Maximum	 18 VDC 24 VDC 30 VDC
Input Frequency Incremental Encoder Operation Event Counter	 50 kHz 100 kHz
Switching Threshold LOW HIGH	 <5 V >15 V
Input Delay	Max. 3 μs (at 18 - 30 V)
Input Current at Nominal Voltage	8 mA
Electrical Isolation	Input - PCC

Module ID	DI135
Incremental Encoder	
Signal Form	Square wave pulse
Evaluation	4-fold
Input Frequency	50 kHz
Count Frequency	200 kHz
Phase Offset between Channel A and B	90° ±25°
Counter Size	32 Bit
Inputs Input 1 Input 2 Input 3 Input 4	 Channel A Channel B Reference pulse R Reference enable switch ENR
Event Counter	
Signal Form	Square wave pulse
Input Frequency	100 kHz
Counter Size	2 x 16 Bit
Inputs Input 1 Input 2	 Counter 1 Counter 2
Outputs	
Number of Outputs	1
Operating Voltage Minimum Nominal Maximum	 18 VDC 24 VDC 30 VDC
Continuous Current	0.5 A
Maximum Switching Frequency	20 kHz with resistive load
Negative Anode Potential	45 V to 55 V
Diagnosis	Reverse polarity protection, short-circuit protection, software monitor status [1]
Electrical Isolation	Output - PCC
Mechanical Characteristics	
Dimensions	B&R 2003 screw-in module

[1] Incremental encoder operation: Module status in data word 0

Event Counter Operation: Module status in data word 2

7.6.2 Four Digital High Speed Inputs

All four inputs are sent to TPU. If the module is inserted e.g. in slot 1 of the CP interface on a CP474, input 1 can be evaluated using the LTX function LTXdi0().

Performance Characteristics

- Counting and measuring digital signals (internal measuring frequency 4 MHz)
- Gate measurement
- Frequency measurement
- Event counting
- Incremental encoder operation
- Reaction to input events in the μs range
- Local counter status monitoring with direct output control

7.6.3 24 V Incremental Encoder / Encoder Signal Evaluation

Inputs 1 and 2 correspond to encoder signals A and B. The encoder signal is generally processed using 4-fold evaluation. The scan time (count generation) is less than 1 ms, but respective hardware allows an input frequency of 50 kHz.

Position Description:

- 32 bit (Long) and status word including referencing bit (data consistency)

Local Referencing Support:

- Clear counter without conditions (directly after receiving command)
- Clear counter after receiving the reference pulse
- Clear counter after receiving the first reference pulse with active reference enable switch

Input 3 is used as a reference signal if required.

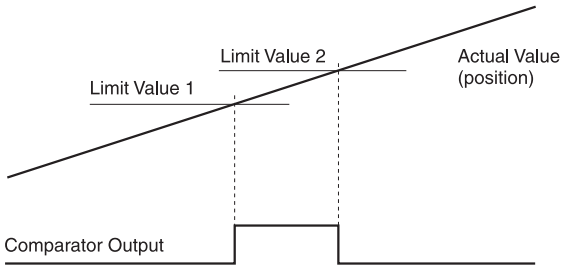
Input 4 is used as a reference enable switch if required.

7.6.4 Event Counter

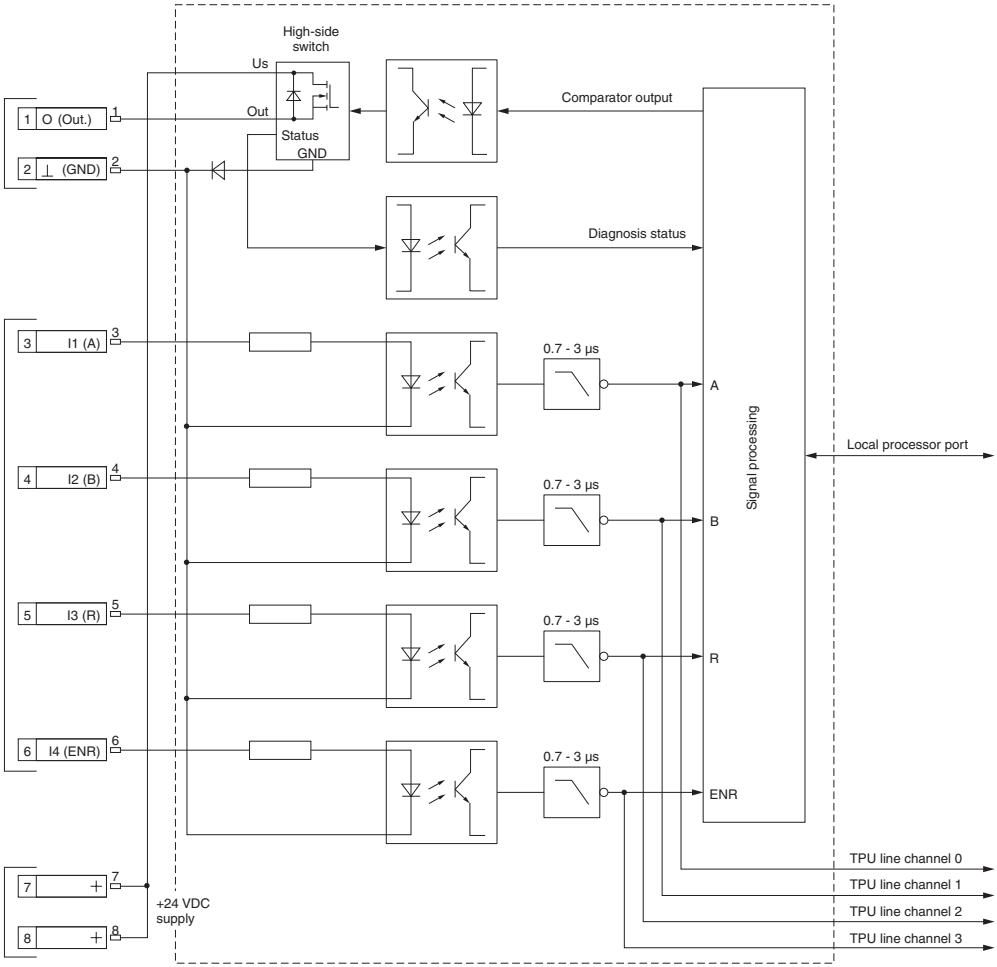
- 16-Bit counter, counts every rising edge or both edges on input 1
- 16-Bit counter, counts every rising edge or both edges on input 2
- The counters are cyclic (..., $FFFE, $FFFF, $0000, $0001, ...) and can be cleared separately on command

7.6.5 Comparator

Local counter status monitoring with direct output control (+24 VDC/0.5 A) and a reaction time of 500 µs. The comparator is either assigned to event counter 2 (16 Bit, Input 2) or to the position counter (encoder operation).



7.6.6 Input/Output Diagram



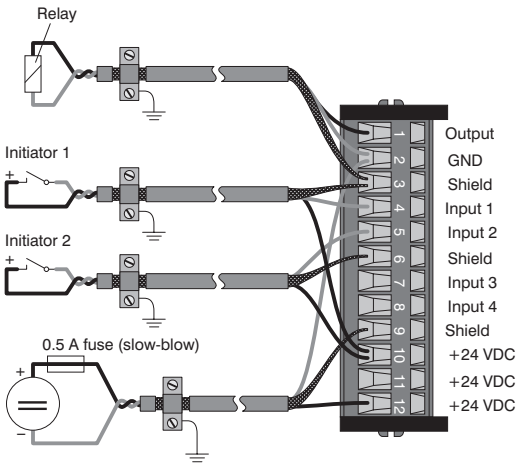
7.6.7 Connections

TB712

Pin	Assignment
1	Output (comparator)
2	GND
3	Shield
4	Input 1 (encoder signal A)
5	Input 2 (encoder signal B)
6	Shield
7	Input 3 (encoder signal R)
8	Input 4 (reference enable switch ENR)
9	Shield
10	+24 VDC for output or encoder
11	+24 VDC for output or encoder
12	+24 VDC for output or encoder

7.6.8 Connection Examples

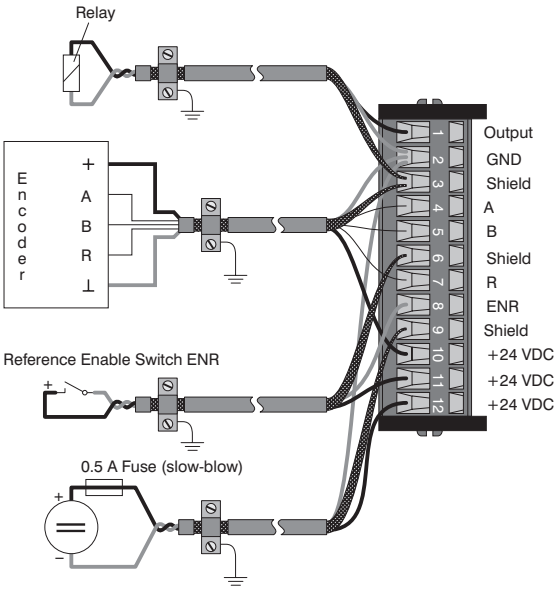
Wiring Example Inputs/Outputs



Supply:

+24 VDC, Protect with 0.5 A slow-blow fuse!

Wiring Example Incremental Encoder (encoder connection)



Supply:

+24 VDC, Protect with 0.5 A slow-blow fuse!

7.6.9 Variable Declaration for Incremental Encoder Operation

The variable declaration is valid for the following controllers:

- 2003 PCC CPU
- Remote I/O Bus Controller
- CAN Bus Controller

The variable declaration is made in PG2000. The variable declaration is described in Chapter 4, "Module Addressing".

Automation Studio™ Support: See Automation Studio™ Help starting with V 1.40

Accessing screw-in modules is also explained in the sections "AF101" and "CPU".

Incremental Encoder Operation with PCC 2003 and Remote Slaves

Data access takes place using data and configuration words. The following table provides an overview of which data and configuration words are used for this module.

Data Access	VD Data Type	VD Module Type	VD Chan.	R	W	Description
Data word 0	WORD	Transp. In	0	●		Module status
Data word 1	INT32	Transp. In	2	●		Counter value
Configuration word 4	INT32	Transp. In	8	●		Counter value at positive edge of the reference enable switch
	INT32	Transp. Out	8		●	Threshold value 1
Configuration word 6	INT32	Transp. In	12	●		Counter value at negative edge of the reference enable switch
	INT32	Transp. Out	12		●	Threshold value 2
Configuration word 8	WORD	Transp. Out	16		●	Incremental encoder / comparator control
Configuration word 12	WORD	Transp. In	24	●		Module status
Configuration word 14	WORD	Transp. In	28	●		Module type
	WORD	Transp. Out	28		●	Module configuration

Incremental Encoder Operation with CAN Slaves

Data access takes place using data and configuration words. The following table provides an overview of which data and configuration words are used for this module.

Data Access	VD Data Type	VD Module Type	VD Chan.	R	W	Description
Data word 0	INT32	Transp. In	0	●		Counter value
Data word 2	WORD	Transp. In	4	●		Module status
Configuration word 4	INT32	Transp. In	8	●		Counter value at positive edge of the reference enable switch
	INT32	Transp. Out	8		●	Threshold value 1
Configuration word 6	INT32	Transp. In	12	●		Counter value at negative edge of the reference enable switch
	INT32	Transp. Out	12		●	Threshold value 2
Configuration word 8	WORD	Transp. Out	16		●	Incremental encoder / comparator control
Configuration word 12	WORD	Transp. In	24	●		Module status
Configuration word 14	WORD	Transp. In	28	●		Module type
	WORD	Transp. Out	28		●	Module configuration

B&R 2000 users have to exchange the two counter status words so that the high word is first (Motorola format)!

Access using CAN Identifiers

Access via CAN Identifiers is used if the slave is being controlled by a device from another manufacturer. Access via CAN Identifiers is described in an example in Chapter 4, "Module Addressing".
The transfer modes are explained in Chapter 5, "CAN Bus Controller Functions".

Data cannot be packed on the DI135. Therefore one CAN object is transferred per screw-in module. If an adapter module AF101 is equipped with a four DI135 modules, the CAN object has the following structure:

Slot	CAN ID [1)]	Word 1		Word 2		Word 3		Word 4
1	542	Counter LL	Counter ML	Counter MH	Counter HH	Status L	Status H	free
2	543	Counter LL	Counter ML	Counter MH	Counter HH	Status L	Status H	free
3	544	Counter LL	Counter ML	Counter MH	Counter HH	Status L	Status H	free
4	545	Counter LL	Counter ML	Counter MH	Counter HH	Status L	Status H	free

[1)] CAN ID = 542 + (nd - 1) x 16 + (ma - 1) x 4 + (sl - 1)
nd ..... Node number of the CAN slave = 1
ma .... Module address of the AF101 = 1
sl ..... Slot number of the screw-in module on the AF101 (1 - 4)

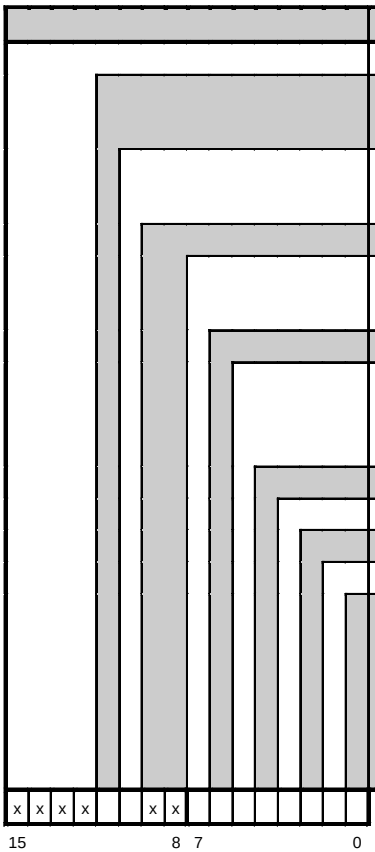
B&R 2000 users have to exchange the data so that the high data is first (Motorola format)!

For more information on ID allocation, see Chapter 5, "CAN Bus Controller Functions".

Description of Data and Configuration Words

Data Word 0 (read)

Data word 0 includes the module status time constant for the counter value.



Bit	Description
12 - 15	x ....not defined, masked out
11	0 ....Counter reading not accepted 1 ....Counter reading when the first positive edge arrives from Reference Enable Switch
10	0 ....Counter reading not accepted 1 ....Counter reading when the first negative edge arrives from the reference enable switch
8 - 9	x ....not defined, masked out
7	0 ....Referencing is in progress 1 ....Counter is referenced (reset occurs after receiving a reference command)
6	changes state after each successful reference
5	0 ....Comparator Output: No error 1 ....Comparator Output: An overload error can only be indicated when the comparator output is set.
4	Comparator output state
3	Level of the encoder input A
2	Level of the encoder input B
1	Level of the reference enable switch
0	1) Bit 0 in configurations word 14 = 0 Level of reference pulses 2) Bit 0 in configurations word 14 = 1 Level of the connection between reference pulse and reference enable switch Normal and inverted reference pulses must be differentiated. The change over for bit 2 occurs in configuration word 14 (refer to the explanation that follows).

Normal Reference Pulse:

Path/state and timing diagrams for incremental encoder operation are shown for the NC161 encoder module. These diagrams are also valid for the DI135.

Bit 0 in Data Word 0 is always 1 when the level of the reference enable switch is 0.
Bit 0 only takes the level of the reference pulse when the level of the reference enable switch is 1.

Bit 0 = Input 3 or (not Input 4)

Input 3 Reference Pulse	Input 4 Reference Enable Switch	Bit 0 Data Word 0
0	0	1
1	0	1
0	1	0
1	1	1

Inverted Reference Pulse:

Bit 0 in data word 0 is always 1 when the level of the reference enable switch is 0.
Bit 0 only takes the level of the inverted reference pulse when the state of the reference enable switch is 1.

Bit 0 = (not Input 3) or (not Input 4)

Input 3 Reference Pulse	Input 4 Reference Enable Switch	Bit 0 Data Word 0
0	0	1
1	0	1
0	1	1
1	1	0

Data Word 1 (read)

Counter Value MSW

Data Word 2 (read)

Counter Value LSW

Configuration Words 4+5 (read)

After setting bit 11 in configuration word 8, the configuration words receive the latched counter value with the first positive edge of the reference enable switch. The value is valid if bit 11 is set in data word 0. Please refer to the timing diagram "Latching the Counter Value" in section "NC161".

Configuration Words 4+5 (write)

Threshold value 1 (32 Bit)

Threshold value 1 must always be ≤ threshold value 2 .
Threshold values are internally arranged in increasing order **including sign**.

Configuration Words 6+7 (read)

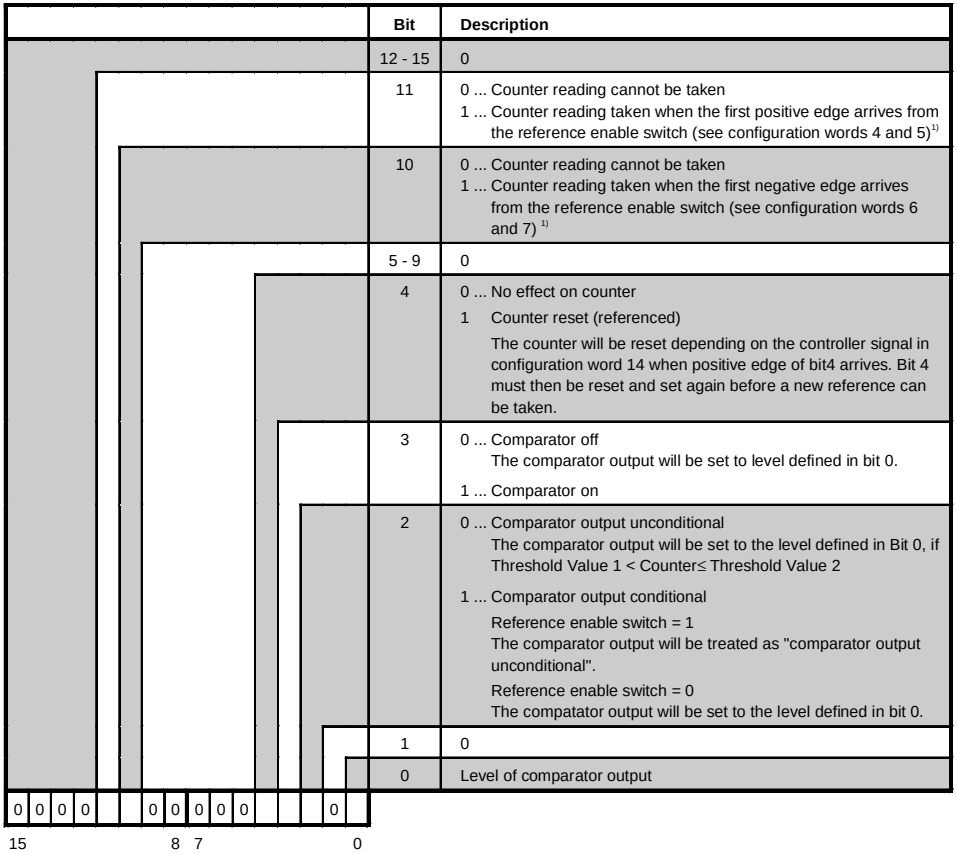
After setting bit 10 in configuration word 8, the configuration words receive the latched counter value with the first negative edge of the reference enable switch. The value is valid if bit 10 is set in data word 0. Please refer to the timing diagram "Latching the Counter Value" in section "NC161".

Configuration Words 6+7 (write)

Threshold value 2 (32 Bit)

Configuration Word 8 (write)

Incremental encoders and comparators are configured using configuration word 8.



Bit	Description
12 - 15	0
11	0 ... Counter reading cannot be taken 1 ... Counter reading taken when the first positive edge arrives from the reference enable switch (see configuration words 4 and 5)[1)]
10	0 ... Counter reading cannot be taken 1 ... Counter reading taken when the first negative edge arrives from the reference enable switch (see configuration words 6 and 7) [1)]
5 - 9	0
4	0 ... No effect on counter 1 Counter reset (referenced) The counter will be reset depending on the controller signal in configuration word 14 when positive edge of bit4 arrives. Bit 4 must then be reset and set again before a new reference can be taken.
3	0 ... Comparator off The comparator output will be set to level defined in bit 0. 1 ... Comparator on
2	0 ... Comparator output unconditional The comparator output will be set to the level defined in Bit 0, if Threshold Value 1 < Counter≤ Threshold Value 2 1 ... Comparator output conditional Reference enable switch = 1 The comparator output will be treated as "comparator output unconditional". Reference enable switch = 0 The compatator output will be set to the level defined in bit 0.
1	0
0	Level of comparator output

[1)] The counter value is only taken once. Bit 10 and bit 11 must be reset for the value to be taken again. Bit 10 and bit 11 can be set again in configuration word 8 after the corresponding bit in the module status bit has gone to 0.

Configuration Word 12 (read)

Configuration word 12 contains the module status (current status unlatched). The module status is written to data word 0.

Configuration Word 14 (read)

The High Byte of configuration word 14 defines the module code.

Bit	Description
8 - 15	Module code = $12
0 - 7	x.... Not defined, masked out

0	0	0	1	0	0	1	0	x	x	x	x	x	x	x	x
15								8	7						0

Configuration Word 14 (write)

The module is configured using configuration word 14.

Bit	Description
13 - 15	0
12	0 ... Incremental encoder operation 1 ... Event counter operation
6 - 11	0
5	0 ... No influence on counter direction 1 ... Reversed counter direction
3 - 4	0
2	0 ... No influence on reference pulse 1 ... Reference pulse is inverted. This change is used for encoders with high pulses.
1	0 ... Counter set immediately to 0. In data word 0 (module status), bit 7 is set directly to1 and the counter reset. 1 ... Counter continues to function. In data word 0 (module status) bit 7 is set directly to 0 (limited reference). If the reference pulse is recorded, bit 7 in data word 0 will be set to 1 depending on the status of bit 0 in configuration word 14, and reset again with a positive edge in configuration 14.
0	0 ... Reference enable switch ignored (referenced with reference pulse) 1 ... Reference enable switch activated (reference pulse and reference enable switch)

0	0	0	0	0	0	0	0	0		0	0			
15							8	7						0

Path/state and timing diagrams for incremental encoder operation are shown for the NC161 encoder module. These diagrams are also valid for the DI135.

7.6.10 Variable Declaration for Event Counter Operation

The variable declaration is valid for the following controllers:

- 2003 PCC CPU
- Remote I/O Bus Controller
- CAN Bus Controller

The variable declaration is made in PG2000. The variable declaration is described in Chapter 4, "Module Addressing".

Automation Studio™ Support: See Automation Studio™ Help starting with V 1.40

Accessing screw-in modules is also explained in the sections "AF101" and "CPU".

Event Counter Operation

Data access takes place using data and configuration words. The following table provides an overview of which data and configuration words are used for this module.

Data Access	VD Data Type	VD Module Type	VD Chan.	R	W	Description
Data word 0	WORD	Transp. In	0	●		Counter value of counter 2
Data word 1	WORD	Transp. In	2	●		Counter value of counter 1
Data word 2	WORD	Transp. In	4	●		Module status
Configuration word 4	WORD	Transp. In	8	●		Counter value of counter 1 at positive edge of the reference enable switch
Configuration word 5	WORD	Transp. In	10	●		Counter value of counter 2 at positive edge of the reference enable switch
	WORD	Transp. Out	10		●	Threshold value 1 for counter 2
Configuration word 6	WORD	Transp. In	12	●		Counter value of counter 1 at negative edge of the reference enable switch
Configuration word 7	WORD	Transp. In	14	●		Counter value of counter 2 at negative edge of the reference enable switch
	WORD	Transp. Out	14		●	Threshold value 2 for counter 2
Configuration word 8	WORD	Transp. Out	16		●	Counter / comparator control
Configuration word 12	WORD	Transp. In	24	●		Module status
Configuration word 14	WORD	Transp. In	28	●		Module type
	WORD	Transp. Out	28		●	Module configuration

Access using CAN Identifiers

Access via CAN Identifiers is used if the slave is being controlled by a device from another manufacturer. Access via CAN Identifiers is described in an example in Chapter 4, "Module Addressing". The transfer modes are explained in Chapter 5, "CAN Bus Controller Functions".

Data cannot be packed on the DI135. Therefore one CAN object is transferred per screw-in module. If an adapter module AF101 is equipped with a four DI135 modules, the CAN object has the following structure:

Slot	CAN ID [1]	Word 1		Word 2		Word 3		Word 4
1	542	Counter 2L	Counter 2H	Counter 1L	Counter 1H	Status L	Status H	free
2	543	Counter 2L	Counter 2H	Counter 1L	Counter 1H	Status L	Status H	free
3	544	Counter 2L	Counter 2H	Counter 1L	Counter 1H	Status L	Status H	free
4	545	Counter 2L	Counter 2H	Counter 1L	Counter 1H	Status L	Status H	free

[1] CAN ID = 542 + (nd - 1) x 16 + (ma - 1) x 4 + (sl - 1)

nd ..... Node number of the CAN slave = 1

ma .... Module address of the AF101 = 1

sl ..... Slot number of the screw-in module on the AF101 (1 - 4)

B&R 2000 users have to exchange the data so that the high data is first (Motorola format)!

For more information on ID allocation, see Chapter 5, "CAN Bus Controller Functions".

Description of Data and Configuration Words

Data Word 0 (read)

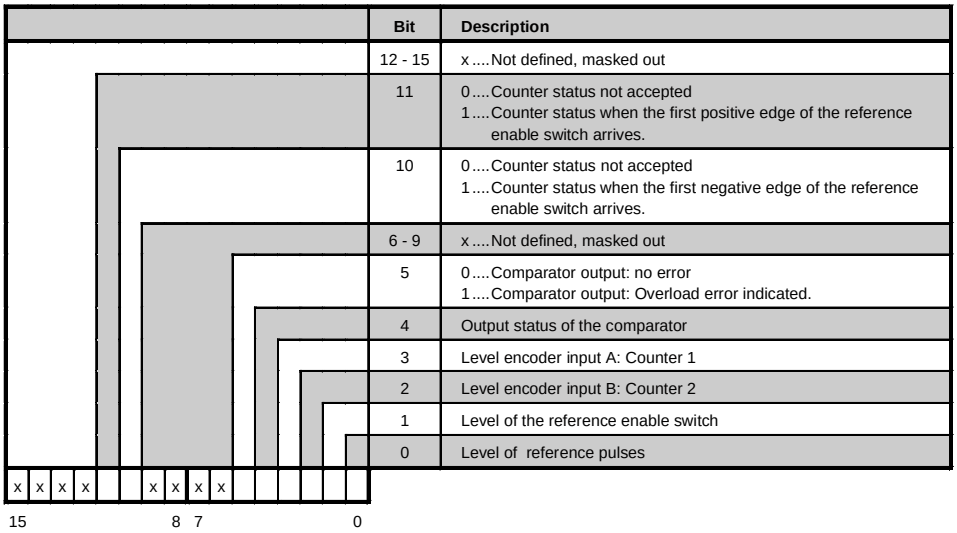
Counter value of counter 2.

Data Word 1 (read)

Counter value of counter 1.

Data Word 2 (read)

Data word 2 includes the module status time constant for both counter values.



Bit	Description
12 - 15	x ....Not defined, masked out
11	0 ....Counter status not accepted 1 ....Counter status when the first positive edge of the reference enable switch arrives.
10	0 ....Counter status not accepted 1 ....Counter status when the first negative edge of the reference enable switch arrives.
6 - 9	x ....Not defined, masked out
5	0 ....Comparator output: no error 1 ....Comparator output: Overload error indicated.
4	Output status of the comparator
3	Level encoder input A: Counter 1
2	Level encoder input B: Counter 2
1	Level of the reference enable switch
0	Level of reference pulses

Configuration Word 4 (read)

After setting bit 11 in configuration word 8, the configuration word receives the latched counter value of counter 1 with the first positive edge of the reference enable switch. The value is valid if bit 11 is set in data word 2.
Please refer to the timing diagram "Latching the Counter Value" in section "NC161".

Configuration Word 5 (read)

After setting bit 11 in configuration word 8, the configuration word receives the latched counter value of counter 2 with the first positive edge of the reference enable switch. The value is valid if bit 11 is set in data word 2.
Please refer to the timing diagram "Latching the Counter Value" in section "NC161".

Configuration Word 5 (write)

Threshold value 1 (16 Bit) for counter 2.

Threshold value 1 must always be ≤ threshold value 2 .
Threshold values are internally arranged in increasing order.

Configuration Word 6 (read)

After setting bit 10 in configuration word 8, the configuration word receives the latched counter value of counter 1 with the first negative edge of the reference enable switch. The value is valid if bit 10 is set in data word 2.
Please refer to the timing diagram "Latching the Counter Value" in section "NC161".

Configuration Word 7 (read)

After setting bit 10 in configuration word 8, the configuration word receives the latched counter value of counter 2 with the first negative edge of the reference enable switch. The value is valid if bit 10 is set in data word 2.
Please refer to the timing diagram "Latching the Counter Value" in section "NC161".

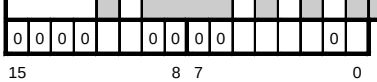
Configuration Word 7 (write)

Threshold value 2 (16 Bit) for counter 2.

Configuration Word 8 (write)

Event counters and comparators are configured using configuration word 8.

Bit	Description
12 - 15	0
11	0 .... Counter reading cannot be taken 1 .... Counter reading taken when the first positive edge arrives from the reference enable switch (see configuration words 4 and 5)
10	0 .... Counter reading cannot be taken 1 .... Counter reading taken when the first negative edge arrives from the reference enable switch (see configuration words 6 and 7)
6 - 9	0
5	0 .... No effect on counter 2 1 .... Reset counter 2 immediately
4	0 .... No effect on counter 1 1 .... reset counter 1 immediately
3	0 .... Comparator off The comparator output will be set to level defined in bit 0. 1 .... Comparator on
2	0 .... Comparator output unconditional The comparator output will be set to the level defined in Bit 0, if Threshold Value 1 < Counter≤ Threshold Value 2 1 .... Comparator output conditional Reference enable switch = 1 The comparator output will be treated as "comparator output unconditional". Reference enable switch = 0 The compatator output will be set to the level defined in bit 0.
1	0
0	Level of the comparator output



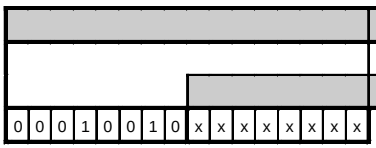
Configuration Word 12 (read)

Configuration word 12 contains the module status (current status unlatched). The module status is written to data word 0.

Configuration Word 14 (read)

The High Byte of configuration word 14 defines the module code.

Bit	Description
8 - 15	Module code = $12
0 - 7	x ....Not defined, masked out



Configuration Word 14 (write)

The module is configured using configuration word 14.

Bit	Description
13 - 15	0
12	0.... Encoder operation 1.... Event counter
6 - 11	0
5	0.... Normal count direction 1.... Reverse count direction
4	0
3	0.... Only count positive edges 1.... Count both edges
0 - 2	0