3.12 Class 8030 Type CRM-210, 211, 220, 222 Local/Remote Interface Modules

The SY/MAX Class 8030 Type CRM-210,211 Local Interface and CRM-220, 222 Remote Interface modules provide a method to remotely locate both digital and register I/O racks from a SY/MAX Model 300, 400, 500 or 700 Processor and to communicate in a serial fashion.

To establish a remote I/O system a Local Interface (LI) module is mounted in the rack containing the SY/MAX Processor and the Remote Interface (RI) module is mounted in the remote digital or register rack, referred to as a drop.

3.12.1 SPECIFICATIONS

ELECTRICAL

The CRM-210, 211, 220 and 222 are UL listed.

Current Draw on SY/MAX Power Supply ..... CRM-210, 211 = 1600 mA. CRM-220, 222 = 1000 mA.

CAPABILITIES

Local Interface Registers ..... CRM-210 contains 512 registers (255 for forcible external I/O, 257 for internal data storage*). CRM-211 contains 4096 registers (255 for forcible external I/O, 3841 for internal data storage*).

Local Interface Channels ..... 2 Channels per Local Interface, 255 registers for digital I/O per module. 8 drops per channel, max

Remote Drops ..... 127 registers per drop max.

Communications .... Continuous, full duplex, serial differential (RS-422) at 31.25K baud.

Drop Configuration .. Daisy Chain

*Unused external registers may also be used for internal data storage. All registers used for internal data storage are retentive.

Recommended Communication Cable Specifications

	BELDEN 8723	BELDEN 9463
Conductor-Conductor Capacitance	35 pF/ft.	19.7 pF/ft.
Wire Size	22 gauge	20 gauge
Conductors/Cable	4	2 (2Cables Required)
Recommended Maximum Distance	7500 ft. (2250 m.)	10,000 ft. (3048 m.)

Compatibility With Processors The LI/RI system is compatible with all Model 400, 500 and 700 processors. Models 500 and 700 support up to seven LIs while Model 300 can support one. The Model 300 processors in the following table are compatible.

PROCESSOR Type	PROCESSOR SERIES*	
	Without Control Functions**	With Control Functions**
SCP-311	E to F	G or later
SCP-312	E to F	G or later
SCP-313	D to F	G or later
SCP-321	D to F	G or later
SCP-322	D to F	G or later
SCP-323	C to F	G or later
SCP-332	D to F	G or later
SCP-333	D to F	G or later
SCP-344	C to F	G or later

**Processors with series designations earlier than these selected in Table 3.1 have local I/O capability only and can force only the first 16 registers while these listed processors can force the first 32 registers.*

***Control Functions Consist of:*

1. *Programmed Halting of Drops*
2. *Failure Override*
3. *Auto Restart upon Communications Loss*
4. *Freeze or Reset Outputs on Communications Loss*

TABLE 3.1 - Model 300 LI Compatibility

Compatibility With I/O ..... All 32, 16 and 8 function I/O, all 4 function input modules. Series B or later 4 point output modules. Register Modules: All compatible. Class 8030 Type CRM-115/ 116, Bus Driver/ Terminator Series ≥ D.

Compatibility With Racks ..... The CRM-210/211 is compatible with all racks except the CRK-100 and 200. The CRM-220 is compatible with all four function digital racks.

ENVIRONMENTAL

Ambient Temp. ..... Operational: 0°C-60°C (32°-140°F) Storage: -40°C-80°C (-40°- 176°F)

Humidity ..... 5% to 95% non-condensing

3.12.2 LI/RI LED INDICATORS

Each LI and RI has several diagnostic LEDs to simplify system troubleshooting. The LEDs indicate diagnostic information such as the status of the communication link, individual drop operation, and module operation.

LOCAL INTERFACE	
All lights OFF indicates loss of 5VDC power.	
RUN *(green)*	
ON-	Indicates LI is operational and CPU is accessing image table information.
OFF-	Indicates LI is in self-diagnostics or has failed.
FLASHING-	Indicates LI is running but one or more drops on its channels have been programmed to halt. (Controlled by bits 1-8 of the LI channel control register.)
HALT *(red)*	
ON-	Indicates LI is in self-diagnostics and/or has halted operation.
OFF-	Indicates LI is fully operational and CPU is accessing image table information.
FLASHING-	Indicates LI is running but one or more drops on its channels have been programmed to halt. (Bits 1-8 of the LI channel control register.)
CHANNEL ERROR *(red)*	
ON-	Indicates LI cannot communicate with one or more of its drops which are shutdown.
OFF-	Indicates all drops operational.
FLASHING-	Indicates a module failure on a drop has caused a drop to shutdown on this channel.
MODULE ERROR *(red)*	
ON-	Indicates a self diagnostic error or internal timeout error has been recognized and halted the CPU.
OFF-	Indicates LI is operational even though a channel HALT or CHANNEL ERROR LED may be ON.
FLASHING-	Not valid

Table 3.2 - LI LED Explanation

REMOTE INTERFACE	
All lights OFF indicates loss of 5VDC power.	
RUN *(green)*	
ON-	Indicates remote drop is operational.
OFF-	Indicates RI is shutdown or has not been initialized. Outputs will de-energize unless the shutdown is the result of a communication error and the Freeze function is also selected.
FLASHING-	Indicates CPU is in Disable Outputs mode. (50% ON, 50% OFF alternately with HALT LED.)
HALT *(red)*	
ON-	Indicates RI is shutdown. If the only LED ON, it indicates rack was shut down due to program control or has not been initialized .
OFF-	Indicates Remote drop is operational.
FLASHING-	Indicates CPU is in Disable Outputs mode. (50% ON, 50%OFF alternately with RUN LED.)
BLINKING-	Indicates LI HALT bit for the drop is set. (95% ON, 5% OFF, alternately with RUN LED.)
CHANNEL ERROR *(red)*	
ON-	Indicates invalid or loss of communications between RI and LI; HALT LED will also be ON.
OFF-	Indicates valid communication between RI and LI.
I/O ERROR *(red)*	
ON-	(HALT LED will also be on.) This condition indicates either: ▸ Read after write error to an output. ▸Error caused by a malfunctioning register module. ▸RI malfunction.
OFF-	Indicates RI is properly communicating with modules in same rack.
FLASHING-	Indicates outputs and inputs are frozen (ON or OFF).
MODULE ERROR *(red)*	
ON-	Indicates a self diagnostic error or internal timeout error has occurred.
OFF-	Indicates RI is operational although drop may be shutdown due to system shutdown or program control.
FLASHING-	Not valid

Table 3.3 - RI LED Explanation

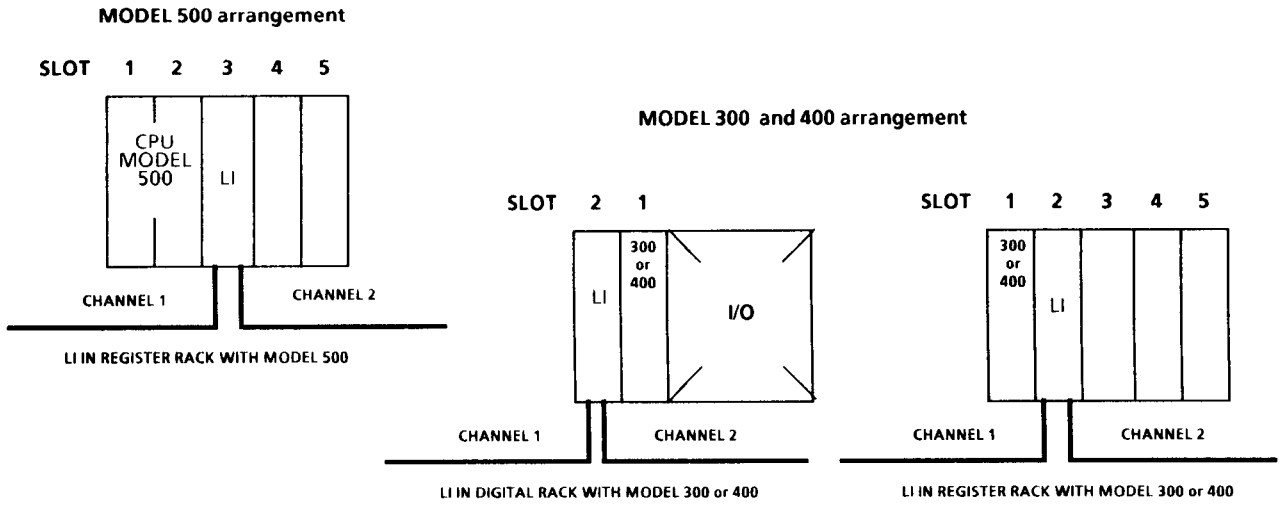


Figure 3.3 - Local Interface Location

3.12.3 MODULE LOCATION

3.12.3.1 Local Interface

The Local Interface module (LI) must be placed in the same rack assembly as the processor (CPU). When a register rack is used to house the CPU, we recommend the LI module be placed in the next closest slot. If more than one LI module is required, place additional modules in adjacent slots.

3.12.3.2 Remote Interface

The Remote Interface module (RI) must be placed in the CPU slot (slot #1) of any rack which is to be a drop. Only one RI is allowed for each drop.

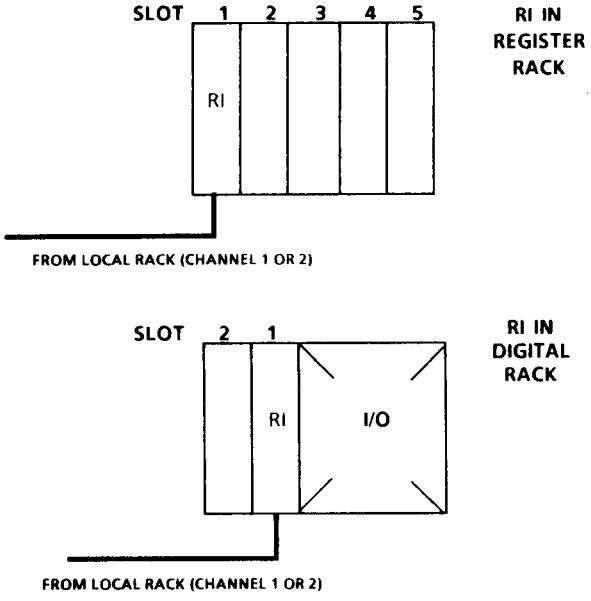


Figure 3.4 - Remote Interface Location

3.13.4 INSTALLATION IN A RACK ASSEMBLY

Power must be removed from the rack assembly before installing or removing the Local or Remote Interface Modules.

After the removal of power, release the latching clamp and insert the module into the appropriate register slot until firmly seated and aligned on the stud located above the socket for the slot. Close the latching clamp and be sure to tighten the captive screw to insure the module is secured and properly grounded. To remove the module, first remove power; then release the latching clamp, loosen the captive screw at the bottom and pull the module out of the slot using the finger tab located on the top of the module.

Note: Refer to Section 8.0 for proper grounding procedures.

3.12.5 FIELD WIRING

3.12.5.1 Power Connection

No external power wiring is required. The LI and RI modules receive their power through the edge connector socket of the rack assembly. Insert the LI module in the register slot until firmly seated and aligned on the stud (the middle post above the socket in that slot) and tighten the captive mounting screw at the bottom of the module. These two connections not only provide support for the module but also provide a ground.

3.12.5.2 Communication Cable

The communication between the LI and RI modules is achieved via a dual shielded twisted pair cable. In order to minimize the potential of electrical interference:

1. Route communication cable in different wire ducts (enclosed metal ducts) than the power wiring is routed.
2. Connect each end of the communications cable shield to the shield terminal on each module. Do not connect this shield to an external ground point since the SHIELD terminals are capacitively coupled to ground.

Transmission cable should be electrically equivalent to:

CABLE TYPE	MAXIMUM LENGTH	CONDUCTOR-CONDUCTOR CAPACITANCE
Belden 8723	7,500 feet 2250 meters	35 pf/ft.
Belden 9463*	10,000 feet 3048 meters	19.7 pf/ft.

*Dual cables required.

Table 3.4 - Recommended Cable Distance

Note: *ADDITIONAL DATA LINE PROTECTION*
In environments where lightning or induced transients over communication lines are likely to cause hardware failures, signal line protection devices are recommended. Even though transient protection is designed into SY/MAX communication circuits, additional specialized protection devices are suggested in areas where there is a high probability of secondary lightning strikes occurring. The specific environments which are of greatest concern are communication cable runs in the outside environment. Refer to Section 8 on Installation, Additional Data Line Protection, for recommended wiring and protection devices.

3.13.5.3 Local/Remote Interface Connections

The wiring method from one module to the next must be in daisy chain configuration. A branch may contain up to 8 drops per LI channel. The total allowable cable distance for each channel when using Belden 8723 cabling is 7500 feet (see Table 3.4). Always connect the shield wire to the shield terminals.

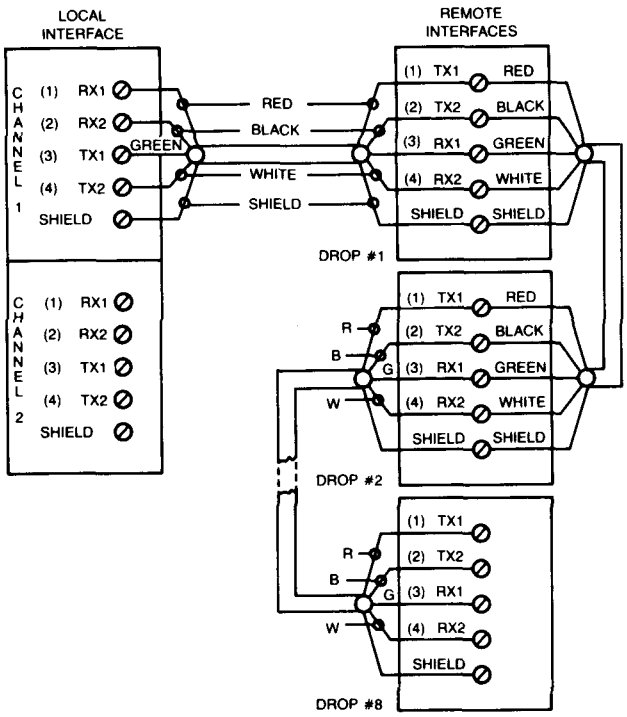
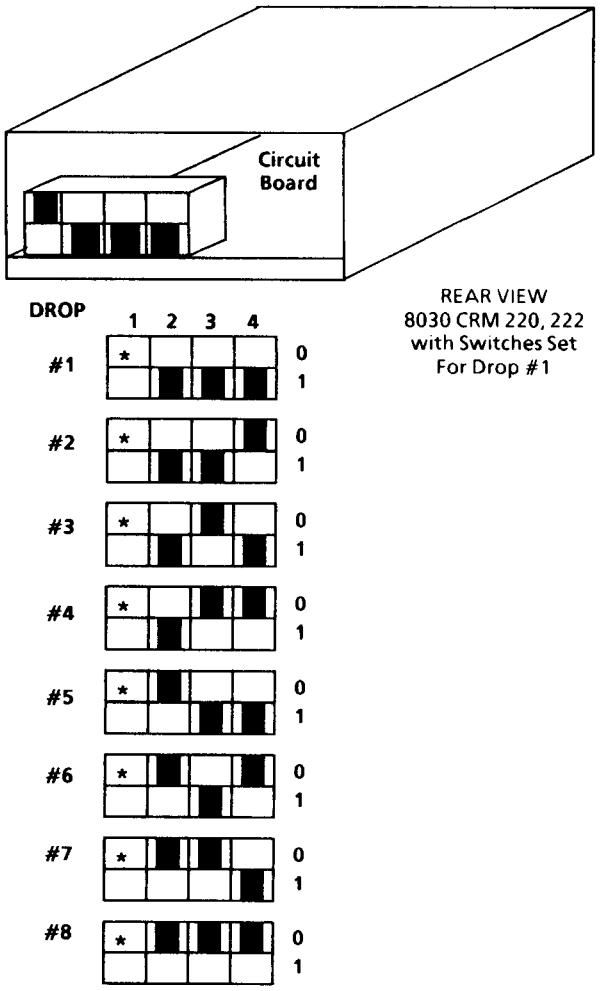


Figure 3.5 - LI/RI Wiring Connections

3.12.6 *RI DIP SWITCH SETTINGS*

The RI Module has four dip switches on the rear of the module near the edge of the circuit board. A module must be assigned as one of the eight drops on a specific channel. The switches must be set for the system to operate properly.

Set the switches for the appropriate drop as shown in Figure 3.6 - RI switch settings.



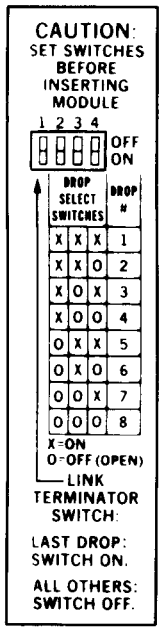
* For each channel, the drop (RI module) farthest from the LI must have switch 1 set ON, to a (1). Only one drop per channel requires this switch to be set. Failure to do so will result in a more noise susceptible communications link.

Figure 3.6 - RI Switch Settings

Label terminology may vary. The following equivalent terms are used:

0	O	UP	OPEN	OFF
1	X	DOWN	CLOSED	ON

Either one of these labels will be located on the side of the RI module.



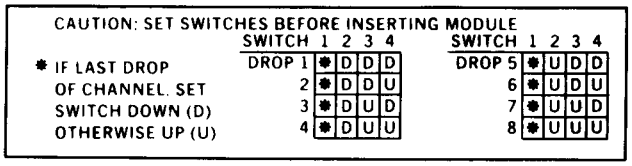


Figure 3.7 - RI Module Labels

3.12.7 LI/RI POWER-UP SEQUENCE

The following describes the power-up sequence for the LI/RI system.

3.12.7.1 LI Light Sequence

The following sequence of events occurs when the LI is energized, or the processor keyswitch goes from HALT to RUN or DISABLE OUTPUTS:

1. The MODULE ERROR LED blinks ON, OFF, ON, OFF, and remains OFF if no detected error* exists within the LI.
2. The CHANNEL ERROR and HALT LEDs are ON and turn OFF when all the self-diagnostic routines are completed.
3. The green channel RUN LED will turn ON when the LI is communicating.

*The MODULE ERROR LED will turn ON if this module has initiated a rack error condition, thus halting the system when:

1. A self-diagnostic error occurs.
2. Missing defined racks are detected (unless the Failure Override Bit is ON (=1).
3. An illegal rack addressing map is detected.

3.12.7.2 RI Light Sequence

The following sequence of events occurs when the RI is energized:

1. All red LEDs turn ON and then OFF.
2. The red HALT LED will turn OFF when the green RUN LED turns ON.
3. The green RUN LED turns ON when the RI is communicating to its rack assembly and the CPU is in Run or Disabled Outputs.

When the processor keyswitch goes from HALT to RUN or DISABLE OUTPUTS, only steps 2 and 3 occur.

The MODULE ERROR LED will remain ON only when a self-diagnostic error is detected.

3.12.7.3 LI/RI Initialization

1. When power is applied, self-diagnostic routines are initiated and verified within the LI, RI, CPU, and other register modules. Completion of the self-diagnostics insures that these modules are operational.
2. The LI then verifies communications with all of its drops.
3. The CPU will initiate the loading of the user defined rack addressing map into the LI.

If valid LI/RI communications cannot be established, an error is generated by the LI module. This error will halt the processor unless the failure override bit of that LI channel control register has been set ON (1).

Special Note: When initially keyswitching the processor from HALT to DISABLE OUTPUTS or RUN, a processor that has a new "out of the box" LI installed will remain in HALT and the LI will indicate a MODULE ERROR. The processor error register (8175) will identify the LI in error, and the LI error register will contain error code 901. This is a normal occurrence, reflecting the fact that the LI storage registers are corrupt (contain random data). Keyswitching the processor from HALT to DISABLE OUTPUTS or RUN a second (or third) time will clear the error.

3.13 Class 8030 Type CRM-230,232 Local and Remote Transfer Interface Modules

The SY/MAX Transfer Interface System enables redundant SY/MAX Model 400, 500≥M or 700≥C Processors to control a common I/O system. The system will transfer control of the I/O system to a backup processor should the primary shut down for any reason. I/O communication occurs in serial fashion.

A SY/MAX Transfer Interface System consist of two or more Class 8030 Type CRM-230 Local Transfer Interface (LTI) Modules and one or more Class 8030 Type CRM-232 Remote Transfer Interface (RTI) Modules.

3.13.1 TRANSFER INTERFACE SYSTEM SPECIFICATIONS

ELECTRICAL

Rated Current Draw On SY/MAX Power Supply	CRM-230: 1600 mA CRM-232: 1000 mA

CAPABILITIES

Registers (CRM-230)	4096 (255 for external drop addressing, 3841 for internal data storage)
I/O Channel	1 I/O Channel per LTI 255 Registers maximum 1024 Digital I/O max. (2048 if 24VDC) 8 Drops maximum
Drops	128 Digital I/O maximum (256 if 24VDC) 127 Registers per drop maximum
Register Transfer Channel	1 Register Transfer Channel per LTI. 32 Registers transferable per scan. Up to 4096 Registers transferable upon system startup
Communication Method	Continuous full duplex serial (RS422A)
Transmission Rate I/O Channel	62.5K baud
Transmission Rate Register Transfer Channel	375K baud
Transmission Distance I/O Channel	2500 feet (762 meters)
Transmission Distance Register Transfer Channel	25 feet (7.62 meters)
Compatibility With Racks	All racks
Compatibility With Processors	The Transfer Interface System is compatible with the Model 400, the Model 500 (Series M or later) and the Model 700 (Series C or later) processors. The Transfer Interface System is *not* compatible with Model 300 processors.

ENVIRONMENTAL

Ambient Temp.	0 to 60°C
Storage Temp.	-40 to 80°C
Humidity	5 to 95% non-condensing

3.13.2 LTI/RTI LED INDICATORS

The Local and Remote Interface Modules have the following LED indicators:

LOCAL TRANSFER INTERFACE	REMOTE TRANSFER INTERFACE
RUN (*green*)	RUN (*green*)
HALT (*red*)	HALT (*red*)
CHANNEL ERROR (*red*)	CHANNEL ERROR (*red*)
PRIMARY (*green*)	PRIMARY (*green*)
BACKUP (*green*)	MODULE ERROR (*red*)
RTC ERROR (*red*)	CPU A (*green*)
MODULE ERROR (*red*)	CPU B (*green*)

Note that when the Transfer Interface System is powered up and operating with a backup in RUN synchronized with the Primary (bumpless transfer mode), the LED indicators will be displayed as follows:

LTI - RUN and either PRIMARY or BACKUP steady ON.

RTI - RUN and either CPU A or CPU B steady ON, with complement (CPU A or CPU B) flashing ON and OFF.

The LED functions for both the Local and Remote Transfer Interfaces are shown on the following page in Tables 3.5 and 3.6 respectively.

Table 3.5 - Local Transfer Interface LED Functions

Name	Color	Function
RUN	GREEN	When ON indicates the I/O channel is fully operational and the CPU is accessing the image table (note CPU need not be in RUN). When OFF indicates the module is either in self-diagnostics or has failed. When flashing (50% duty cycle) indicates that one or more drops have been programmed to halt (bits 1 through 8 of the LTI I/O channel control register).
HALT	RED	The complement of the RUN LED.
CHANNEL ERROR	RED	When ON indicates one or more drops are shut down due to a communication problem. When OFF indicates all drop are operational. When flashing indicates that a drop has shut down due to a failure on the drop (typically a remote bus error).
PRIMARY	GREEN	When ON indicates the LTI is in Primary status. When flashing (50% duty cycle) indicates a Backup which is not able to become Primary. When blinking (10% duty cycle) indicates a Backup in "bump transfer" mode.
BACKUP	GREEN	The complement of the primary LED with the exception of a 90% duty cycle to indicate a backup in "bump transfer" mode.
RTC ERROR	RED	When ON indicates the RTC is not receiving communication. When OFF the RTC is fully operational. When flashing, indicates the RTC is receiving data but the other RTC is not.
MODULE	RED	When ON indicates the LTI has recognized a bus error and has halted the CPU. Note this does not necessarily mean the LTI itself is bad. When OFF indicates the LTI itself is operational, despite the possibility that other LTI error LEDs may be ON.

Table 3.6 - Remote Transfer Interface LED Functions

Name	Color	Function
RUN	GREEN	When ON indicates the drop has been initialized and is operating normally. When flashing (50% duty cycle) indicates the CPU is in DISABLE OUTPUTS. When blinking (10% duty cycle) indicates that the LTI halt bit has been set for that drop.
HALT	RED	When ON indicates that the drop either has not initialized or has been shut down due to program control. When flashing (50% duty cycle) indicates the CPU is in DISABLE OUTPUTS. When blinking (90% duty cycle) indicates that the LTI halt bit has been set for that drop.
CHANNEL ERROR	RED	When ON indicates a communication problem with the LTI. When flashing indicates a Primary is present but that no communication has been established with the Backup.
I/O ERROR	RED	When ON indicates a problem has been detected on the remote rack (not necessarily an RTI failure). When flashing indicates outputs on the drop have been FROZEN.
MODULE	RED	When ON indicates a self-diagnostic error. If error is transient, power-cycling the drop will allow recovery.
CPU A	GREEN	When ON indicates CPU A is Primary. When flashing (50% duty cycle) indicates CPU A is in ready Backup status. When OFF indicates CPU A is neither Primary nor a ready Backup.
CPU B	GREEN	Same conditions as CPU A LED except applied to CPU B.

3.13.3 MODULE LOCATION

3.13.3.1 Local Transfer Interface

The Local Transfer Interface (LTI) module must be placed in the same rack as the Model 400, 500 or 700 processor. The first LTI in a Transfer Interface system should be placed in the third slot of the register rack, though any slot is acceptable. Additional LTIs are placed in adjacent register slots.

3.13.3.2 Remote Transfer Interface

The Remote Transfer Interface (RTI) module must be placed into the CPU slot (slot #1) of any rack which is to be a drop. Only one RTI is allowed for each drop.

3.13.4 INSTALLATION IN RACK ASSEMBLY

Power must be removed from the rack assembly before installing or removing the Local or Remote Transfer Interface Modules.

After the removal of power, release the latching clamp and insert the module into the appropriate register slot until firmly seated and aligned on the stud located above the socket for the slot. Close the latching clamp and be sure to tighten the captive screw to insure the module is secured and properly grounded. To remove the module, release the latching clamp, loosen the captive screw at the bottom and pull the module out of the slot using the finger tab located on the top of the module.

Note: Refer to Section 8.0 for proper grounding procedures.

3.13.5 FIELD WIRING

3.13.5.1 I/O Channel Configuration

The LTIs I/O Channel must be wired in a daisy chain configuration to the RTI modules. Figure 3.9 illustrates this typical configuration. *A "star" wiring configuration is not allowed anywhere along the I/O channel.*

Note that all LTIs in the CPU rack selected as 'CPU A' must be connected to the 'CPU A' channel of the RTIs. Likewise, LTIs in 'CPU B' rack must be connected to the 'CPU B' channel of the RTIs. There can be no intermixing: wiring from 'CPU A' RTIs must not be connected to any of the 'CPU B' RTI terminals and vice versa.

Note: 'CPU A' and 'CPU B' terminals must be wired consistently for each drop (A to A and B to B). Otherwise the RTI will generate error code 29510 and not go to RUN, regardless of the state of the I/O Failure Override bit.

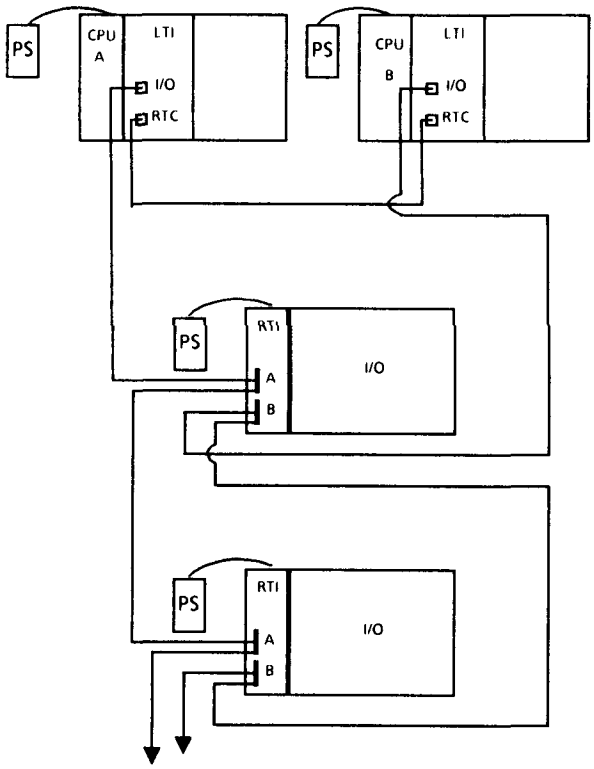


Figure 3.9 - I/O Channel Wiring Configuration

3.13.5.2 Communication Cable

The communication between modules of a Transfer Interface System takes place via a two pair, twisted, shielded cable. In order to minimize the potential of electrical interference:

1. Route communication cable in separate, enclosed, metal wire ducts, away from power wiring and electro-magnetic devices.
2. Connect each end of the communication cable shield to the SHD terminal on each device. *Do not connect this shield to an external ground point since the SHD terminals are capacitively coupled to ground.*

Follow all applicable electrical codes for wiring and communication cable routing.

Communication cable should be equivalent to Belden 8723. Using a cable with different specifications may cause unreliable operation.

The maximum communication distance for the *Belden 8723 or equivalent cable is as follows:*

Communication Channel	Maximum Length
I/O Channel	2500 feet (762 m.)
Register Transfer Channel	25 feet (7.6 m.)

Because the Transfer Interface System uses redundant LTI-to-RTI communication cables, it is possible (and desirable) to route the two cables separately or in different wire ducts. This practice will minimize the chances of both communication cables being broken or damaged simultaneously.

NOTE:
(ADDITIONAL DATA LINE PROTECTION)

In environments where lightning or induced transients over communication lines are likely to cause communication failures, signal line protection devices are recommended. Even though transient protection is designed into SY/MAX communication *circuits, additional specialized protection devices are* suggested for communication lines that are exposed to the outside environment. Refer to Section 8 for recommended wiring scheme and protection devices.

Authoritative reference material which discusses the art and science of noise reduction and data line protection includes the ANSI/IEEE Std. 518 as well as a book entitled *Noise Reduction Techniques in Electronic Systems* by Henry Ott (Wiley-Interscience 1976).

3.13.5.3 LTI/RTI Connections

There are five terminals on the LTI and RTI modules for each communication link connection. These terminals are labeled 1, 2, 3, 4, and SHD.

The twisted-pair continuity of the communication cables must be maintained in the communication links (for example, Black with Red and Green with White for Belden 8723 cable). The RTC communication link for each pair of LTI modules are connected together as in Figure 3.10. This distance is restricted to a maximum of 25 feet.

***Note:** For the RTC communication link the wiring crisscrosses; terminals 1 and 2 of one LTI connect to terminals 3 and 4 of its matched LTI, and vice versa.

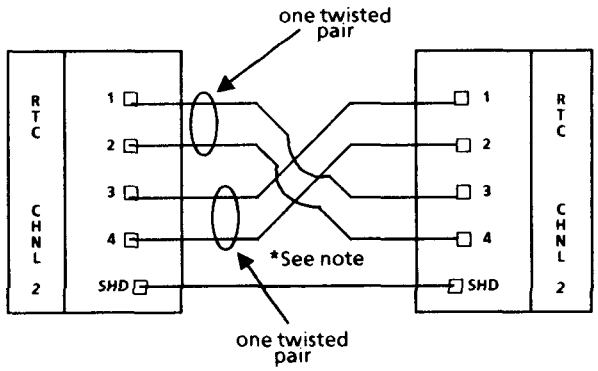


Figure 3.10 - RTC Channel: LTI-to-LTI Connections

The I/O communication link between the LTIs and RTIs *is wired as shown in Figure 3.11. A maximum* of two communication wires should be connected to each RTI terminal since each RTI in the daisy chain should be wired to the next RTI "straight through."

Note that for the I/O communication link, the wiring is straight through; there is no crisscrossing.

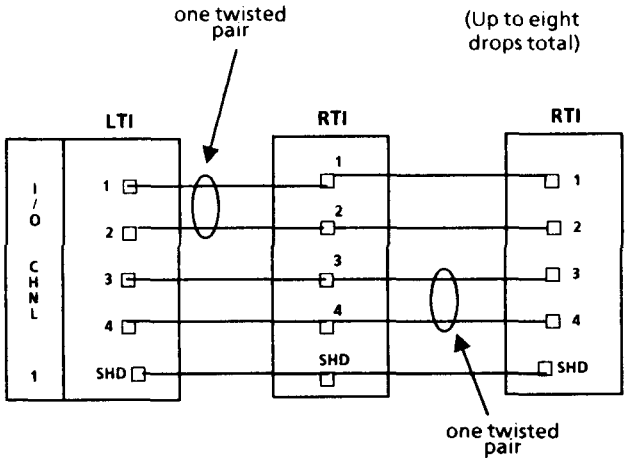


Figure 3.11 - I/O Channel: LTI-to-RTI Connections

3.13.6 RTI DIP SWITCHES

The RTI module has six dip switches on the rear of the module near the edge of the circuit board. See Figure 3.12. Each RTI module must be assigned as one of the eight drops on the LTI I/O Channel. The switches must be set correctly for the system to operate properly. See the following section on RTI DIP switch settings. Also, terminator switches must be set (ON) for the farthest drop of the channel. A label on the side of the module describes the switch settings. See Figure 3.13.

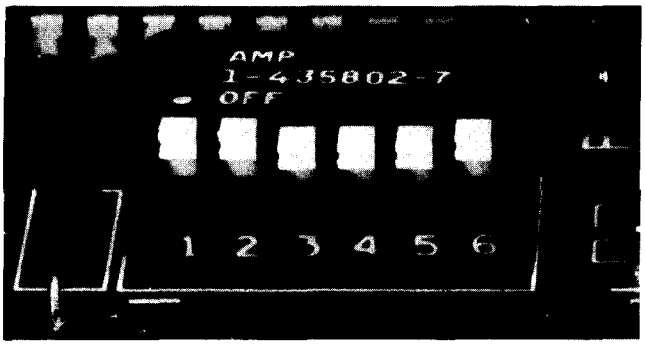


Figure 3.12 - RTI DIP Switches

3.13.6.1 Setting the RTI DIP Switches

Before putting an RTI into a rack assembly, set the DIP switches for correct operation. The bank of six switches is accessible from the rear of the module. The switches are ON when they are set towards the PC board.

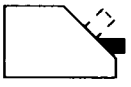
Switches 3,4 and 5 should be set according to the label on the RTI module (Figure 3.13) to specify the drop number of the rack on the I/O Channel.

Switches 1 and 2 are terminators which must be properly set to minimize the electrical interference on the communications link. For each LTI I/O Channel, the last RTI on the channel (the unit farthest along the link from the LTI) must have the terminator switch ON. Note that because the I/O Channel is redundantly controlled, it is possible to use different wire routing from processor A and from processor B. Therefore, there are two terminator switches on the RTI - one for processor A (switch 2) and one for processor B (switch 1). All other RTIs on the channel must have the terminator switches OFF.

Note: Switch 6 is not used.

NOTICE: FOR PROPER OPERATION SWITCHES MUST BE SET CORRECTLY BEFORE INSERTING MODULE

OFF
ON
1 2 3 4 5 6



DROP NO.	TERM B	TERM A	DROP SELECT			
1	▲	▲	X	X	X	✱
2	▲	▲	X	X	0	✱
3	▲	▲	X	0	X	✱
4	▲	▲	X	0	0	✱
5	▲	▲	0	X	X	✱
6	▲	▲	0	X	0	✱
7	▲	▲	0	0	X	✱
8	▲	▲	0	0	0	✱

X=ON-CLOSED-DWN
0=OFF-OPEN-UP
✱ =NOT USED

▲ TERMINATOR SWITCHES:

A = CPU A CHNL.
B = CPU B CHNL.

SET SWITCH ON FOR DROP AT END OF EACH DAISY CHAIN. ALL OTHER TERMINATOR SWITCHES OFF.

30608-406-01

Figure 3.13 - RTI DIP Switch Label

WARNING

Before operating the Transfer Interface System, be sure that all RTI DIP switches are set properly. Improper switch settings will cause unpredictable system operation and personal injury or property damage may result from unanticipated output actuation.

3.13.7 POWER UP SEQUENCE

Once the processors have "rack addressing" and ladder programs loaded into them, the Power Up Sequence can be initiated. The user is advised to perform the power up sequence as described below, to insure correct initialization of the Transfer Interface System (TIS). Along with insuring correct initialization this sequence will determine the Primary/Backup status of the system.

In the following sequence the user will power up the processors separately and check them out by observing the status of the LED indicators, and then put both processors in operation for redundant control.

Special Note: When initially keyswitching the processor from HALT to DISABLE OUTPUTS or RUN, a processor that has a new "out of the box" LTI installed will remain in HALT and the LTI will indicate a MODULE ERROR. The processor error register (8175) will identify the LTI in error, and the LTI error register will contain error code 901. This is a normal occurrence, reflecting the fact that the LTI storage registers are corrupt (contain random data). Keyswitching the processor from HALT to DISABLE OUTPUTS or RUN a second (or third) time will clear the error.

Proceed with the Power Up Sequence:

1. With both processors powered down, power up the processor that will be designated Backup, and keyswitch it to DISABLE OUTPUTS. Verify, by the status of the LED indicators shown in Figure 3.14, that the unit is operating correctly. Note that when switching processors from one state to another the LED indicators will momentarily change states before stabilizing.

   If an LED display other than that indicated in Figure 3.14 occurs, refer to the Special Note above. If trouble persists, refer to Troubleshooting Section 3.15.4.

2. Once the unit is operating correctly in DISABLE OUTPUTS, the unit can be further verified to be operating correctly by keyswitching it to RUN. Be reminded that when the processor is in RUN, it controls external I/O via the ladder program.

The correct LED indication when the unit is in RUN is shown in Figure 3.15.

PROCESSOR	LTIs	RTIs
RUN - *flashing*	**RUN** - ON ***PRIMARY*** - ON **RTC ERROR** - ON	**RUN** - flashing ***HALT*** - *flashing* **CHNL ERROR** - flashing **CPU A** or **B** - ON

Figure 3.14 - DISABLE OUTPUTS LED Display

PROCESSOR	LTIs	RTIs
RUN - ON	**RUN** - ON **PRIMARY** - ON **RTC ERROR** - ON	**RUN** - ON **HALT** - OFF **CHNL ERROR** - flashing **CPU A** or **B** - ON

Figure 3.15 - RUN LED Display

3. Once the unit designated to be Backup is operating properly, power it down in preparation for the succeeding steps.
4. With the processor designated to be Backup powered down, apply power to the processor to be designated Primary, then keyswitch it to DISABLE OUTPUTS. As before, verify by the status of the LED indicators shown in Figure 3.14, that the unit is operating correctly.

   If an LED display other than indicated in Figure 3.14 occurs, refer to the Special Note on the previous page. If trouble persists, refer to the Troubleshooting Section 3.15.4.
5. Once the unit is operating correctly in DISABLE OUTPUTS, keyswitch it to RUN and verify by the status of the LED indicators, shown in Figure 3.15 that the unit is operating correctly.
6. After the processor designated to be the Primary is operating correctly in RUN, leave it powered up and in RUN in preparation for the following steps.
7. With the Primary in RUN (for at least 10 seconds), apply power to the Backup and keyswitch it to RUN. If the Register Transfer Channel communication link is connected and operating correctly, the "RTC ERROR" LED on the Primary will turn OFF and the Backup will initialize and go into RUN. If the TIS is operating correctly there should be no ERROR indicators illuminated at this time; on the RTIs, CPU A or B will be ON steady with the complement CPU A or B flashing.
8. Now that the Transfer Interface System is up and running, a more comprehensive ladder program can be entered and appropriate control bits set to adapt the TIS to the particular user application.

3.13.8 TROUBLESHOOTING

In the power-up sequence the user verifies correct operation of the TIS by observing the status of the LED indicators. If the LED indications are not as illustrated in the power-up sequence, the user may refer to Section 3.13.2 (*LED Indicators*) and to Section 7.0 (Error Codes) for help.

It should be noted that the illustrated LED indications for the power-up sequence assume "rack addressing" matches existing external I/O. Some typical causes for the LED indications to be different than as illustrated in the power-up sequence are described below:

1. When initially keyswitching a processor that has a new "out of the box" LTI installed to DISABLE OUTPUTS or RUN, the processor will remain in HALT and the LTI will indicate a MODULE ERROR. The processor error register (8175) will identify the LTI in error, and the LTI error register (S8163 if the first LTI) will contain error code 901. This is a normal occurrence, reflecting the fact that the LTI storage registers are corrupt (contain random data). Keyswitching the processor from HALT to DISABLE OUTPUTS or RUN a second (or third) time will clear the error.
2. The I/O LED indicator on the processor will illuminate if "rack addressing" includes drops that don't actually exist, are not wired, or are not communicating for some reason. Also, on the affected LTIs the HALT, CHNL ERROR, and MODULE ERROR indicators will be ON. Interrogation of the error codes in Section 7.0 will reveal the drop in error.
3. The RTI HALT and CHNL ERROR LED indicators will remain ON steady, regardless of the keyswitch position of the processor, if the RTI is not communicating with the LTI (RTI not wired).
4. The RTI HALT, CHNL ERROR, and CPU A (or B) LED indicators will remain ON steady - regardless of the keyswitch position of the processor - if the RTI drop number is incorrect (for example, RTI DIP switch setting does not match an existing drop in "rack addressing").
5. Since these modules annunciate system errors that may actually originate in another module, error LEDs on the LTI or RTI themselves do not necessarily indicate a failure in these modules. If beset by erratic and seemingly contradictory indications, we suggest following a pattern which includes power-cycling all remote and CPU racks with the processor keyswitch in HALT. This should be followed by turning each of the processors to RUN, accompanied by the user recording error code information as described in Section 7.0. Useful information is contained in Register 8175 as well as the appropriate LTI error code registers (S8163, S8160, etc.). Registers 8183 and 8184 may also contain relevant information, depending on the nature of the failure.

3.14 LI/LTI CONTROL REGISTERS

Control Registers 8001-8163 (contained in the processor) are used to monitor and in some cases, control the Local/Remote Interface (LI/RI) system and/or Local/Remote (LTI/RTI) Transfer Interface System. These registers reflect the condition of the LI/RI and LTI/RTI system and contain information about registers and I /O modules.

Each control register consists of two parts, a DATA field and a STATUS field. The DATA field can be programmed by the user for control functions. The STATUS field, as the name implies, is used just to monitor the status of specific system conditions.

The Local Interface (LI) and Local Transfer Interface (LTI) control registers are dynamically assigned on the basis of physical position in the CPU rack and rack addressing assignments.

3.14.1 REGISTER ALLOCATION OF THE LOCAL INTERFACE SYSTEM (LI)

The Class 8030 Type CRM-210 and CRM-211 Local Interface modules (LI) are two- channel modules in which up to three control registers are used to communicate directly with the processor (CPU). The first register is an error code control register. The second is a control register for Channel 1 and the third is a control register for Channel 2, if used.

1. Local Interface Control registers are assigned in descending order starting with S8163 for the Local Interface module closest to the processor.

2. Local Interface Control register are further defined by the number of channels used.

For example, the local interface module closest to the processor would use control register 8163 as an error code register and use control register 8162 for Channel 1 and control register 8161 for Channel 2.

In the case where only one channel is assigned to the first LI, there will be no control registers assigned to Channel 2. S8163 is the error code control register. S8162 is the channel control register for Channel 1 and S8161 is left unassigned. If an additional LI is placed in a higher numbered CPU slot, it would be assigned the next available control register, for example, S8161 becomes the second LI's error code register, S8160 is the control register for Channel 1 of the second LI. S8159 is unassigned and available for Channel 2 or for the third LI's error code register. If only Channel 2 is defined, the system automatically assigns a control register to Channel 1 whether Channel 1 is used or not.

Figure 3.16 on the following page lists the error code and channel control registers for systems using both channels on each local interface module. This includes up to the maximum of seven local interface modules that can be used with a Model 500 or Model 700 processor system.

3.14.2 REGISTER ALLOCATION OF THE TRANSFER INTERFACE SYSTEM (TIS)

The 8030 CRM-230 Local Transfer Interface (LTI) is a two channel module which utilizes three registers to communicate directly with the processor (CPU). The first register is an error code register. The second is a control register for Channel 1 (I/O Channel). The third is a control register for Channel 2 (Register Transfer Channel-RTC). The number of control registers used to monitor a particular TIS is based on the number of LTI modules used in the system. Each matched pair of LTI modules uses three control registers.

LTI control registers are automatically assigned in descending order starting with S8163 for the LTI nearest the CPU with the lowest numbered CPU rack slot number. The first matched pair of LTI modules in a Transfer Interface System have register S8163 designated as their error code register. The I/O Channel (Channel 1) control register is S8162. The RTC (Channel 2) control register is S8161. Following the above sequence, S8160 would be the Error Code Register of the second LTI in the rack. See Figure 3.17 on the following page for LTI Control Register assignment.

REGISTER	L.I.	LOCATION	FUNCTION
S8163	First	(Right of	Error Code
S8162	First	CPU)	Channel 1 Control Data and Status
S8161	First*	↓	Channel 2 Control Data and Status
S8160	Second*	(Right of first LI	Error Code
S8159	Second*	module)	Channel 1 Control Data and Status
S8158	Second*	↓	Channel 2 Control Data and Status
S8157	Third*	(Right of second	Error Code
S8156	Third*	LI module)	Channel 1 Control Data and Status
S8155	Third*	↓	Channel 2 Control Data and Status
S8154	Fourth*	(Right of third	Error Code
S8153	Fourth*	LI module)	Channel 1 Control Data and Status
S8152	Fourth*	↓	Channel 2 Control Data and Status
S8151	Fifth*	(Right of fourth	Error Code
S8150	Fifth*	LI module)	Channel 1 Control Data and Status
S8149	Fifth*	↓	Channel 2 Control Data and Status
S8148	Sixth*	(Right of fifth LI	Error Code
S8147	Sixth*	module)	Channel 1 Control Data and Status
S8146	Sixth*	↓	Channel 2 Control Data and Status
S8145	Seventh*	(Right of sixth	Error Code
S8144	Seventh*	LI module)	Channel 1 Control Data and Status
S8143	Seventh*	↓	Channel 2 Control Data and Status

* Indicated LI register assignments may vary, dependent upon rack addressing assignments. Control registers are dynamically assigned in accordance with rack addressing and further defined by the number of channels used. They are not assigned solely based upon LI count.

Figure 3.16 - LI Control Register Assignments

REGISTER	LTI	LOCATION	FUNCTION
S8163	First	(Right of	Error Code
S8162	First	CPU)	I/O Channel 1 Control Data and Status
S8161	First	↓	RTC Channel 2 Control Data and Status
S8160	Second	(Right of first	Error Code
S8159	Second	LTI module)	I/O Channel 1 Control Data and Status
S8158	Second	↓	RTC Channel 2 Control Data and Status
S8157	Third	(Right of second	Error Code
S8156	Third	LTI module)	I/O Channel 1 Control Data and Status
S8155	Third	↓	RTC Channel 2 Control Data and Status
S8154	Fourth	(Right of third	Error Code
S8153	Fourth	LTI module)	I/O Channel 1 Control Data and Status
S8152	Fourth	↓	RTC Channel 2 Control Data and Status
S8151	Fifth	(Right of fourth	Error Code
S8150	Fifth	LTI module)	I/O Channel 1 Control Data and Status
S8149	Fifth	↓	RTC Channel 2 Control Data and Status
S8148	Sixth	(Right of fifth	Error Code
S8147	Sixth	LTI module)	I/O Channel 1 Control Data and Status
S8146	Sixth	↓	RTC Channel 2 Control Data and Status
S8145	Seventh	(Right of sixth	Error Code
S8144	Seventh	LTI module)	I/O Channel 1 Control Data and Status
S8143	Seventh	↓	RTC Channel 2 Control Data and Status

Figure 3.17 - LTI Control Register Assignments

3.14.3 REGISTER INFORMATION

3.14.3.1 Error Code Control Register

The LI/LTI error code register is the first of the group of registers allocated to an LI/LTI. It is this register which provides diagnostic information in the event an LI/LTI, RI/RTI register card, or I/O module experience a failure. If a device in the serial interface system causes the PC system to shutdown, control register 8175 will indicate which LI/LTI is responsible (by register address number) for the control of that device. The particular LI error code control register can then be examined to further diagnose the error. In general, errors indicated in S8175 refer to CPU and LI/LTI module problems or local register module problems, while errors indicated in the LI/LTI error code control registers refer to problems between the LI/LTI module and RI/RTI module, remote register module or I/O module. Error codes which are displayed in the LI/LTI error code register as decimal numbers can be separated into three basic groups as follows:

ERROR CODE NUMBER*	TYPE OF ERROR
30,000 - 32,700	Master Module Error (LI/LTI or RI/RTI internal error.)
20,000 - 28,192	Slot Error (Gives the first register address of the CPU rack register module that malfunctioned.)
10,000 - 18,192	Read after Write Error (Remote outputs or registers do not have the same state as commanded by the CPU.)

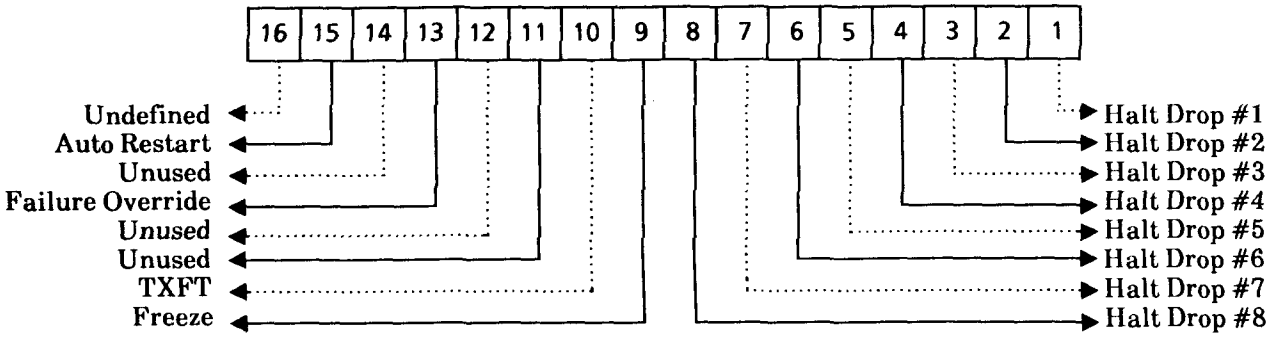
*All specific error codes are listed in Section 7.0.

Note: If the failure override bit is set in the channel control register (see Section 3.14.4 on the following page), S8175 will only indicate 30,000 and above errors. 10,000 to 28,192 errors will go unnoticed by 8175 but will be indicated by the LI/LTI error control register.

3.14.3.2 Channel Control Register

Associated with each channel contained in a local interface module is a 32 bit control register. The first 16 bits provide several LI/LTI control options which can be programmed by the user. Bits 17-32 comprise the status field and provide to the CPU operational information about the RI/RTI or LI/LTI system. A number of these bits can be used as inputs to affect the control of the options previously mentioned. A break-down and description of Channel Control Registers is given on the following pages.

3.14.4 LOCAL INTERFACE MODULE CONTROL DATA REGISTER

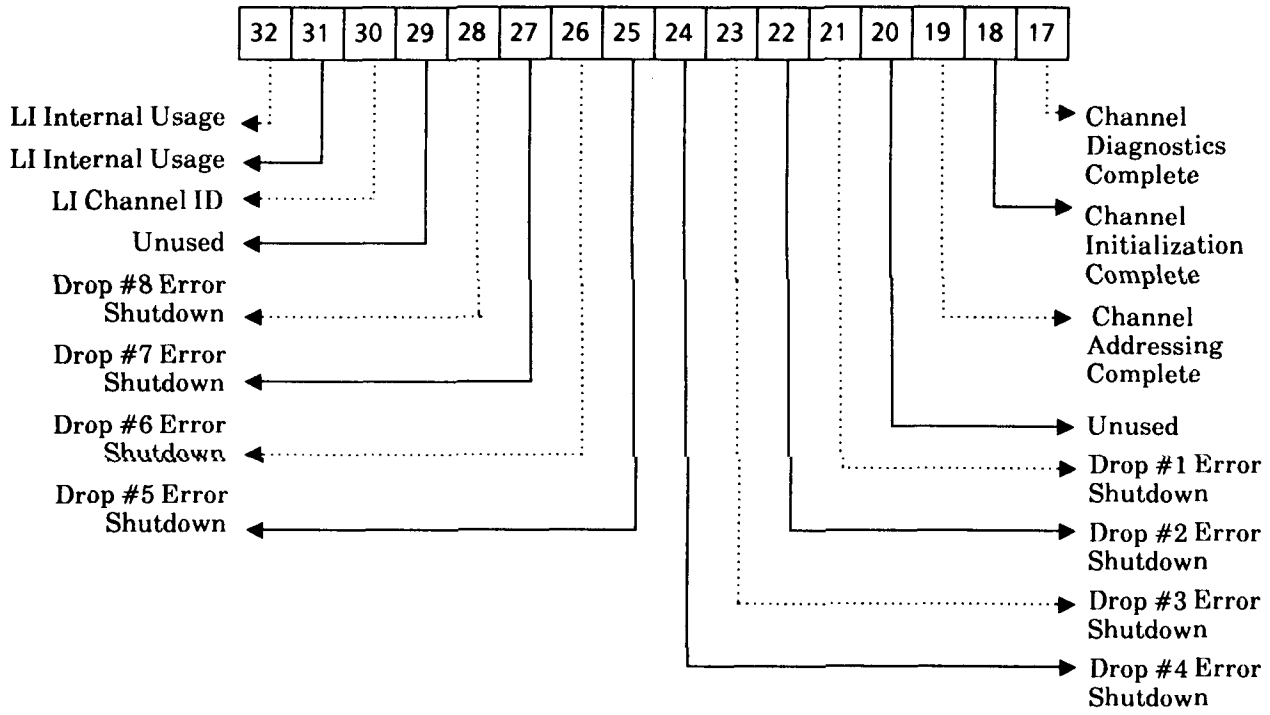


CHANNEL CONTROL REGISTER BIT *	NAME	DESCRIPTION
1 2 3 4 5 6 7 8	Halt Drop #1 Halt Drop #2 Halt Drop #3 Halt Drop #4 Halt Drop #5 Halt Drop #6 Halt Drop #7 Halt Drop #8	When OFF (0) - the drop will operate as the ladder logic indicates. When ON (1) - the drop will be shutdown. 1. Input status still valid 2. Outputs turn OFF 3. Register I/O clear (depending upon module type)
9	Freeze	When ON (1) and a loss of transmission or transmission error or local rack error occurs, all outputs are maintained in their last state.
10	TXFT	Transmission Fault Tolerance determines whether 3 or 20 consecutive transmission errors occur before a channel error is acknowledged. OFF (0) = 3 errors ON (1) = 20 errors
11	Unused	
12	Unused	
13	Failure Override	When ON (1) allows the channel to continue operating if a drop error on a channel occurs. When OFF (0) and drop error is present, channel will shutdown and processor will halt.
14	Unused	
15	Auto Restart	When ON (1) allows the channel to attempt to reestablish valid communications with any drop shutdown due to transmission errors. (Bit 13 must be set to enable bit 15 to be recognized.) This control bit accomplishes a similar function as the restart button on the LI module. **Note:** When the LI/LTI failure override bit (13) and auto restart bit (15) are set and a channel error occurs, the drop will restart automatically. When bus errors occur operator intervention is necessary. Toggle the keyswitch or press the restart button for the drop to restart.
16	Unused	

* Only in certain series of Model 300 processors. See Table 3.1 in Section 3 - page 20.

Figure 3.18 - LI Control Data Register

3.14.5 LOCAL INTERFACE MODULE CONTROL DATA REGISTER (Read Only)



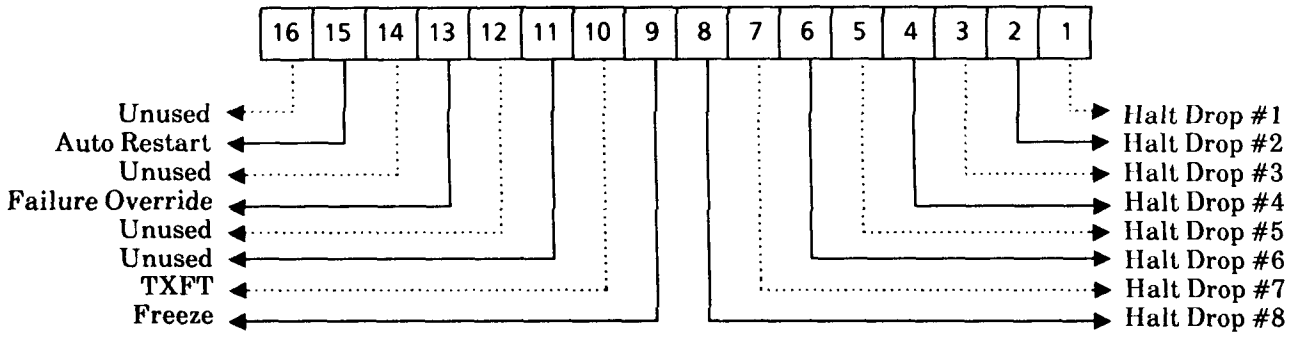
CHANNEL CONTROL REGISTER BIT	NAME	DESCRIPTION
17	Channel Diagnostics Complete	When ON (1) - LI channel completed its diagnostics.
18	Channel Initialization Complete	When ON (1) 1. RIs have completed their diagnostics. 2. Valid LI/RI communication. 3. Image table updating sequence complete.
19	Channel Addressing Complete	When ON (1), indicates the CPU has loaded valid rack addressing information into the LI.
20	Unused	
21 22 23 24 25 26 27 28	Drop #1 Error Shutdown Drop #2 Error Shutdown Drop #3 Error Shutdown Drop #4 Error Shutdown Drop #5 Error Shutdown Drop #6 Error Shutdown Drop #7 Error Shutdown Drop #8 Error Shutdown	If drop has been rack addressed: When OFF (0) drop is operating. When ON (1) drop is shutdown due to error. If drop has NOT been rack addressed: When OFF (0) no drop exists. When ON (1) drop exists without addressing.
29	Unused	
30	LI Channel ID	When OFF (0), indicates a one channel LI.
31	LI Internal Usage	
32	LI Internal Usage	

* Only in certain series of Model 300 processors. See Table 3.1 in Section 3 - page 20.

Figure 3.19 - LI Control Status Register

3.14.6 LTI CONTROL REGISTER - I/O CHANNEL

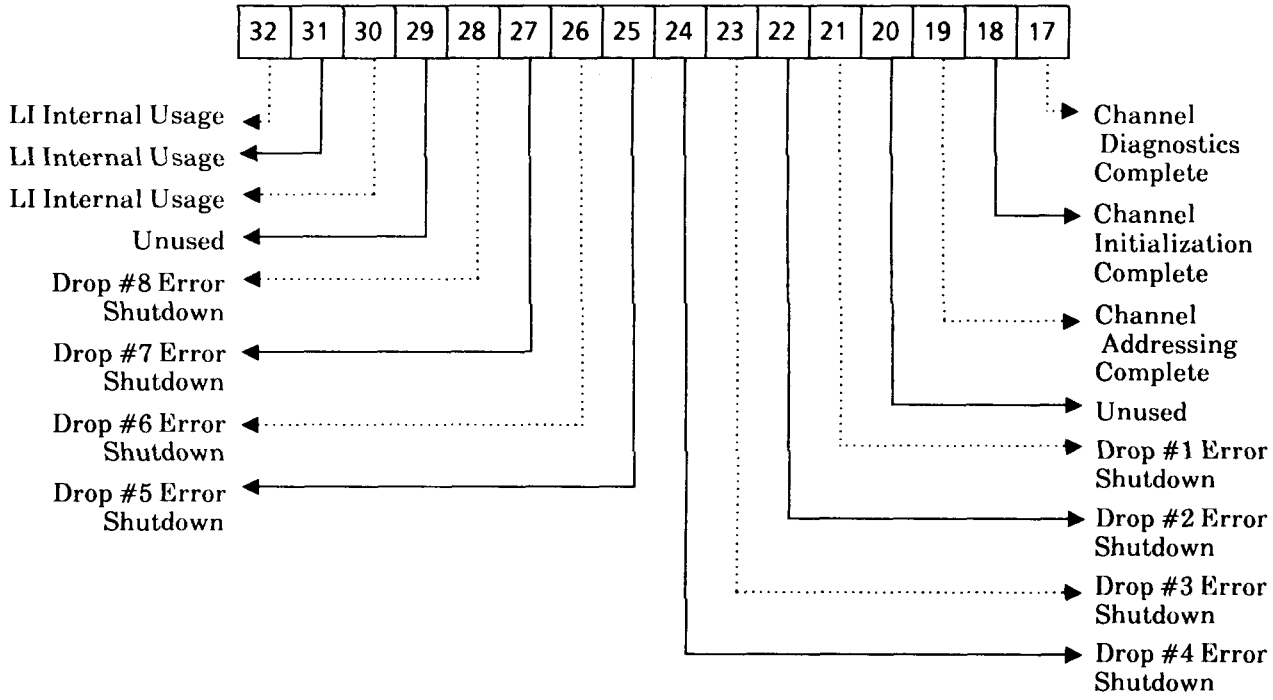
3.14.6.1 I/O Channel Data Field



CONTROL REGISTER BIT	NAME	DESCRIPTION
1 2 3 4 5 6 7 8	Halt Drop #1 Halt Drop #2 Halt Drop #3 Halt Drop #4 Halt Drop #5 Halt Drop #6 Halt Drop #7 Halt Drop #8	When OFF (0) the drop will operate as the ladder program indicates. When ON (1) the drop will be shut down. 1. Input status still valid. 2. Outputs turn OFF. 3. Register I/O clear (depending upon module type). 4. A drop shutdown under Primary control will not cause a transfer from Primary to Backup.
9	Freeze	When ON (1) and a loss of transmission, transmission error, or CPU rack error occurs, all outputs are maintained in their last state. This bit is ignored in a Primary LTI if a running Backup is able to take control.
10	TXFT (Transmission Fault Tolerance)	Transmission Fault Tolerance determines whether three or twenty consecutive transmission errors are allowed to occur before a channel error is acknowledged and an attempt is made to transfer to Backup. OFF (0) = Three Errors ON (1) = Twenty Errors
11	Unused	
12	*Unused*	
13	I/O Failure Override	When OFF (0) and drop error occurs, I/O channel will shut down and processor will HALT. When ON (1) - and **Backup is ready** - TIS will switch control to the Backup rather than run with the channel in error (thus ignoring the I/O Failure Override Bit). When ON (1) - and **Backup is not ready** - The I/O channel will be allowed to continue operating if a drop error occurs.
14	Unused	
15	Auto Restart	When ON (1) allows the I/O Channel to attempt to reestablish valid communications with any drop shut down due to transmission errors (bit 13 must be set to enable bit 15 to be recognized). This control bit performs the same function as the RESET button on the primary LTI module. This bit is only active in a Primary system with no Backup; otherwise control will be switched to the ready Backup.
16	Unused	

Figure 3.20 - LTI I/O ControlRegister Data Field

3.14.6.2 I/O Channel Status Field

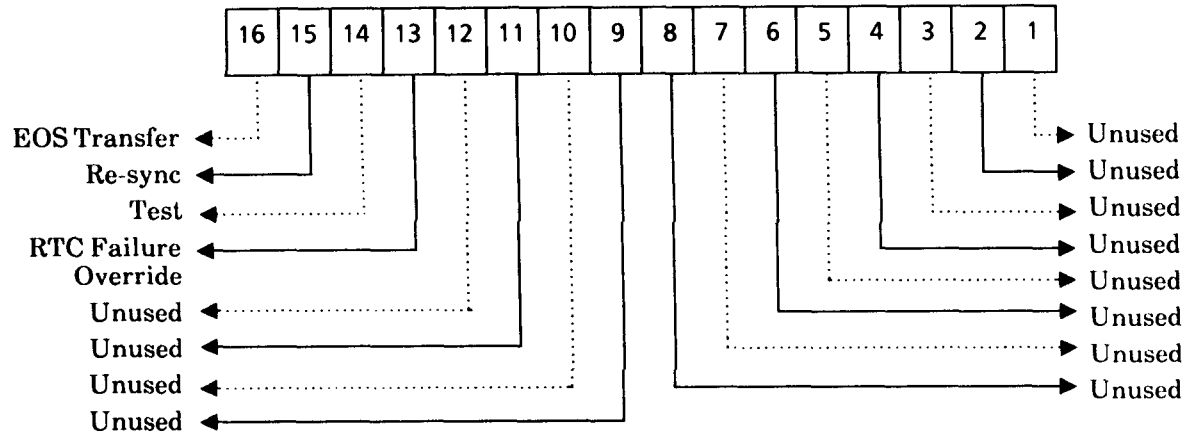


CONTROL REGISTER BIT	NAME	DESCRIPTION
17	Channel Diagnostics Complete	When ON (1) - LTI channel completed its diagnostics.
18	Channel Initialization Complete	When ON (1) 1. RTIs have completed their diagnostics. 2. Valid LTI/RTI communication. 3. Image table updating sequence complete.
19	Channel Addressing Complete	When ON (1), indicates the CPU has loaded valid rack addressing information into the LTI.
20	Unused	
21 22 23 24 25 26 27 28	Drop #1 Error Shutdown Drop #2 Error Shutdown Drop #3 Error Shutdown Drop #4 Error Shutdown Drop #5 Error Shutdown Drop #6 Error Shutdown Drop #7 Error Shutdown Drop #8 Error Shutdown	If drop has been rack addressed: When OFF (0) drop is operating. When ON (1) drop is shutdown due to error. If drop has NOT been rack addressed: When OFF (0) no drop exists. When ON (1) drop exists without addressing.
29	Unused	
30	Internal Usage	
31	Internal Usage	
32	Internal Usage	

Figure 3.21 - LTI I/O Channel Control Status Field

3.14.7 LTI CONTROL REGISTER - REGISTER TRANSFER CHANNEL

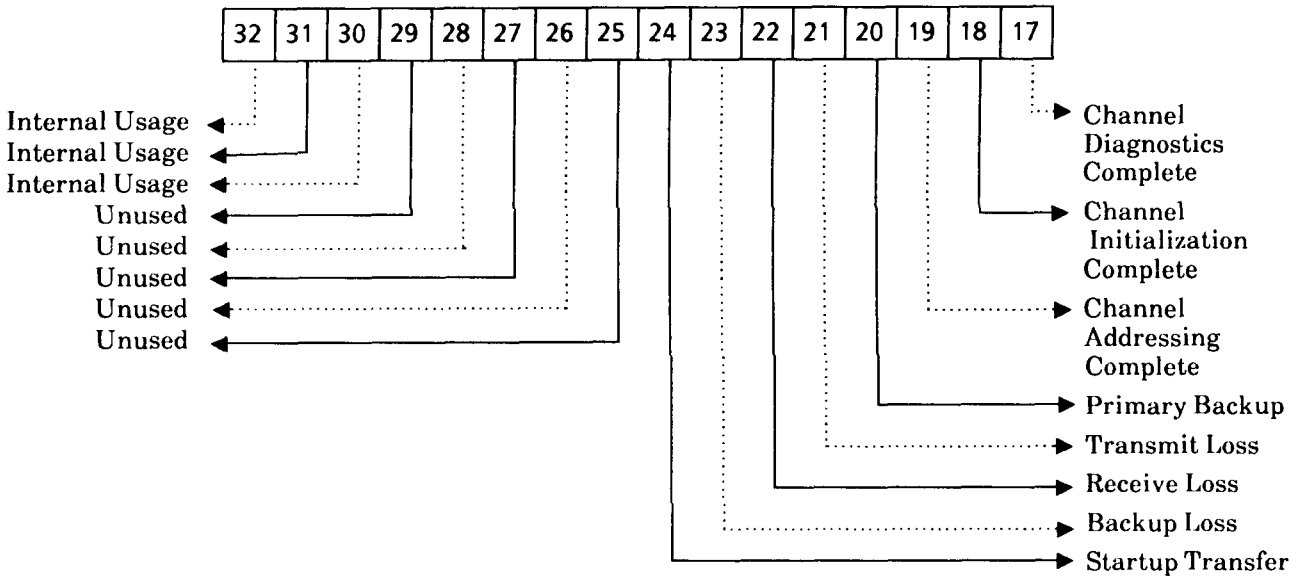
3.14.7.1 RTC Data Field



CONTROL REGISTER BIT	NAME	DESCRIPTION
1 2 3 4 5 6 7 8	Unused Unused Unused Unused Unused Unused Unused Unused	
9	Unused	
10	Unused	
11	Unused	
12	Unused	
13	RTC Failure Override	When set ON (1) in a Backup LTI, will allow Backup processor to continue to RUN despite losing synchronization with the Primary. This bit is active only in the Backup LTI.
14	Test	When set ON (1) in a Backup LTI,the LTI (upon a HALT to RUN transition) will *not* request a Startup Transfer from the Primary processor.
15	Re-sync	When set ON (1) in a Backup LTI that is in RUN, the Backup system will attempt a Startup Transfer to re-synchronize the TIS. To enable the RE-SYNC bit, the RTC FAILURE OVERRIDE bit must also be set ON (1) and the TEST bit must be reset OFF (0).
16	EOS Transfer	When set ON (1) in a Backup LTI that is in RUN, the Backup LTI will request an End of Scan Transfer of 32 registers. The block of 32 registers to be transferred is determined by the value residing in the End of Scan Transfer Register (second register assigned to the RTC).

Figure 3.22 - RTC Control Register Data Field

3.14.7.2 RTC Status Field



CONTROL REGISTER BIT	NAME	DESCRIPTION
17	Channel Diagnostics Complete	When ON (1) - LTI channel completed diagnostics. Reset OFF (0) - Self-tests are in progress.
18	Channel Initialization Complete	Set ON (1) when: 1. LTI is in RUN with a verified address map. 2. I/O channel is initialized
19	Channel Addressing Complete	Set ON (1) when address map has been loaded and verified
20	Primary/Backup	Set ON (1) when LTI is Primary. Set OFF (0) when LTI is Backup.
21	Transmit Loss	Set ON (1) when matched LTI has its RECEIVE LOSS bit set.
22	Receive Loss	Set ON (1) when LTI has not received communication from its matched pair.
23	Backup Loss	Set ON (1) in Primary LTIs that do not have a Backup that can become Primary. Reset OFF (0) when a Backup in full RUN is present. Backup LTIs will also set their BACKUP LOSS bit when they are unable to become Primary.
24	Startup Transfer	Set ON (1) one scan before a Primary does a Startup Transfer. Reset OFF (0) upon completion of the Startup Transfer.
25	Unused	
26	Unused	
27	Unused	
28	Unused	
29	Unused	
30	Internal Usage	
31	Internal Usage	
32	Internal Usage	

Figure 3.23 - RTC Control Register Status Field